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A Fast 8-Bit Wallace Tree Multiplier using MTCMOS based Dynamic Adders

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Abstract: ***A Multiplier is an Essential component to build digital circuits, like ALU, Processors, Controllers and other various applications in VLSI domain. But in DSP Processors conventional multipliers will take more silicon space, time and power. In this paper MTCMOS technology based Domino and TSPC adders are used to implement 8-bit Wallace tree multiplier. The proposed design is implemented with two dynamic adders and results are compared. Initially the two adders are designed using MTCMOS technology. The TSPC (True Single Phase Clock) adder based Wallace tree Multiplier shows highest speed, and better performance. The Dynamic MTCMOS technology reduces more leakage power compare to static CMOS technology. MTCMOS technology adds High Threshold Voltage Transistor (HVT) with actual logic for reducing leakage power. The Core logic of adder designed with Low Threshold Voltage Transistors (LVT) for higher speed of operation. The proposed design is carried out using 45 nano-meter (nm) technology using Cadence ICFB (ver.6.1.0) (Integrated Circuit Front to Back end) tool.***
Index Terms: Domino, TSPC, CMOS, MTCMOS, Power, Sleep mode, Wallace tree.

I. INTRODUCTION

Multipliers are significantly important in the area of digital systems. It plays a vital role in arithmetic operations. The speed of computation in digital systems are mainly depends upon type of multiplier. The existed multipliers has more circuitry and hence more leakage power. In portable digital systems (mobile phones, mp3 players, tablets, laptops etc) power leakage is one of the most limitation parameter. It is necessary to implement low power, high speed multipliers. But the existed static CMOS based Wallace tree multiplier is slow compare to dynamic adder based Wallace tree multiplier [1]. The proposed design is a advanced high speed, Wallace tree multiplier which composed of TSPC (True Single Phase Clock) dynamic adder [2]. To achieve high speed, the adder logic built with LVT cells, and Compressor techniques in Wallace tree multiplier.

A. DOMINO logic

The Domino logic [3] is similar to that of dynamic logic with a static CMOS logic and used to avoid cascading issues. Fig. 1 Shows Domino logic for an inverter. During Pre-charge (CLOCK= 0), output is charged to maximum VDD and output of inverter becomes zero. In the Evaluation Phase (CLOCK=1) OUTPUT makes transition from logic high to logic low. Domino logic gates can achieve high speed. The inverters can be sized to match the fan-out, which are smaller than in complimentary static CMOS. The Domino logic based full adder consists of 21 transistors and circuit is shown in fig.2.

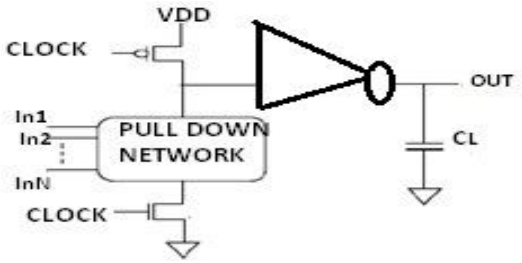

Fig1. Domino Logic

B. TSPC Logic

The TSPC (True Single Phase Clock) adder has only single phase clock, and hence TSPC logic reduces clock skew problems during the circuit operation. The circuit will be evaluated when clock signal is 1 and high impedance when clock signal is 0. TSPC full-adder logic requires only 18 transistors, where as existed design has 36 transistors. Thus the proposed Wallace tree multiplier circuit silicon area reduced to 49.96% compare to earlier design. The circuit diagram for 1 bit TSPC full adder is shown in fig 4. The proposed design has conclusion in section V.

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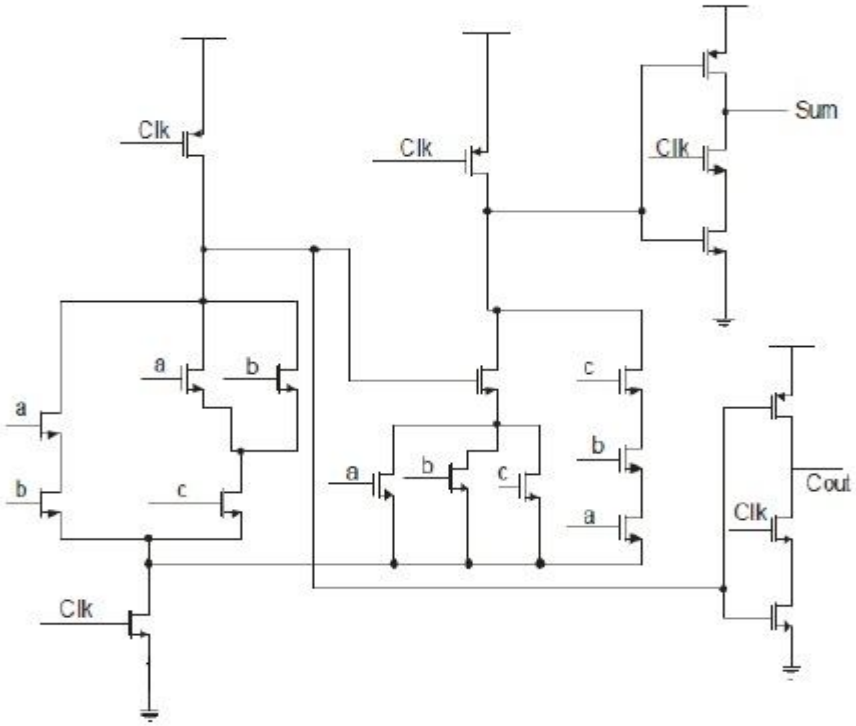

Fig2. Domino logic for 1 bit full adder circuit

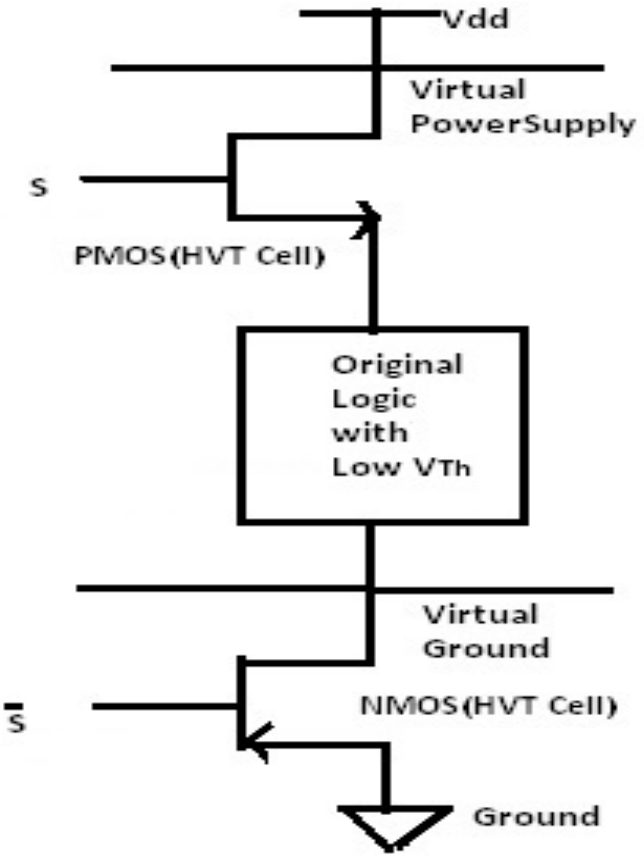

Fig 3. Basic MTCMOS LOGIC

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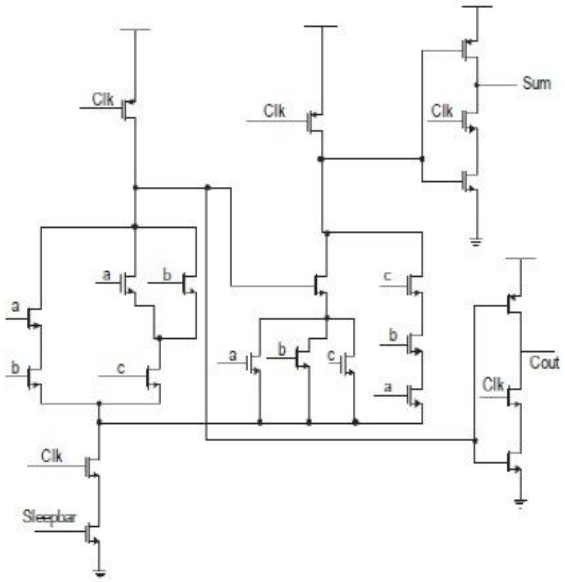

Fig4. TSPC logic for 1 bit full adder circuit

C. MTCMOS Dynamic Logic

MTCMOS logic a very efficient technique for reducing sub threshold leakage power during idle mode [4]. MTCMOS technology is directly to use because existing design can easily be changed into MTCMOS based circuits simply by adding high threshold voltage (HVT) power supply switches. Multi Threshold Voltage CMOS (MTCMOS) Logic is to improve speed performance and less power consumption. Leakage power can be reduced up to 90% compare to static CMOS technology.

II. WALLACE TREE MULTIPLIER

The Wallace tree multiplier is the fastest multiplier than all existed multipliers. It reduces partial product count and the intermediate stages. The Wallace tree operation includes three stages , the first phase is to generate Partial products, in second stage partial products are reduced, in final stage addition can be performed. The Wallace tree structure is shown in Fig 5.

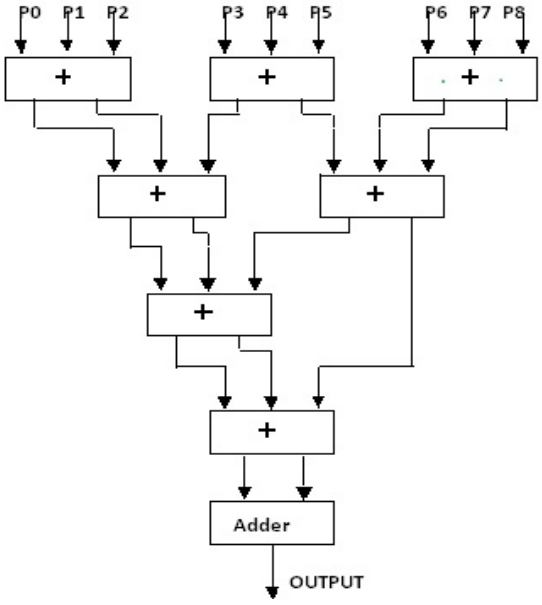

Fig 5.Wallace tree multiplier structure

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III. PROPOSED SYSTEM

The proposed architecture aims to reduce the maximum delay. This leads to increased speed of operation and decreases power consumption. The proposed Wallace tree design has compressors, one half adder, one full adder and one conventional parallel adder for final stage addition of two rows. The first stage has one full adder, In the second stage, two full adders have been grouped using a 4 by 2 Compressor. Similarly, the 3'rd stage consists of a 5 by 2 compressor, which is a combination of three full adders and so on. The graphical representation of one 5 by2 compressor is shown in Fig 5. The number of inter connections are taken care of, because they play a important role in the flow of carry from one stage to the next stage the tree structure.

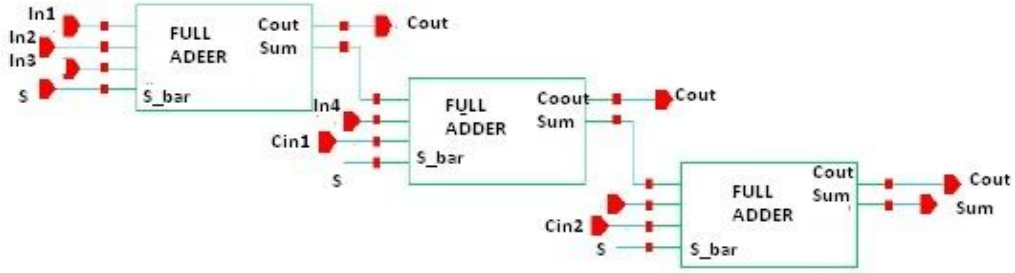

Fig 6. 5 by 2 Compressor schematic circuit.

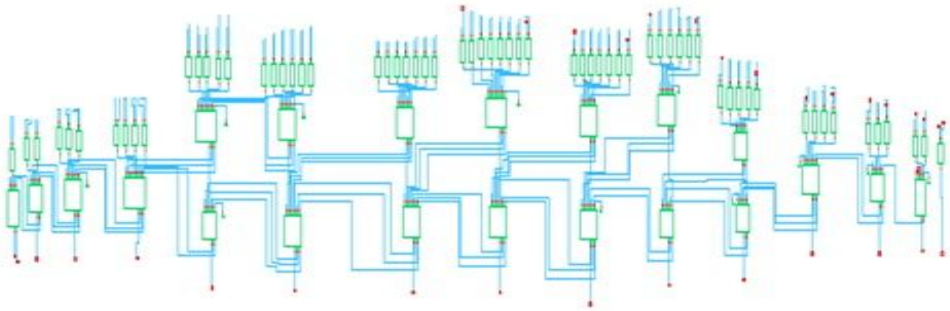

Fig 7. Implementation of Wallace tree multiplier Schematic circuit

IV. RESULTS

The 8 bit fastest Wallace tree multiplier designed and simulated using Cadence ICFB version 6.1.0 tool package. The Eight bit Wallace tree schematic circuit is shown in Fig 7. Initially two separate i.e Domino and TSPC adders are designed and simulated. The TSPC adder has achieved better performance than static CMOS and Domino adders. The simulated waveform for 8-bit TSPC adder and 8-bit Wallace tree multiplier is shown in Fig.8 and Fig.9 respectively.

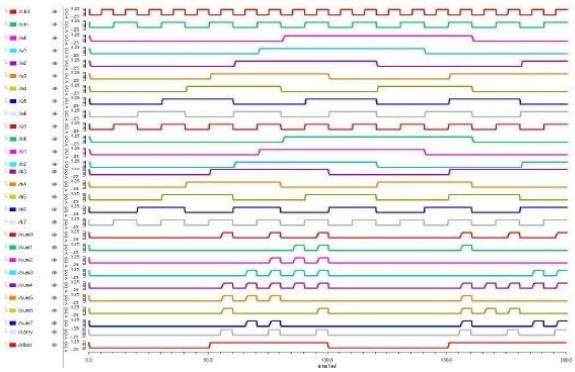

Fig 8. An eight- bit TSPC adder simulated waveform

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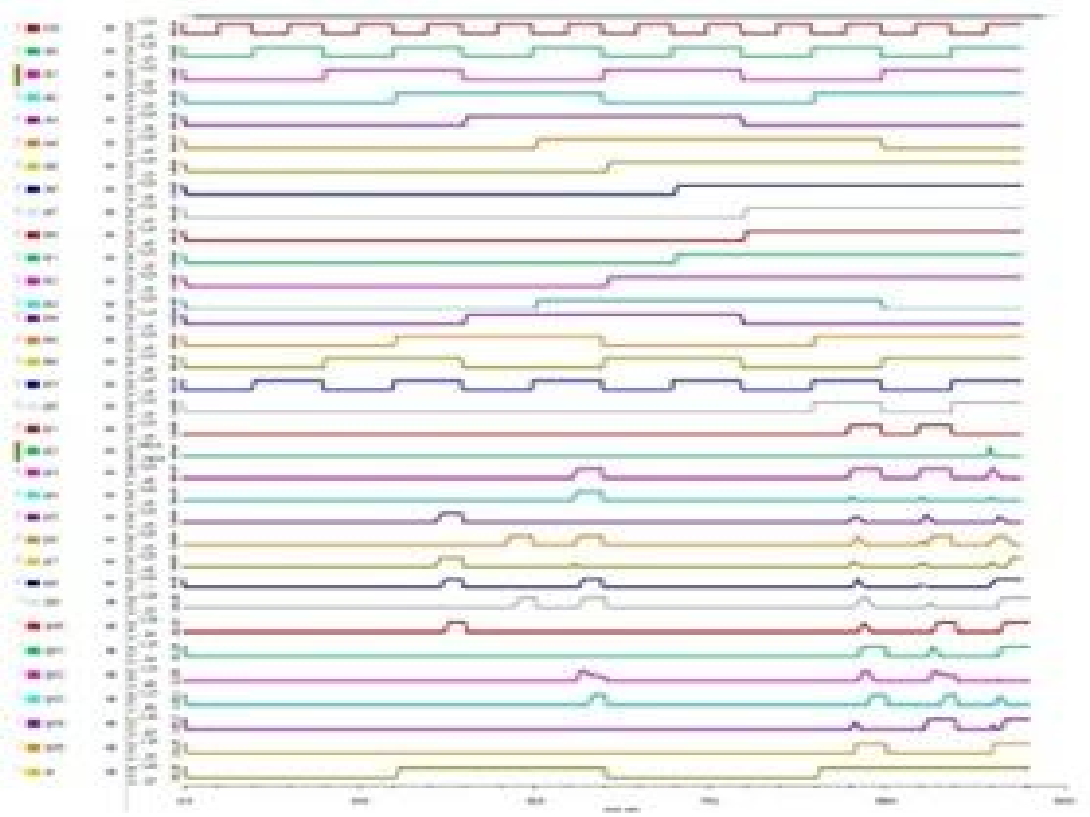

Fig 9. An 8-bit Wallace tree multiplier simulated waveform

Table 1 shows the Comparison of Power and Delay in CMOS and MTCMOS technology for TSPC and Domino adder based Wallace tree multiplier The analysis's for power, Leakage power and delay is calculated, and compared. The comparison graph for Wallace tree multiplier power and delay product using different adders are shown in Fig 10.

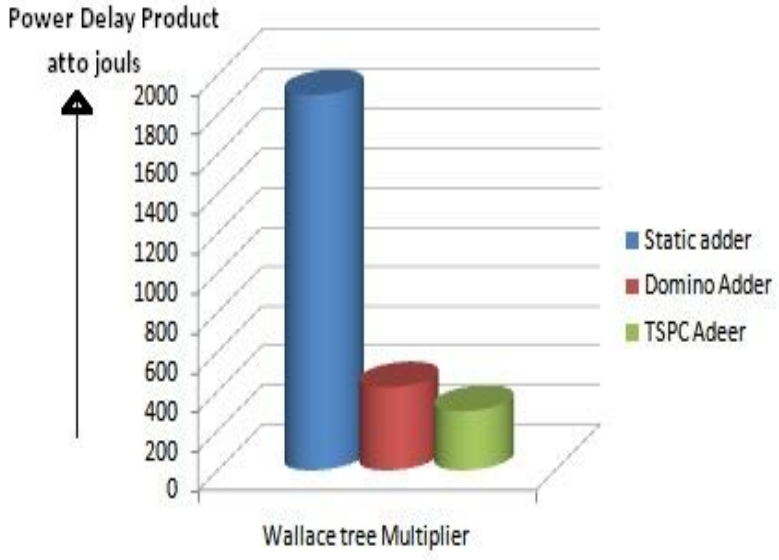

Fig 10. Power delay product versus different technologies of adder based Wallace tree multiplier

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Table-I: Comparison of Power and Delay in CMOS and MTCMOS technology for TSPC Adder

Wallace Tree MULTIPLIER	Average Power Dissipation (µW)	Delay (ps)
Static CMOS Adder based multiplier (Existed)	69.72	272.3
Domino dynamic MTCMOS Adder based multiplier (Proposed)	68.23	62.5
TSPC dynamic MTCMOS Adder based multiplier (Proposed)	61.6	56.2

V. CONCLUSION

An eight bit Wallace tree multiplier is designed by using MTCMOS dynamic logic adders, and verified using 45 nano-meter technology[5]. The Wallace tree is fast since the critical path delay is less due to two reasons, first one is, MTCMOS Dynamic technology, second one is minimum number of transistors and compressors used. The speed, area and power consumption of the TSPC based Wallace tree multipliers will be improved. The delay for existed design is 272.3ps, and for proposed design it is reduced to 56.2ps. The leakage power can be reduced to 90% compare to existing design.

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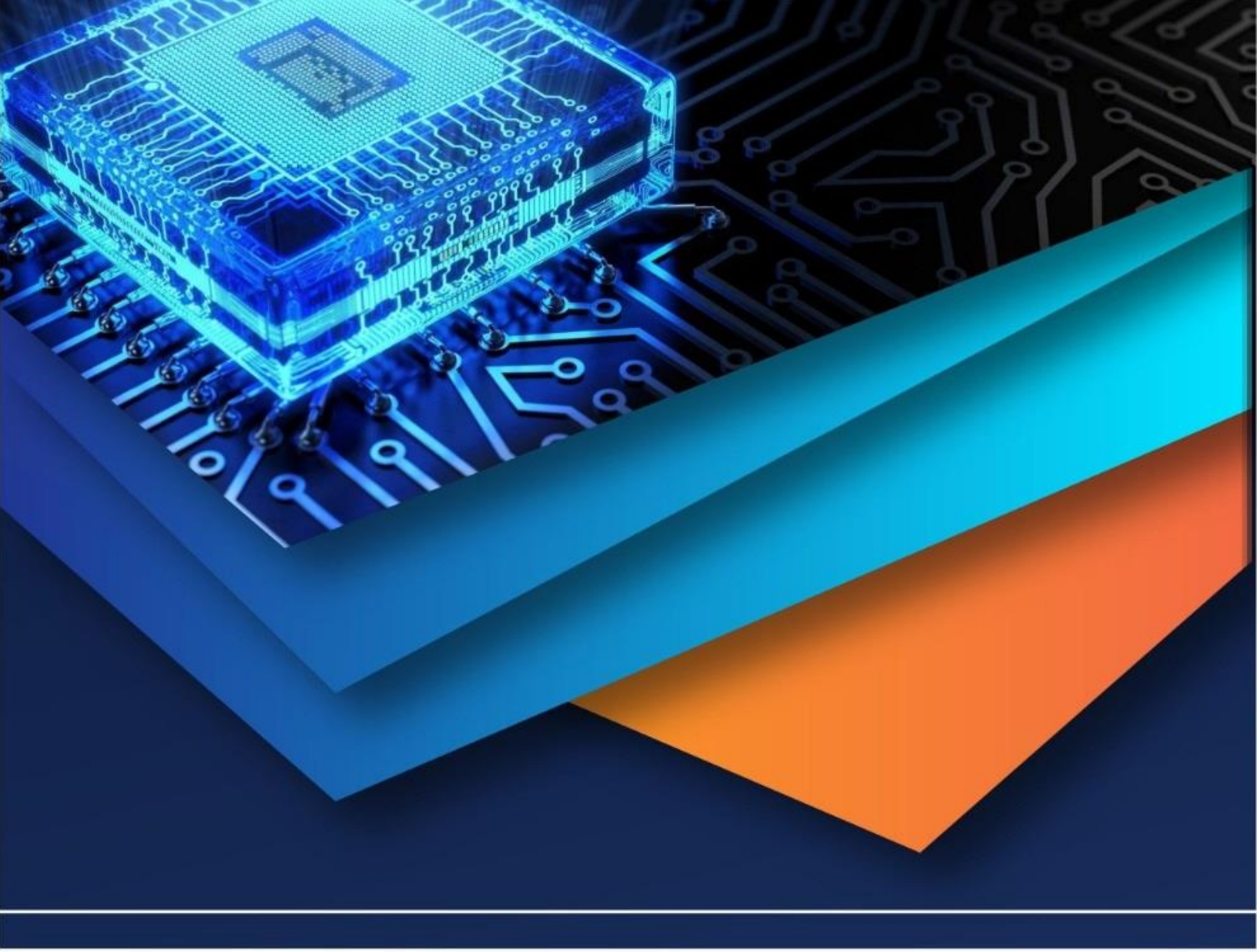

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