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A Low Power Higher Order Switched capacitor design for Sigma Delta ADC`s

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Abstract*: *In this paper the fifth order sigma-delta ADC using switched-capacitor is proposed. The feed-forward architecture is used in sigma-delta ADC with oversampling ratio (OSR) of 64. The modulator input signal range is more than the full scale of the quantizer with suitable coefficients scaling and internal DAC reference scaling. To improve the linearity of a multi-bit DAC, A 25-level quantizer with data weighted averaging dynamic element matching technique is employed. The sigma delta ADC implemented in a 40nm CMOS process achieves 93.7 dB peak signal-to-noise and distortion ratio (SNDR), 94.2 dB peak signal-to-noise ratio (SNR) with 1 KHz input signal over 6.25KHz signal bandwidth while consuming 2mW (1.8mw of analog power and 200uw of digital power) with the clock frequency of 400 KHz at 1.2V supply voltage. The designed low power fifth order sigma delta ADC shows very high figure of merit (FOM) with optimized performance.

Keywords: dynamic element matching (DEM), feed-forward architecture, ADC, fifth order Delta-sigma modulator, low power, optimized performance and high figure of merit.

I. INTRODUNCTION

With the development of the technology and accuracy challenges, people are paying more and more attention on the data conversion precision. It needs the analog to data converter with high accuracy in the temperature monitoring systems, high fidelity audio system, Aanlog and Digital converter must have more than 16-bit resolution. However, when adapting the traditional ADC convert principle, based on the double integral model it won't have so high accuracy. Sigma-delta is an accomplishment method to realize converter with high accuracy. It uses the over sampling principle to compress the energy of quantization noise largely in the signal frequency band, and finally, through the down sampling accomplished by decimation filter, so the higher SNDR can be obtained. Comparing the converters with other structures, sigma-delta ADC has the advantages of high accuracy, linearity and large dynamic range etc.

Sigma-delta ADC mainly consists of front end modulator and digital decimation filter, and according to bit of the modulator, it can be divided into single-bit quantization and multi-bit quantization. The current low order and single-bit ADC [1] is limited by the order of modulator and single-bit quantization, which decreases the possibility to get the higher SNDR. With the wider application of sigma-delta ADC, the more demand for sigma-delta ADC . The SNR is the uppermost parameter to measure the performance, and it can be improved largely by changing the modulator order, over sampling rate and quantization bits. Even though increasing the modulator order can largely improve the SNR, the attendant problems have emerged, such as the stability and complexity of circuit, and so on [2]. These problems are also serious in low voltage and low power circuits at present. Moreover, the performance of the modulator can be improved through the increased resolution of the quantizer. However, the nonlinearity caused by the multi-bit DAC of the first integrator is directly referred to the input signal of the modulator and degrades the overall performance. To enhance the multi-bit DAC linearity, a DEM technique is typically employed [3].

In this paper, a low power multi bit fifth order sigma-delta ADC by using the simple coefficients scaling method to extend the input signal range is presented. This paper is organized as follows. Section II discusses the proposed sigma-delta modulator architecture. Section III describes MATLAB Simulink model. Section IV describes details of the circuit implementation. In SectionV simulation results are presented. The overall conclusion is discussed in Section VI.

II. PROPOSED FIFTH ORDER MODULATOR ARCHITECTURE

The proposed block diagram of sigma-delta ADC is shown in Fig. 1. It consists of a fifth-order sigma-delta modulator containing 25-levels quantizer. The Delayed feed-forward path is employed to guarantee the timing margin of the modulator [4]. Allowable input signal range of the modulator is extended by scaling the gain coefficients *e* and *h*. Two resonators consist of second and third, fourth and fifth integrators are adopted to reduce the in-band quantization noise. The distortion introduced by the capacitor mismatches in the multi-bit DAC is attenuated by using the DEM logic.

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A. Delayed feed-forward

In The proposed ADC the low-distortion feed-forward architecture is employed [4]. The conventional feed-forward architecture is shown in Fig. 2, the modulator input signal, X is eliminated by the subtraction of delay free path feedback signal starting from the modulator input to the first integrator DAC input through the quantizer. As a result, the first integrator processes only shaped quantization noise and there is no distortion introduced by the integrator. However, in high speed operation, it is difficult to implement delay free path feedback signal due to the limited timing margin. In the proposed sigma-delta modulator, one clock delay is inserted into the feed-forward path to relax the timing requirement as shown in Fig. 3. With this one clock delay insertion, nth order shaped input signal appears at the output of the first integrator which is small enough for the target performance of the proposed sigma-delta ADC [5]-[6].

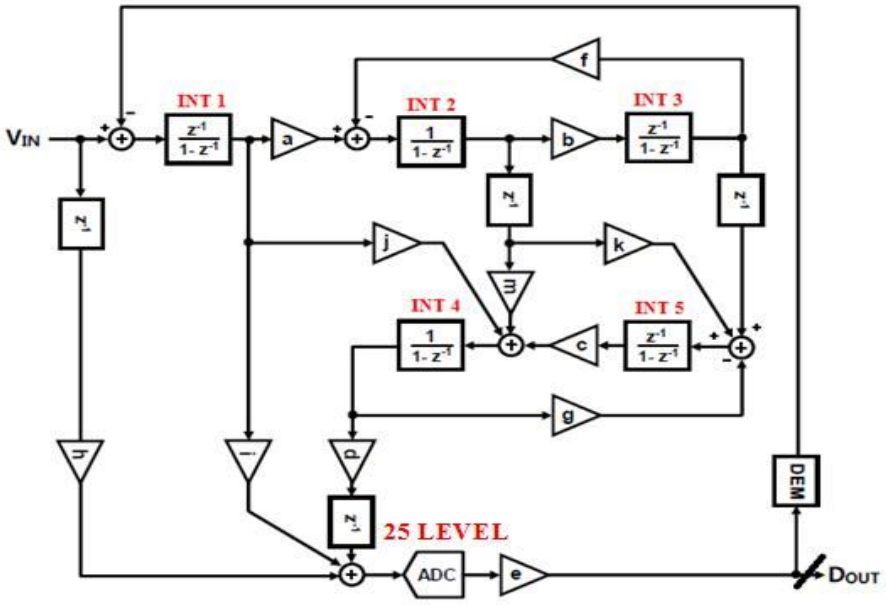

Fig.1. Proposed fifth order sigma delta AD

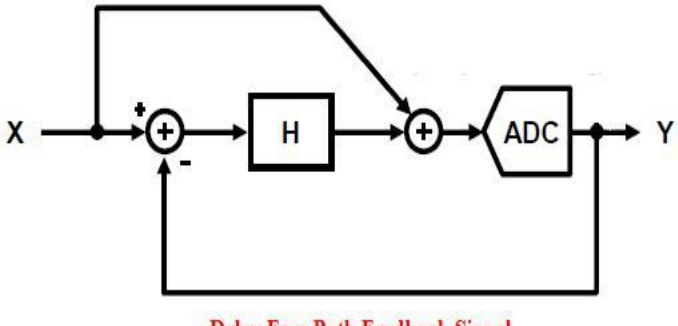

Fig.2. Linearized model of the proposed sigma-delta ADC

B. Input signal range

The stable operation of single-stage modulators are disturbed by higher the input signal swings at the output of the integrators and the input of the quantizer. Even though the feed-forward architecture contributes to lowering the output swing of the integrators, overloading of the quantizer input resulted by the large input signal of the modulator still disturbs the stable operation. The proper coefficients scaling and DAC reference voltage scaling are used, To avoid the overloading of the quantizer input and increase stable input signal range. Fig. 3 shows a linearized model of the proposed modulator with loop filter H. Since the gain from input, X to the output, Y is almost unity in the signal bandwidth, node voltage, V1, at the input of the quantizer contains input signal component

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divided by gain coefficient *e*. To avoid the quantizer overloading, swing range of V1 can be scaled down by increasing the gain coefficient *e* at the output of the quantizer. The full scale of the DAC is increased as compared with the full scale of the quantizer to cover the amplified digital output by the gain coefficient *e*. The full scale of the quantizer is 0.65 Vp-p, while the internal DAC is 0.9 Vp-p. With gain coefficient, stable input signal range of the modulator is increased by 1dB above the full scale of the quantizer.

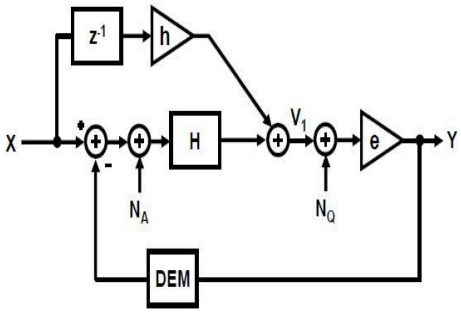

Fig.3. Linearized model of the proposed sigma-delta ADC

C. Resonators

The higher operating clock frequency dramatically increases power dissipation. In wide-band sigma-delta modulators. Moreover, the operating speed is limited by the process technology even with the more power consumption so the allowable OSR is limited. In the proposed modulator, OSR of 64 is selected by considering the process technology and power budget. To improve SNDR with selected OSR, the proposed modulator employs two notches within the signal band [7]. The closed loop of second, third and fourth, fifth integrators make notches respectively.

III. MATLAB SIMULINK MODEL OF PROPOSED ARCHITECTURE

The MATLAB-based system level analysis [8]-[10] is performed for fifth order sigma delta ADC design. The behavior of the proposed design is implemented using a Simulink model to extract some parameters. The complete Simulink model is shown in Fig.4. The non-idealities such as sampling jitter, kT/C noise and amplifier parameters as in white noise, slew rate, finite bandwidth, slew rate, saturation voltages and power supply noise are implemented in the model. Table I provides the ideal and actual performance parameters of the proposed design which matches closely with simulation results.

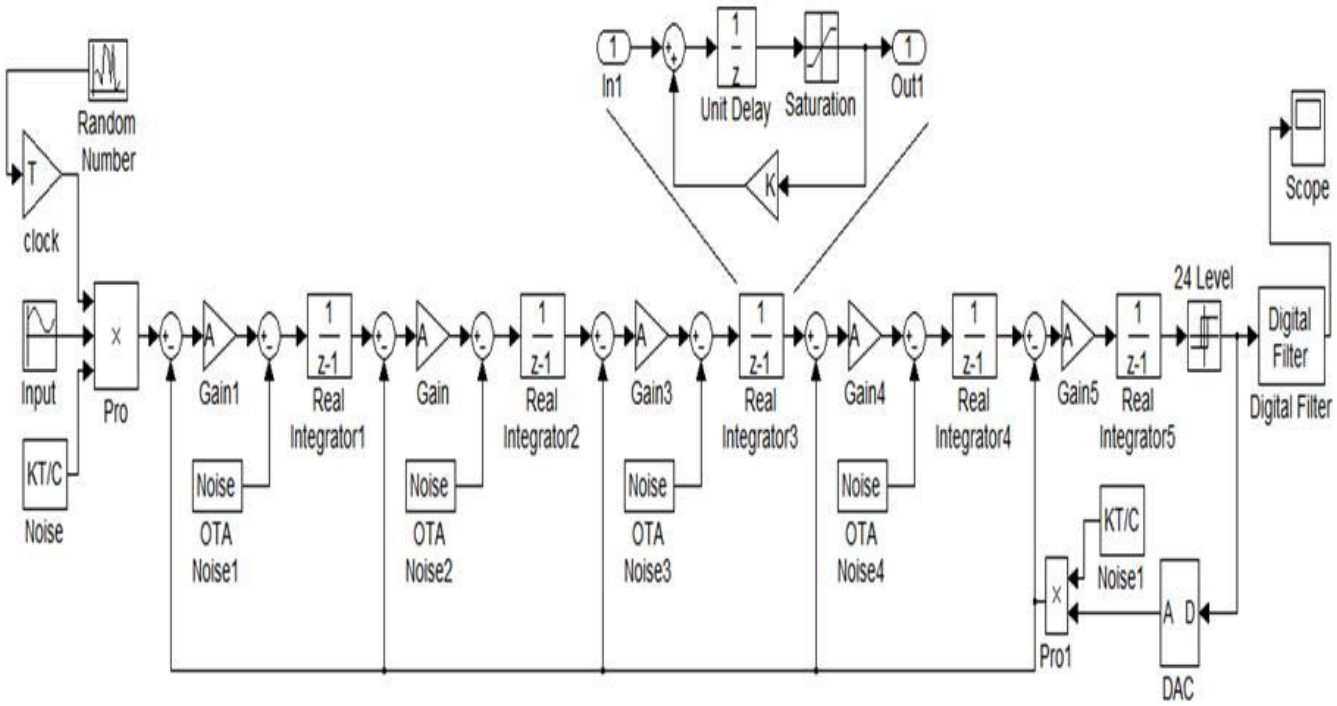

Fig.4. MATLAB Simulink model of the proposed sigma-delta ADC

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B. Jitter

Jitter is the deviation from true periodicity of a presumed periodic signal in electronics and telecommunications, often in relation to a reference clock source.

Sampling Jitter:- In analog to digital and digital to analog conversion of signals, the sampling is normally assumed to be periodic with a fixed period—the time between every two samples is the same. If there is jitter present on the clock signal to the ADC or DAC, the time between samples varies and instantaneous signal error arises. The error is proportional to the slew rate of the desired signal and the absolute value of clock error.

B. Slew Rate

The slew rate of an electronic circuit is defined as the maximum rate of change of the output voltage. Slew rate is usually expressed in units of V/μs. The limitations in slew rate capability can give rise to nonlinear effects in electronic amplifiers. For a sinusoidal waveform not to be subject to slew rate limitation, the slew rate capability (in volts per second) at all points in an amplifier must satisfy the condition "$SR \geq 2\pi Vpk$". Where f is the operating frequency and Vpk is the peak amplitude of the waveform.

C. kT/C Noise

Johnson–Nyquist noise (thermal noise, Johnson noise, or Nyquist noise) is the electronic noise generated by the thermal agitation of the charge carriers (usually the electrons) inside an electrical conductor at equilibrium, which happens regardless of any applied voltage. Thermal noise on capacitors is referred to as kT/C noise. Thermal noise in an RC circuit has an unusually simple expression, as the value of the resistance (R) drops out of the equation. This is because higher R contributes to more filtering as well as to more noise. The noise bandwidth of the RC circuit is 1/(4RC), which can substituted into the above formula to eliminate R. The mean-square and RMS noise voltage are considered. Thermal noise accounts for 100% of kT/C noise, whether it is attributed to the resistance or to the capacitance.

D. White Noise

In signal processing, white noise is a random signal with a constant density. White noise refers to a statistical model for signals and signal sources, rather than to any specific signal. The term is also used for a discrete signal whose samples are regarded as a sequence of serially uncorrelated random variables with zero mean and finite variance. Depending on the context, one may also require that the samples be independent and have the same. In particular, if each sample has a normal distribution with zero mean, the signal is said to be Gaussian white noise.

E. Dc gain

The dc gain of the integrator described by infinite. In practice, however, the actual gain is limited by circuit constraints and in particular by the operational amplifier open loop gain. The consequence of this integrator "leakage" is that only a fraction of the previous output of the integrator is added to each new input sample. The limited dc gain of the integrator increases the in-band noise.

F. Bandwidth

In computing, bandwidth is the bit-rate of available expressed typically in metric multiples of bits per second.

G. Saturation

Saturation is the fully conducting state in semiconductor junction. The term is used especially in applications involving diodes and bipolar transistors.

TABLE I Ideal and actual parameters of proposed design

Parameter Modeling	SNDR (dB)
Proposed Ideal ADC Model	98.9
Sampling Jitter	98.4
KT/C noise	97.6
Amplifier White Noise	97.2
Amplifier finite Bandwidth	96.5

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Amplifier Slew Rate	95.6
Amplifier Saturation Voltage	95.0
Charge Injection	94.5
Clock Feed through	94.2
50-60 Hz Power Supply Noise	93.9

IV. CIRCUIT IMPLEMENTATION OF PROPOSED BDESIGN

In this section circuit design implementation of integrator amplifier, latched comparator, adder and interpolating quantizer are described in detail.

A. Integrator Amplifiers

The most of the power consumed by Amplifiers are the most critical circuits which are used in the sigma-delta modulator. Single-stage folded-cascade integrator amplifier with the common-mode feedback shown in Fig. 5 is employed to guarantee the low-voltage operation in the proposed sigma delta modulator.

The NMOS input differential pair is used to bias the input common-mode voltage of the amplifier near to ground, thus small size PMOS transistors can be used for the switches connected to the input of the amplifiers. Also, the low level input common-mode voltage allows the use of cascoded tail current source for the input differential pair which results in improved common-mode rejection ratio (CMRR) and the accuracy of the bias current. The DC gain of 98 dB is achieved by using this opamp.

B. Latched Comparator

The schematic of the comparator which is shown in Fig.6 consists of preamplifier and latch. When LAT signal is low, the preamplifier amplifies input signal and the latch is in reset mode. When LAT signal goes high, the latch is triggered to regenerate the output signal of the preamplifier.

C. Adder

The summing node is employed in front of the quantizer using an active adder in amplifier . Although the passive adder can be used without an extra amplifier and power consumption, there is signal attenuation at the input of the comparator which limits the accuracy of the quantizer especially when a multi-bit quantizer is employed in the modulator. To guarantee the reliable operation of the quantizer and reduce the kick back noise from the latches, active adder is used at the expense of the additional power consumption and area

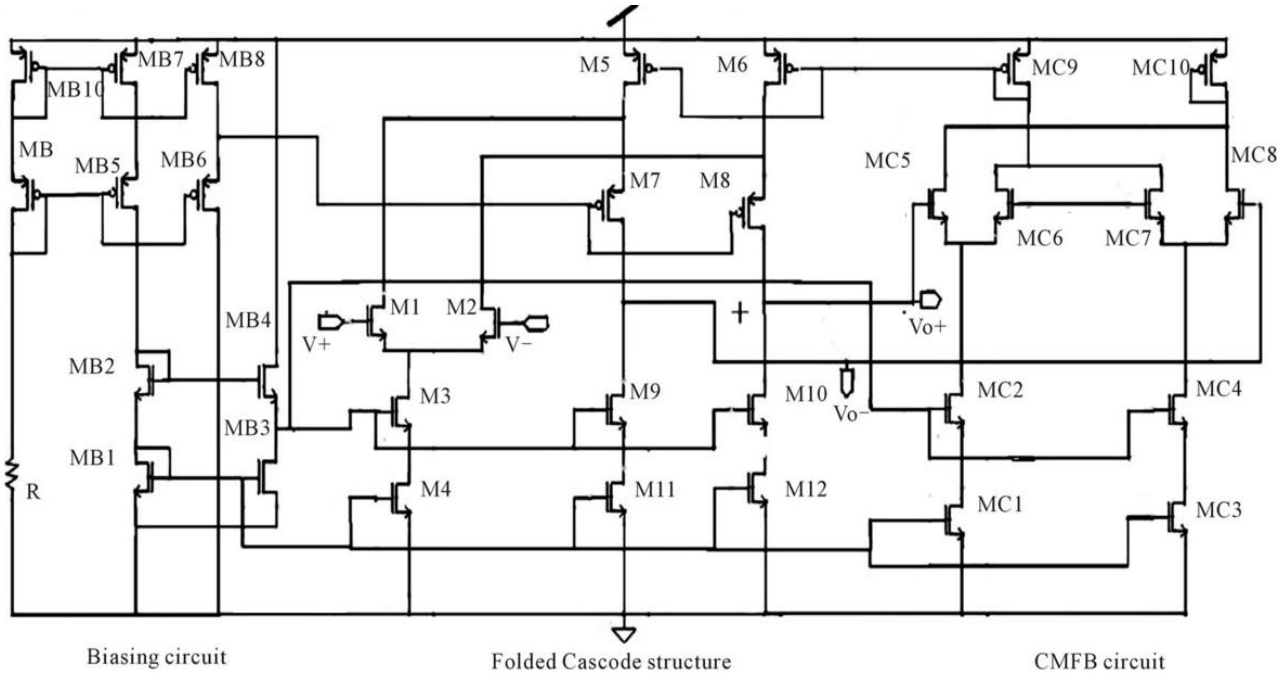

Fig.5. Schematic of Integrator Amplifier

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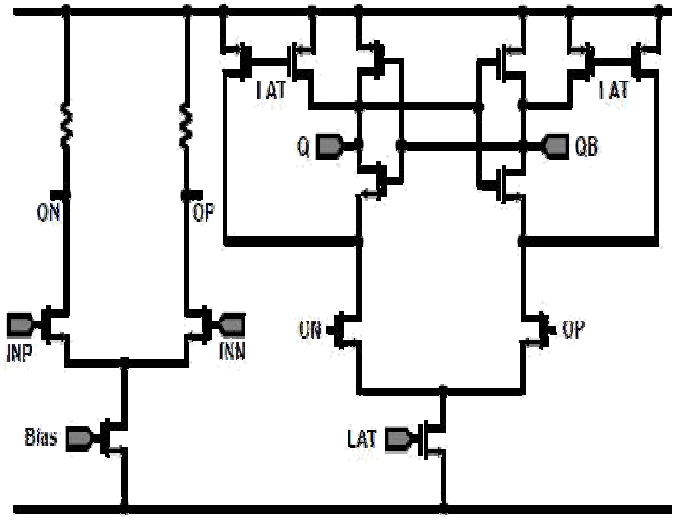

Fig.6. Schematic of Latched Comparator

D. Interpolating quantizer and DEM

A 25-level quantizer is used in the proposed modulator. Preamplifiers followed by latches are employed to reduce the input referred offset and kick back from the latches. In order to reduce the number of preamplifiers in the quantizer, interpolating technique is used as illustrated in Fig. 5 [10]. 26 latches and 13 preamplifiers including dummy pattern are employed in the 25-level quantizer. Data weighted averaging logic is located in digital feedback path to reduce the mismatch error between DAC capacitors [3]. The block diagram of the Data weighted averaging logic is illustrated in Fig 7. The shifter shuffles selected unit DAC capacitors according to the output of the pointer generator. The pointer generator calculates the origin of the selection by using its previous output and the current output of the quantizer.

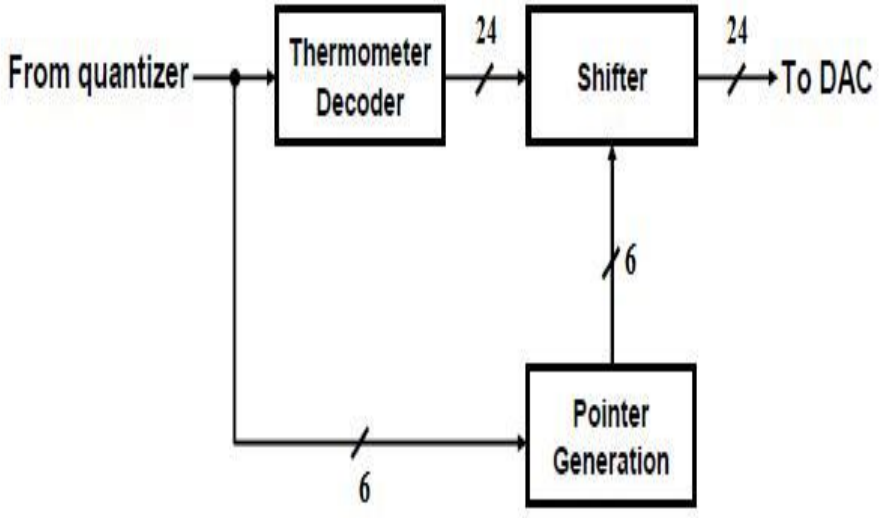

Fig.7. Block diagram of Data weighted averaging logic

V. SIMULATION RESULTS

The proposed design fifth order sigma delta ADC is designed in 40nm standard CMOS technology. Fig.8 shows the proposed design layout view and measured active die area is 0.91 mm2. Fig. 9 shows the measured power spectrum of the output for a 1 KHz, 1 dBFS sine wave input with 400 KHz clock frequency. The SNDR vs. input amplitude curve is shown in Fig.10 [13]-[14]. The measured results demonstrate that the modulator can process input beyond the full scale of the quantizer without overloading. The

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peak SNDR and SNR reach 93.7 dB and 94.2 dB, respectively. The figure of merit (FOM) [7] of the proposed design is 166.4, the total power dissipation is 2 mW (analog: 1.8 mW, digital: 200uW) with 1.2 V supply voltage. The overall measured results are summarized in Table II.

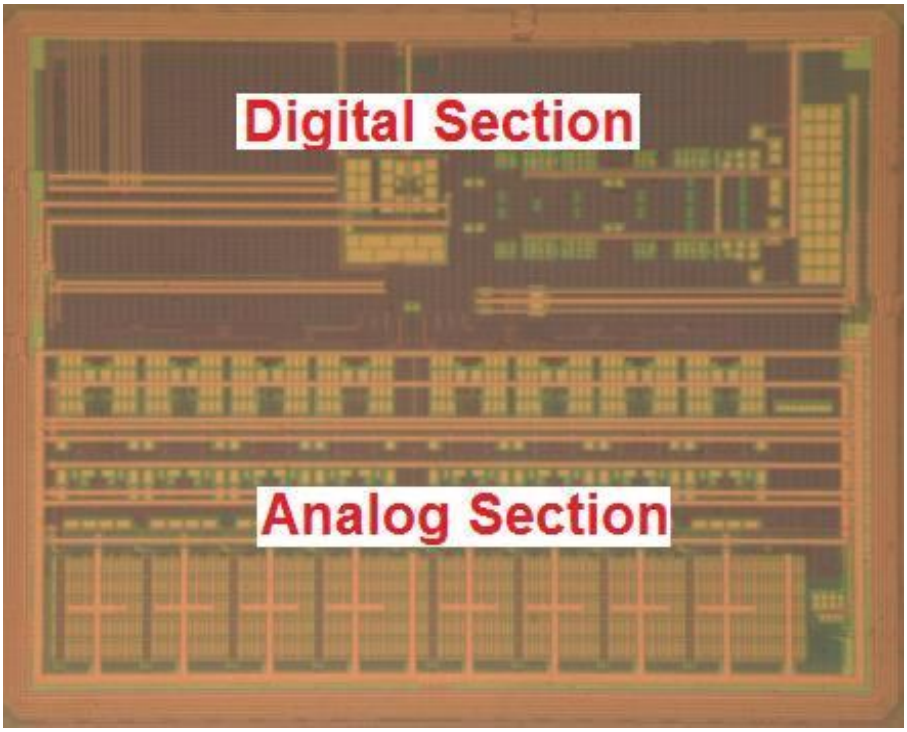

Fig.8. Proposed Design Layout View

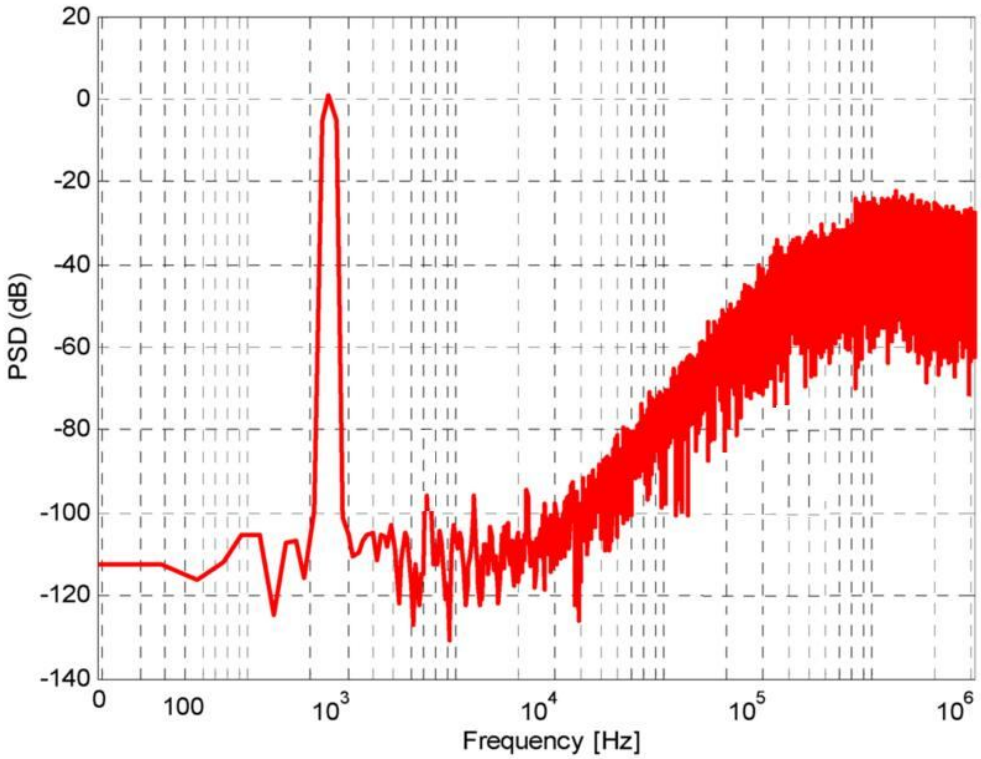

Fig.9. Measured Output Spectrum

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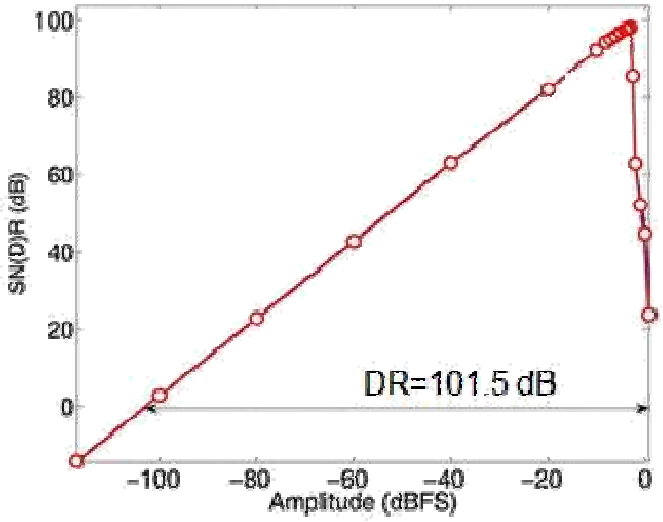

Fig.10. Measured SNDR w.r.t Input amplitude

TABLE II Measured Results Summary

Technology	40nm CMOS Process
Power Supply	1.2V
Input Range	0.9 Vp-p,diff
Clock Frequency	400 KHz
Oversampling Ratio	64
Signal Bandwidth	6.25 KHz
Dynamic Range	101.5 dB
Peak SNR	94.2 dB (@ Input=1KHz)
Peak SNDR	93.7 dB (@ Input=1KHz)
Power Consumption (Analog+Digital)	2mW (1.8mw + 200uw)
Figure of Merit (FOM) ADC	166.44
Layout Active Area	0.91 mm^2

VI. CONCLUSION

A low power fifth order sigma delta ADC in 40nm CMOS process is presented in this paper. The Simulation results verify the effectiveness of the proposed design technique to achieve low-power and high-accuracy, the proposed sigma-delta ADC has wide stable input range beyond the full scale of the quantizer by using feed-forward architecture [12] and proper coefficients scaling. The FOM of the proposed sigma ADC proves that the presented modulator has highly optimized performance.

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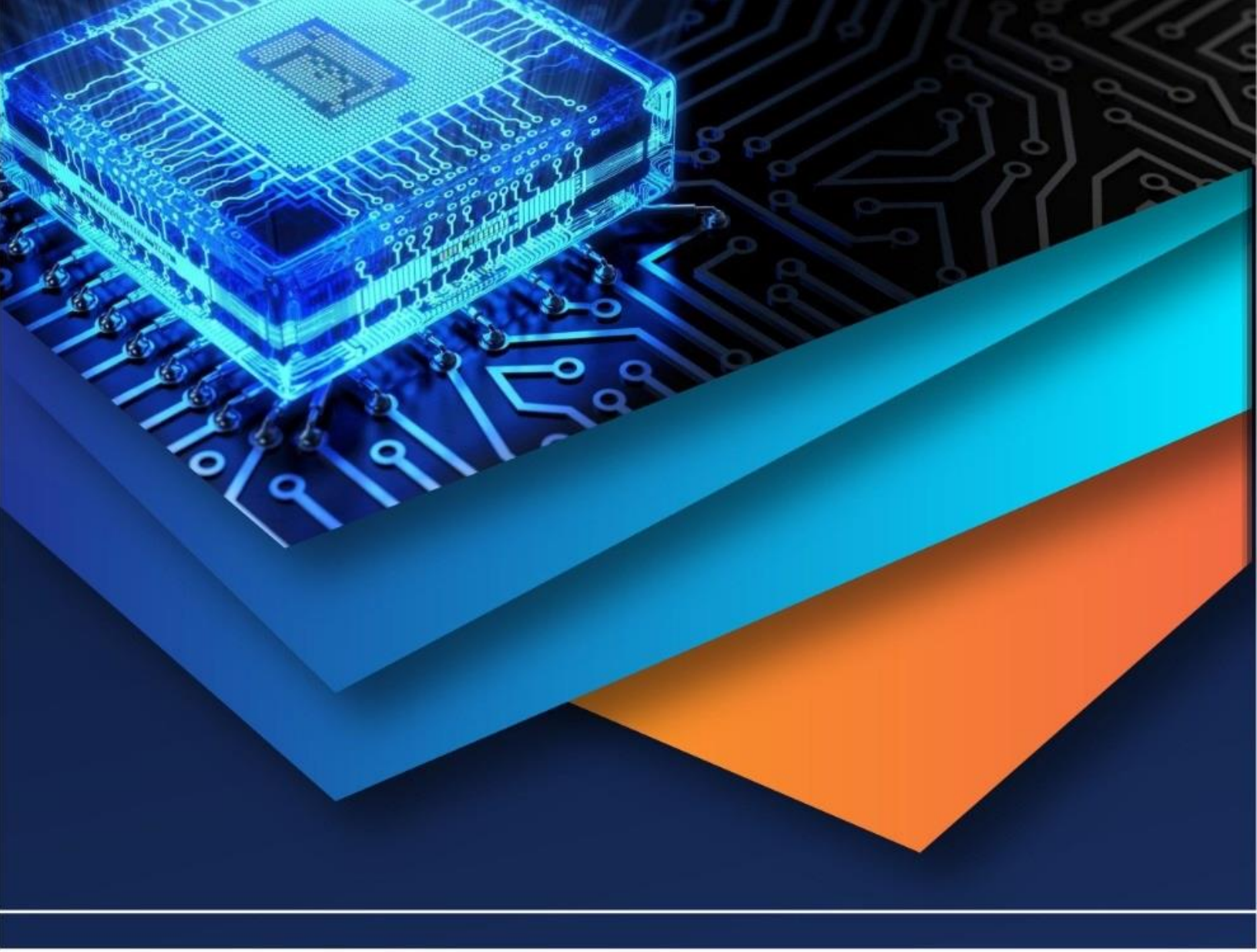

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