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Design and Implementation of LMS and DLMS Adaptive Filter and its Performance Analysis based on FPGA

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Abstract: ***The hardware implementation of adaptive filters is a challenging issue in real-time practical noise cancellation, echo cancellation, prediction and system identification applications. An adaptive filter is a kind of filter that changes and updates its specifications according to the application automatically and does not need user intervention to do the changes. A digital filter takes a digital input, gives a digital output, and consists of digital components. An adaptive filter consists of two blocks. The first block named Filter can be a FIR or IIR digital filter. Nowadays FIR filters are more common, because they are less complicated and more stable. The second block is Weight Adaptation that updates filter block weights according to adaptation algorithm to decrease error signal and achieve filter model. In our project we are considering adaptive least mean square (LMS) filter and self-correcting adaptive filter called as delayed least mean square (DLMS)algorithm architectures.***
The objective of our project is to present implementation of least mean square (LMS) and Delayed least mean square (DLMS) architectures on a Field Programmable Gate Arrays (FPGA) chip. The performance of both approaches is compared in terms of convergence speed, hardware utilization and maximum frequency. The architecture of filter is considered for designing and the VHDL hardware description language is used for algorithm modeling. Modelsim software is used for simulation and Xilinx 13.1 for synthesis and analysis.
Keywords*: MS, DLMS, FPGA, Adaptive filter, Modelsim, VHDL.*

I. INTRODUCTION

In signal processing, a filter is a device or process that removes some unwanted components or features from a signal. Filtering is a class of signal processing, the defining feature of filters being the complete or partial suppression of some aspect of the signal. Most often, this means removing some frequencies or frequency bands. However, filters do not exclusively act in the frequency domain; especially in the field of image processing many other targets for filtering exist. One of the most important issues for practical signal processing applications such as sound signal processing is removing the noise signals from origin signals to achieve clear signals. In some cases, the noise model is time varying and could not be removed by stationary- coefficient based filters. To overcome this problem, the adaptive filters are employed that could adapt their coefficients by changing the filter inputs and processing environment conditions and parameters. An adaptive filter is one which can automatically design itself and can detect system variation in time. Adaptive filters may contain FIR or IIR filters with respect to their impulse response, which can be either finite or infinite. Finite impulse response (FIR) filters are digital filters whose response to a unit impulse (unit sample function) is finite in duration. This is in contrast to infinite impulse response (IIR) filters whose response to a unit impulse (unit sample function) is infinite in duration. FIR and IIR filters each have advantages and disadvantages, and neither is best in all situations.

Adaptive digital FIR filters are widely employed in practical real-time digital signal processing, communication and networks applications. They utilize different training techniques for updating the filter weights in dynamic environments. The LMS algorithm is a well-known adaptive algorithm for updating filter coefficients in dynamic and unknown environments. . The DLMS algorithm is a pipelined representation of LMS algorithm which uses some registers along the filter and error feedback path. The objective of our project is to present implementation of least mean square (LMS) and Delayed least mean square (DLMS) architectures on a Field Programmable Gate Arrays (FPGA) chip. The aim of this paper is to model the adaptive LMS and DLMS adaptive filters by VHDL and realization of them on FPGA.

II. LITERATURE REVIEW

Vella, and Debono [1] illustrated an LMS adaptive filter in a line echo cancellation scheme and different architectures were used to implement multiplication blocks for decreasing hardware utilization and increasing computation speed. The ever increasing data rates used in communication systems bring along the need for faster adaptive filtering systems that are capable of handling the echo tail generated. The two main requirements were kept in mind that were, i) robust and stable algorithms to ensure efficient functionality under these conditions and ii) more processing power. This paper describes the implementation of such an adaptive filter on a Xilinx Spartan 3 FPGA.

Pramod K. Meher and Meghamaheswari [2] In their paper, they have presented a modified delayed least means square (DLMS) adaptive algorithm to achieve lower adaptation-delay. They have proposed an efficient pipelined architecture for the implementation of this adaptive filter. They have shown that the proposed DLMS adaptive filter can be implemented by a pipelined inner-product computation unit for calculation of feedback error, and pipelined weight-update units consisting of N parallel multiply accumulators, for filter order N.

Elhossini et al [3] has proposed three different architectures for implementing a least mean square (LMS) adaptive filtering algorithm, using a 16 bit fixed-point arithmetic representation. These architectures were implemented using the Xilinx multimedia board as an audio processing system. The Virtex-II FPGA chip is used to implement the three architectures. A comparison is then made between the three alternative architectures with different filter lengths for performance and area. Results obtained showed an improvement by 90% in the critical part of the algorithm when used to perform it over a pure software implementation. The results was a total speed up 3.86 times. They had also showed that using a pure hardware implementation results in a much higher performance with somewhat lower flexibility.

Fohl and Matthies [4] implemented an adaptive filter on FPGA to investigate the applicability of this chip as a hardware base for real-time audio processing and they concluded that the FPGA is so suited for complex real-time audio processing. A 64-tap 9-bit LMS adaptive FIR filter for active noise control (ANC) was implemented on Altera Cyclone II FPGA considering a 24 KHZ uniform random noise signal.

Kim and Poularikas [5] in their paper developed classic ANC, variable step size ANC and SCAF ANC for removing noise in speech signals and compared those schemes according to their performance and computation complexity. In the paper, an adjusted step size LMS (least mean squares) algorithm is proposed for possible improvements in the performance of adaptive FIR filters in non stationary environments. Nonstationary signals means that the statistical properties of the noise changes in time such as the high frequency channel time variations. They have proposed two methods to improve the adaptive filtering characteristics. One of the proposed methods is based on the signal to noise ratio value for adjusting the adaptive step size parameter. The other method is based on a self-correcting approach for a fast processing time.

T.J. Milna, S.K Mythili [6] has done survey on DLMS Adaptive Filter With Low Delay. This paper present an efficient architecture for implementation of a delayed least mean square adaptive filter. It is concluded that the partial product generator (PPG) architecture is the best for implementation of low power adaptive filter.

III.PROPOSED WORK

In many practical scenarios it is observed that we are required to filter a signal whose exact frequency response is not known. A solution to such problem is an adaptive filter. An adaptive filter is one which can automatically design itself and can detect system variation in time. An adaptive filter is a computational device that attempts to model the relationship between two signals in real time in an iterative manner. The theory of widely used algorithm named as least mean square (LMS) algorithm was developed by widrow and Hoff in1960. A significant feature of the LMS algorithm is its simplicity. It does not require matrix inversion nor pertinent correlation function. The simplicity of LMS algorithm made it the standard against other linear adaptive filtering algorithm. The LMS algorithm is a linear adaptive filtering algorithm which consists of two processes. A filtering process, which involves firstly computing the output of filter in response to input signal and secondly generating an estimation error by comparing this output with desired response. Figure below shows general adaptive filter. An adaptive process, which involves the automatic adjustment of parameters of filter in accordance with estimation error.

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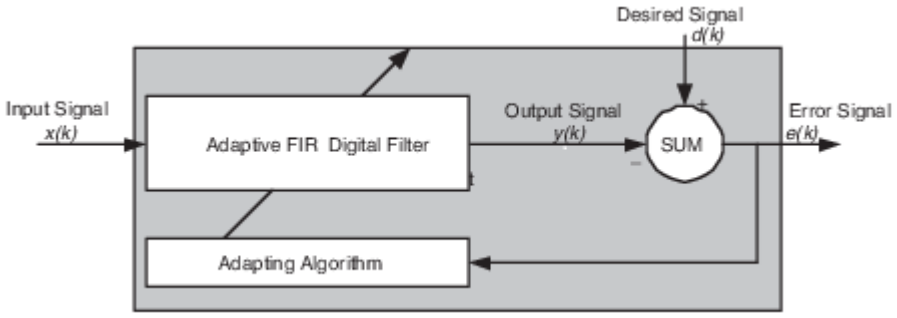

Fig. 1 General adaptive filter

In filtering process the filter may be FIR or IIR, FIR filters are commonly used as they used forward paths only and are stable. This adaptive weight control mechanism may be different algorithms such as LMS, DLMS, RLS, NLMS which are used for error minimization. LMS algorithm is a least mean square algorithm used among different algorithms due to its simplicity, low computational processing tasks and high robustness.

The combination of these two processes forms a feedback loop. First we have transversal filter around which LMS algorithm is built, responsible for filtering process and we have adaptive control process on tap weights of filter thus called as adaptive weight control mechanism.

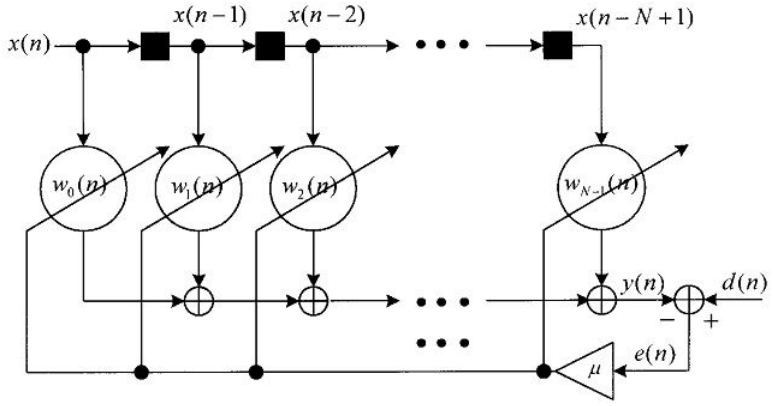

Fig. 2 LMS adaptive filter

Details of LMS adaptive filter are presented in fig 2. The tap inputs x(n),x(n-1).....x(n-N+1) form the elements of N-by-1 tap input vector x(n) where (N-1) is the no. of delay elements. The tap weights w0 (n),w1(n), ...wN-1(n) form the elements of N-by-1 tap weight vector w(n). During filtering process, the desired response d(n) is supplied for processing alongside the tap input vector x(n). Given this input, the transversal filter produces an output y(n) used as an estimate of desired response d(n).

Accordingly following equations are defined,

Filter output:

$$y(n) = w(n)\, x(n) \text{ .....(1)}$$

Estimation error:

$$e(n) = d(n) - y(n) \text{ .....(2)}$$

In adaptive weight control mechanism a scalar version of inner product of estimation error e(n) and tap input x(n-k) for k= 0, 1, 2,……., N-2, N-1; is processed. The result so obtained defines correction applied to tap weight wk(n) at iteration (n+1). The scaling factor used in this computation is denoted by positive quantity 'μ' called as step size parameter. Step size (μ) plays an important role in deciding the error and then weights. But there is a bound on this step size which is denoted as

$$0 < \mu < 2/MSmax \text{ ……..(3)}$$

Where,

Smax is the value of power spectral density of tap input x(n) and M is the filter length.

Tap weight adaptation:

$$w(n+1)=w(n) + \mu x(n)e(n) \ldots\ldots\ldots\ldots\ldots\ldots(4)$$

If we observe, that LMS algorithm requires only 2M+1 multiplications & 2M additions per iterations, where M is the number of tap weights. This is repeated and the new weights minimize the error signal. In other words the computational complexity of LMS algorithm is less than the steepest descent algorithm which is time consuming.

DLMS is a delayed least mean square algorithm which has a pipelined architecture. In the conventional LMS adaptive filter, the estimated signal in each data interval is computed and subtracted from the desire signal. The error is then used to update the tap coefficients before the next sample arrives. The DLMS algorithm is similar to the LMS algorithm, except that in case of DLMS algorithm, the weight increment terms to be used in the current iteration are estimated from the error value and input samples corresponding to a past iteration. Figure 3 shows the structure of conventional DLMS algorithm.

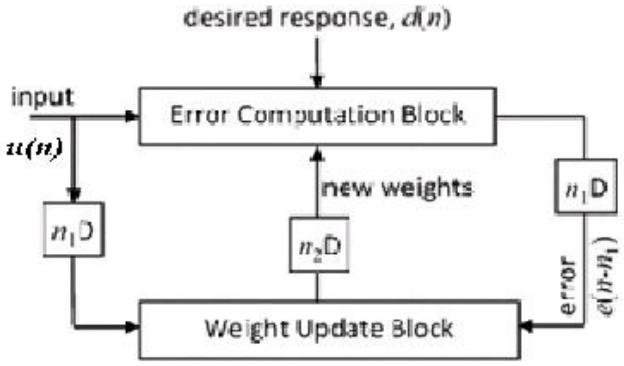

Fig 3 DLMS adaptive filter

From the figure 3 it is clear that the error signal is delayed by n1 number of cycles and then given to weight update block. Same amount of delay is provided to the input signal. In the weight update block these signals are utilized according to the equation 6.

The weight update equation algorithm is given by,

$$w(n + 1) = w(n) + \mu\, u(n - D)\, e(n - D) \ldots\ldots\ldots\ldots\ldots(5)$$

Then further n2 number of cycles delay is given and then this output is distributed to FIR filter in terms of new weights.

IV. RESULTS AND DESCRIPTION

A LMS and DLMS adaptive filter is designed and compared with respect to performance parameters in this paper. These filters are designed and simulated using Modelsim simulator. Figure 4 and 5 shows the simulation result of LMS adaptive filter. The value of error which is to be minimized is observed with the help of waveform as per input value given to it. The design is also verified. Simulation results are provided within the paper. This design is synthesized and analysed with the help of Xilinx ISE 13.1 design suite for both LMS and DLMS adaptive filters. The performance parameters are observed and compared in tabulated form as under.

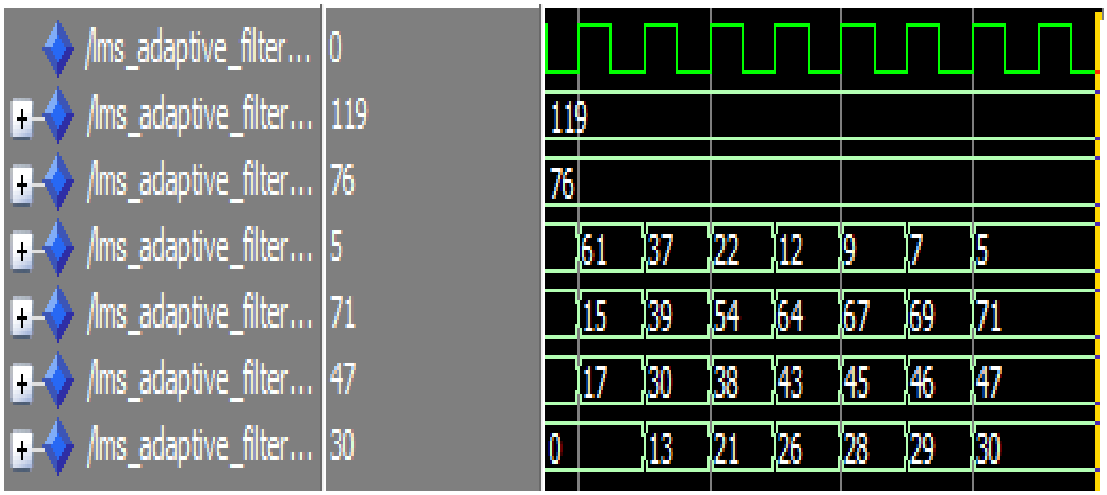

Fig 4 Simulation result of LMS Adaptive filter for $x_{in=119}$ and $d_{in=76}$.

The simulation result of the DLMS adaptive filter is same as that of LMS adaptive filter which is shown in 5 below.

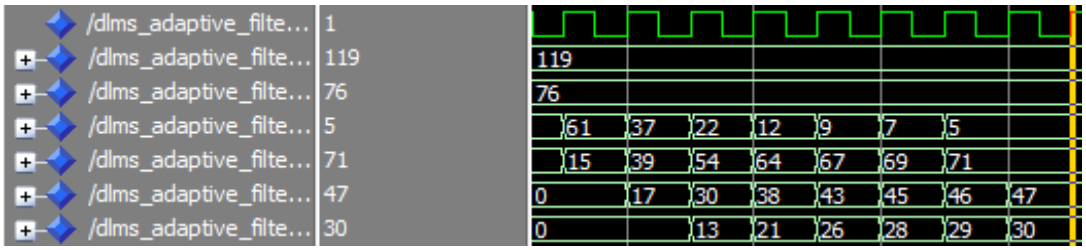

Fig 5 Simulation result of DLMS Adaptive filter for $x_{in=119}$ and $d_{in=76}$.

Synthesis and analysis of LMS and DLMS adaptive filters are done using Xilinx 13.1 design module and following comparison results are obtained

TABLE I
COMPARISON OF LMS AND DLMS ADAPTIVE FILTERS

PARAMETERS	LMS	DLMS
Number of slice registers	24	40
Number of slice LUT's	30	26
Number of occupied slices	8	13
Number of LUT flip-flop pairs used	30	50
Propagation delay	18.908 ns	17.454 ns
Maximum frequency	0.0528 GHz	0.0572 GHz
Throughput	422.40 Mbps	457.60 Mbps

V. CONCLUSIONS

The implementation of least mean square (LMS) and self-correcting adaptive filter (SCAF) i.e Delayed least mean square (DLMS) architectures on a Field Programmable Gate Arrays (FPGA) chip is proposed. Thus, the comparison of the behavior of algorithms in terms of Hardware utilization, convergence speed and the frequency is carried out.

The direct FIR architecture is considered for filter designing and the VHDL hardware description language is used for algorithm modeling. These filters are designed and simulated using Modelsim simulator. This design is synthesized and analyzed with the help of Xilinx ISE 13.1 design suite for both LMS and DLMS adaptive filters.

The results demonstrates that the DLMS FIR filter is faster that LMS FIR filter which comes from the pipeline architecture and is showing improved behavior of performance parameters.

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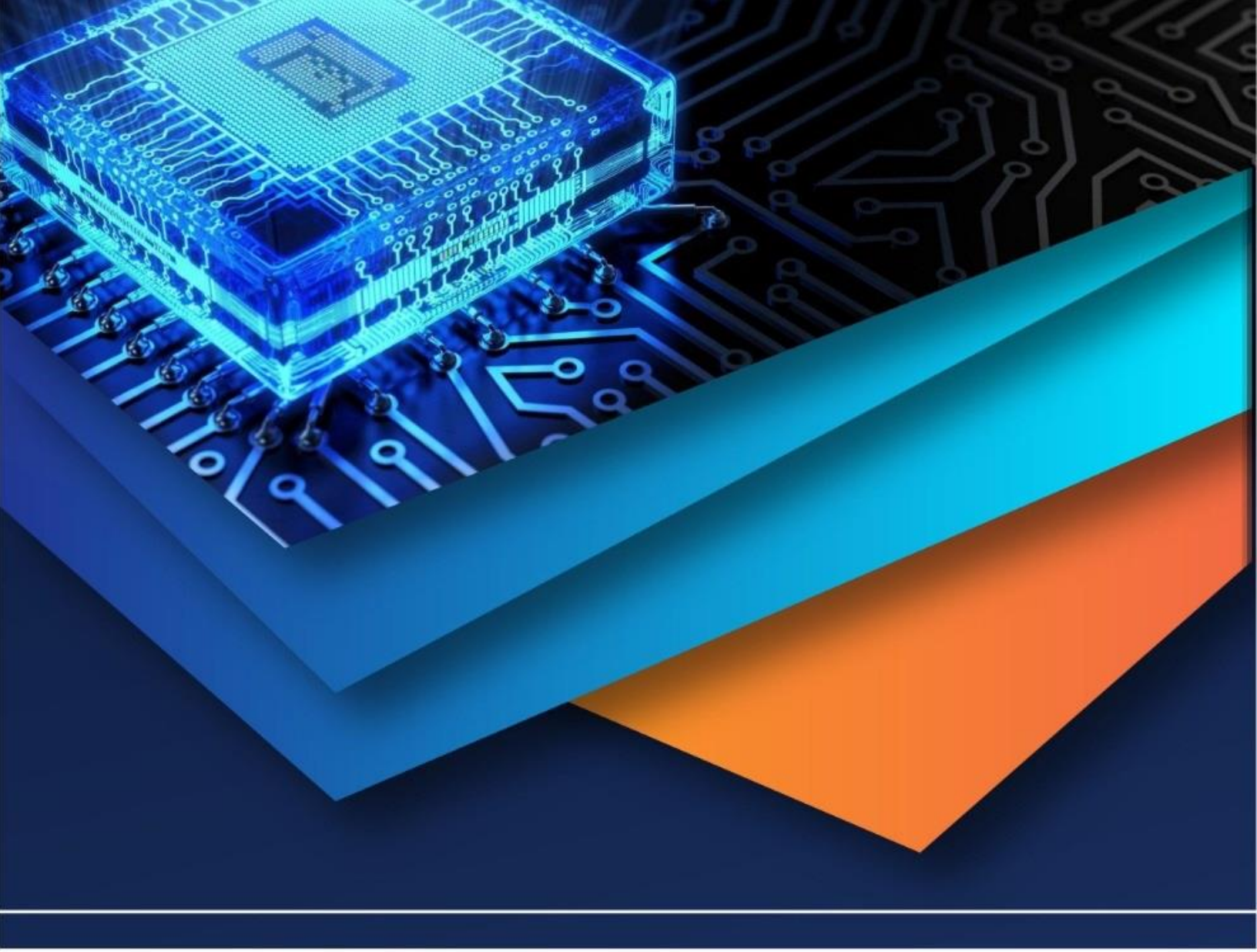

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