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An Application of Multi-Interaction Cellular Neural Network on the Basis of STM32 and FPGA

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This paper presents Multi-Interaction Cellular Neural Network applied on the Basis of STM32 and FPGA[2][3][4][6]. It is for digital image processing with high-order interaction of cells in the network in order to access and interlaced processing and pixel compensation from neighboring cameras according to the matrix given in this article which has a 3x3 ratio corresponding to a combination of 9 cameras[1][5]. It is designed in relation to the cellular neural network to signaling image to the FPGA and then processed before being sent to STM32 to output to LCD, computer or wireless environment. This paper also presents an overview of high-order interaction celluar neural networks, STMs and FPGAs in image processing.
Keywords: MiCNNs, HoCNN, CFPGA, CSTM, ptit.

I. INTRODUCTION

Nowadays, high-speed digital image processing is used in a wide variety of fields such as robot vision, computer vision, image processing in high-definition television, image processing in automation systems, industry. Network neural network technology is implemented on hardware that uses CMOS, FPGA, SoC, VsoC, optical technology, etc… Processing systems applied technology of cellular neural network are now generally designed with combinational and hybrid architectures such as integrated cellular neural network chip with DSP and optical sensors, or other sensors to receive directly the signal array into the cellular neural network chips. Cells of cellular neural networks are multi-layer, multi-interaction, high-order interaction combined directly with sensors. This structure is similar to the biological structure of the retina in mammals.Cellular Neural Networks in image processing work in parallel on both hardware and software. Hardware-based operations for high-speed image processing includes both input and output. Image signals can be captured from a high-resolution CMOS sensor or from a processor-specific sensor designed as a mammalian retina with a large number of cellular processors. When the array size is larger than that of the processor, it is proposed to use the Tilling technique to divide into smaller arrays that handle sub arrays, and then multiply. The processing in DSPs is serial sequential processing. Neural network processors can operate in standalone mode, boot from programs in EEPROM or work with digital computers over Ethernet, Wifi, optical fiber, etc...

II. MULTI-INTERACTION CELLULAR NEURAL NETWORK

A. The structure of the neural elements of the standard cells

In the cellular neural network (CNN) [1][6] each cell C_{ij} with i is the number of rows, j is the number of columns links with neighboring cells C_{kl} in neighboring N_r (i, j) of radius r (r is a positive integer). Each cell is an input processor v_{uij}, state $v_{xij}(t)$, the output $v_{yij}(t)$. Dynamical equations describe the structure of a cell neural as follows:

$$C\frac{dv_{xij}(t)}{dt} = -\frac{1}{R_x}v_{xij}(t) + \sum_{C(k,l)\in Nr(i,j)} A(i,j;k,l)v_{ykl}(t) + \sum_{C(k,l)\in Nr(i,j)} B(i,j;k,l)v_{ukl} + I \qquad (1)$$

$$1 \le i \le M; 1 \le j \le N$$

Output function (1)

$$v_{yij}(t) = \frac{1}{2}\left(\left|v_{xij}(t)+1\right| - \left|v_{xij}(t)-1\right|\right) \qquad (2)$$

Input signal: $v_{uij} = E_{ij}$

The conditions $\left|v_{xij}(0)\right| \le 1; \left|v_{uij}\right| \le 1$

Other theories A(i, j; k, l)=A(k, l; i, j) and C>0; Rx>0

With $1 \le i, k \le M; \quad 1 \le j, l \le N$

Where M, N is the size of the network [1]

Stability of cellular neural network

Leon O. Chua have proposed Lyapunov function:

$$E(t) = -\frac{1}{2}\sum_{(i,j)}\sum_{(k,l)} A(i,j;k,l)v_{yij}(t)v_{ykl}(t) + \frac{1}{2R_X}\sum_{(i,j)} v_{yij}(t)^2 - \sum_{(i,j)}\sum_{(k,l)} B(i,j;k,l)v_{yij}(t)v_{ukl} - \sum_{(i,j)} Iv_{yij}(t) \quad (3)$$

Conditions and demonstration of the network stability have been referred in [6]

B. The structure of multi-interactive cellular neural network

Multi-interactive cellular neural network is associated with the sum of the controlling links and basic feedback to the sum of the input controlling signal accumulations and the output sum of the feedback signal accumulations at any point (k,l) and (m,n) in the vicinity of the point (i,j).

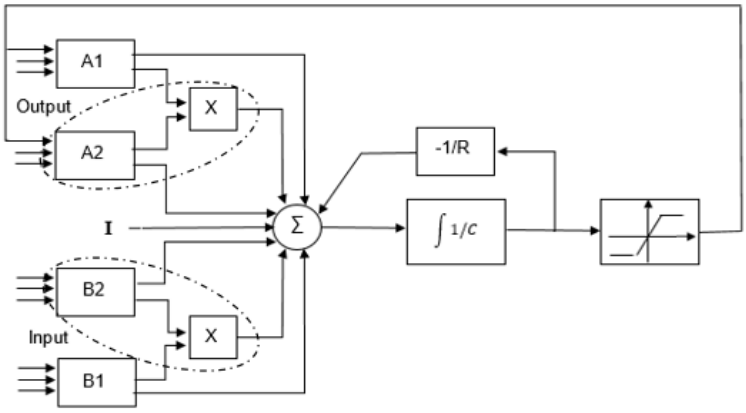

Fig.1 Network block diagram

C_{11} (i-1,j+1)	**C_{12}** (i,j+1)	**C_{13}** (i+1,j+1)
C_{21} (i-1,j)	**C_{22}** (i,j)	**C_{23}** (i+1,j)
C_{31} (i-1,j-1)	**C_{32}** (i,j-1)	**C_{33}** (i+1,j-1)

Fig.2 Cellular Neural Network 3x3

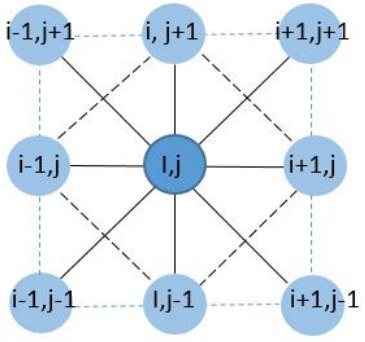

Fig 3. Connections of each neural in the CNN

Multi-interactive cellular neural network is associated with the sum of the controlling links and basic feedback to the sum of the input controlling signal accumulations and the output sum of the feedback signal accumulations at any point (k,l) and (m,n) in the vicinity of the point (i,j). Dynamical equation for multi-interactive cellular neural network as follows:

$$C\frac{dv_{xij}(t)}{dt} = -\frac{1}{R_x}v_{xij}(t) + \sum_{C(k,l)\in Nr(i,j)} A(i,j;k,l)v_{ykl}(t) + \sum_{C(k,l)\in Nr(i,j)} B(i,j;k,l)v_{ukl} +$$
$$+ \sum_{C(k,l),C(m,n)\in Nr(i,j)} A(i,j;k,l,m,n)v_{ykl}(t)v_{ymn}(t) + \sum_{C(k,l),C(m,n)\in Nr(i,j)} B(i,j;k,l;m,n)v_{ukl}v_{umn} + I \quad (4)$$

$$v_{yij}(t) = \frac{1}{2}\left(\left|v_{xij}(t)+1\right| - \left|v_{xij}(t)-1\right|\right) \quad (5)$$

Where: A (i,j, k,l, m,n) and B (i,j, k,l, m,n) is the ratio of the accumulation of the two feedback signals from the output and controls at point respectively (k,l) and (m,n) at point (i,j). The input signals, assumptions and similar binding conditions (1).

1) Stability of output state: The problem in multi-interactive cellular neural network is that the network state must be stable to be able to put in the application?*Consider the largest state*

$$V_{\max} = \max_{(i,j)}\left\{1 + R_x|I| + R_x \sum_{C(k,l)\in Nr(i,j)} \left(\left|A(i,j;k,l)\right|\right) + R_x \sum_{C(k,l),C(m,n)\in Nr(i,j)} \left(\left|A(i,j;k,l;m,n)\right| + \left|B(i,j;k,l;m,n)\right|\right)\right\} \quad (6)$$

It is necessary to prove limited state (stability of output state). Conditions and demonstration of the stability of the network have been referred in [1][5].

III. MULTI-INTERACTION CELLULAR NEURAL NETWORKS ON THE BASIC OF FPGA AND STM32

A. Architectural background of the FPGA

The architecture of the FPGA [2][3] allows a relatively large amount of integration of semiconductor elements into one chip, which is an array of logic blocks. It makes the FPGA be more capable of containing more logic elements, maximizing programmability of logic elements and connection circuit system. FPGA is also equipped with a number of basic arithmetic logic optimizations, high-speed RAM, ROM, kernel, add-ons, etc…

The structure of the FPGA is illustrated

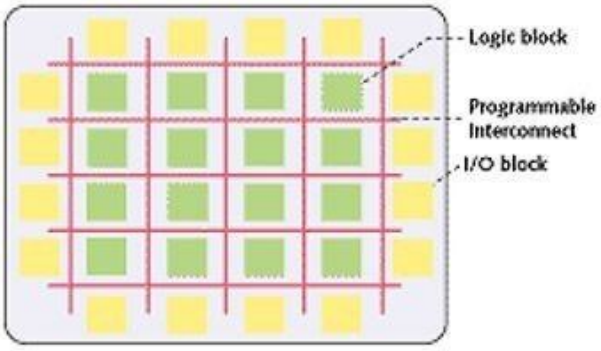

Fig.4 Structure of the FPGA

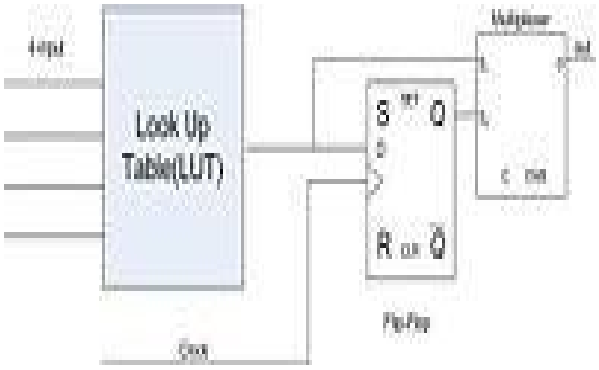

Fig.5 FPGA logic blocks

+ FPGA logic block (Fig.5) The main components of the FPGA are logical blocks. The logical block is composed of a LUT and a flip-flop synchronous memory element. LUT (Look up table) is a logical block that can perform any logical function from 4 inputs, the result of which depends on the purpose to send out the logic block directly or through the flip-flop memory element. From the overall structure of the LUT array, in addition to the four inputs mentioned above, it supports two additional inputs from the logic blocks distributed before and after it raising the total input of the LUT to 6 feet. This structure speeds up logical arithmetic. Interconnected circuit is FPGA's switching network. The interconnected network in the FPGA is composed of vertical and horizontal line connections, depending on the type of FPGA that the links are divided into different groups. For example, the Xilinx's XC4000 has three types of connections: short, long and very long. Links are connected through a programmable switch. The switch containing a number of programmable switching nodes is guaranteed for different types of hyperlinks.

Built-in elements In addition to the logic blocks according to the different types of FPGAs, there are additional built-in components, for example, for designing SoC applications, in the Xilinx Virtex 4.5 series that include the PowerPC processing core, or in Atmel FPSLIC integrated ARV ..., or for digital signal processing applications in FPGAs integrated DSP Slide. It is a high speed multiplier, implementing A * B + C function, for example the Xilinx Virtex line contains from a few dozen to hundreds of DSP slices with 18-bit A, B and C.

Design Description:

When building an FPGA chip for an application in image processing, it will require the IC designer to make the most of these applications. The first step of the design process is to take over the requirements of the design and build the overall architecture of the design.

In this step, the design requirements and the capabilities of the existing technology for the overall architecture design must be described.

+ The blocks should be designed
+ Functions of each block
+ Activities of the design and of each block
+ Technical analysis used in design and tools, software support design.

A design can be described using hardware description language, such as VHDL or Verilog HDL, or can be described via schematic. A design can both include circuit diagrams describing common block diagrams, and can use HDL to describe in detail the blocks in the diagram.

Functional Simulation: After the design description is the overall simulation of functional design to test the design and see if it works properly with the proposed function.

Synthesis of logic: Synthesis of logic is the process of synthesizing the design description into schematic layout circuit. The process divides into the following: converting the RTL code, HDL code into a description in the form of Boolean algebraic expressions and based on these expressions in conjunction with the available standard cell library to synthesize an optimal design.

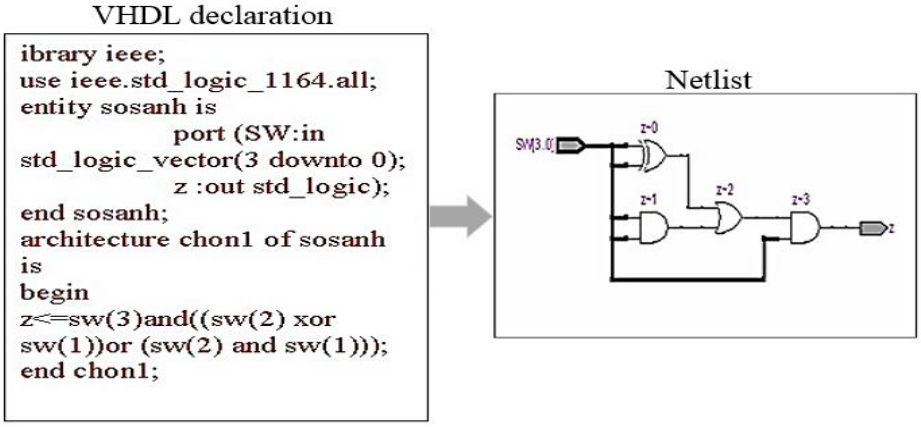

Fig.6 Logic Synthesis

Edit the connection: Use the time analysis tool to analyze the netlist and time constraints. This analysis tool will separate the connections of the design, calculate the delay time of the connection based on the constraints. Based on the analytical report of the analysis tool, identify unsatisfactory connections in time. Depending on the cause of the dissatisfaction, one can rewrite the code and proceed to synthesize the logic or revise the constraints.

B. Image processing on STM32

An image processing on STM[6], image capture and processing system using microcontrollers has a block diagram as follows:

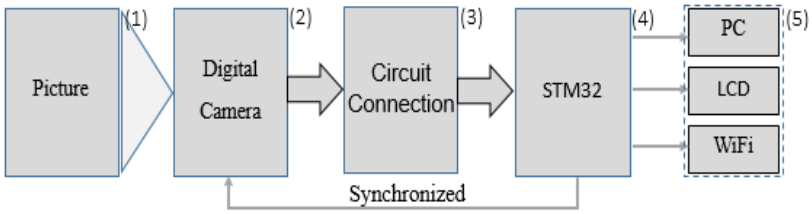

Fig.7 Block diagram of the image processing system

Digital camera is a sensor that converts pixel (color or gray) into data words. Variable speeds should be fast enough to meet real-time processing requirements.

Patching: Compatibility between camera and microcontroller. N Microcontrollers have the primary task of synchronizing the signals (VSYNC and HYSNC) for the camera, collecting image data into the on-screen cache (or transmitting information channels. For ART port for PC, Wifi-TCP / IP channel, etc.).Screen is responsible for displaying pictures. If it is streaming video can test for the high speed.

The STM32 is a microcontroller produced by ST Microelectronic based on the ARM Cortex®-M processor core. It is a 32-bit microcontroller family of processors combining high performance, real-time processing, digital signal processing, low power consumption, low-voltage operation, Maintain complete integration and ease of application development.

C. Application of HoMTCNNs on the basis of FPGA and STM

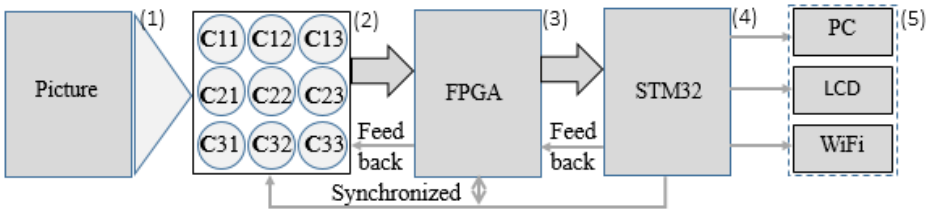

Fig.8 Block diagram for image processing system on the basis of FPGF and STM32

As shown in Figure 8, we have block 1 as the input image signal of the system. Block 2 is a set of CMOS cameras that are set up in the structure of a 3x3 camera cellular neural network. These cameras receive the image signal sent to the FPGA (block 3), the processor is set up in terms of the structure of the high-order multi-interaction neuronal network shown in (4)

$$C\frac{dv_{xij}(t)}{dt} = -\frac{1}{R_x}v_{xij}(t) + \sum_{C(k,l)\in Nr(i,j)} A(i,j;k,l)v_{ykl}(t) + \sum_{C(k,l)\in Nr(i,j)} B(i,j;k,l)v_{ukl} + \sum_{C(k,l),C(m,n)\in Nr(i,j)} A(i,j;k,l,m,n)v_{ykl}(t)v_{ymn}(t) + \sum_{C(k,l),C(m,n)\in Nr(i,j)} B(i,j;k,l;m,n)v_{ukl}v_{umn} + I$$

This block is responsible for signaling the greatest impact from nearby signals, and then image data will be rearranged and put into temporary memory before being sent to the STM32 processor (block 4). At block 4, the STM32 receives image data sent from the FPGA to and synchronizes the signal before it is sent to the output device such as a computer for storage or processing for other jobs via optical coupling or transmission to the display to view processed images or to broadcast Wifi signals to pair with other devices such as actuators, storage (block 5), etc.

IV. CONCLUSION

The paper presents an application of high-order multi-interaction neural network in FPGA-based image processing in conjunction with STM32 based on the application of multidimensional effects of each centred cell to the neighboring cells, also known as the direct effect of ½ (50%) and ¼ (25%) [6] to compensate for the corresponding color ratios in the neighboring and neighboring regions as shown in equation (3) and Fig 8. The application is being implemented in Lab center, Posts and Telecommunications Institute of Technology and Vietnam Research Institute of Electronics, Informatics and Automation.

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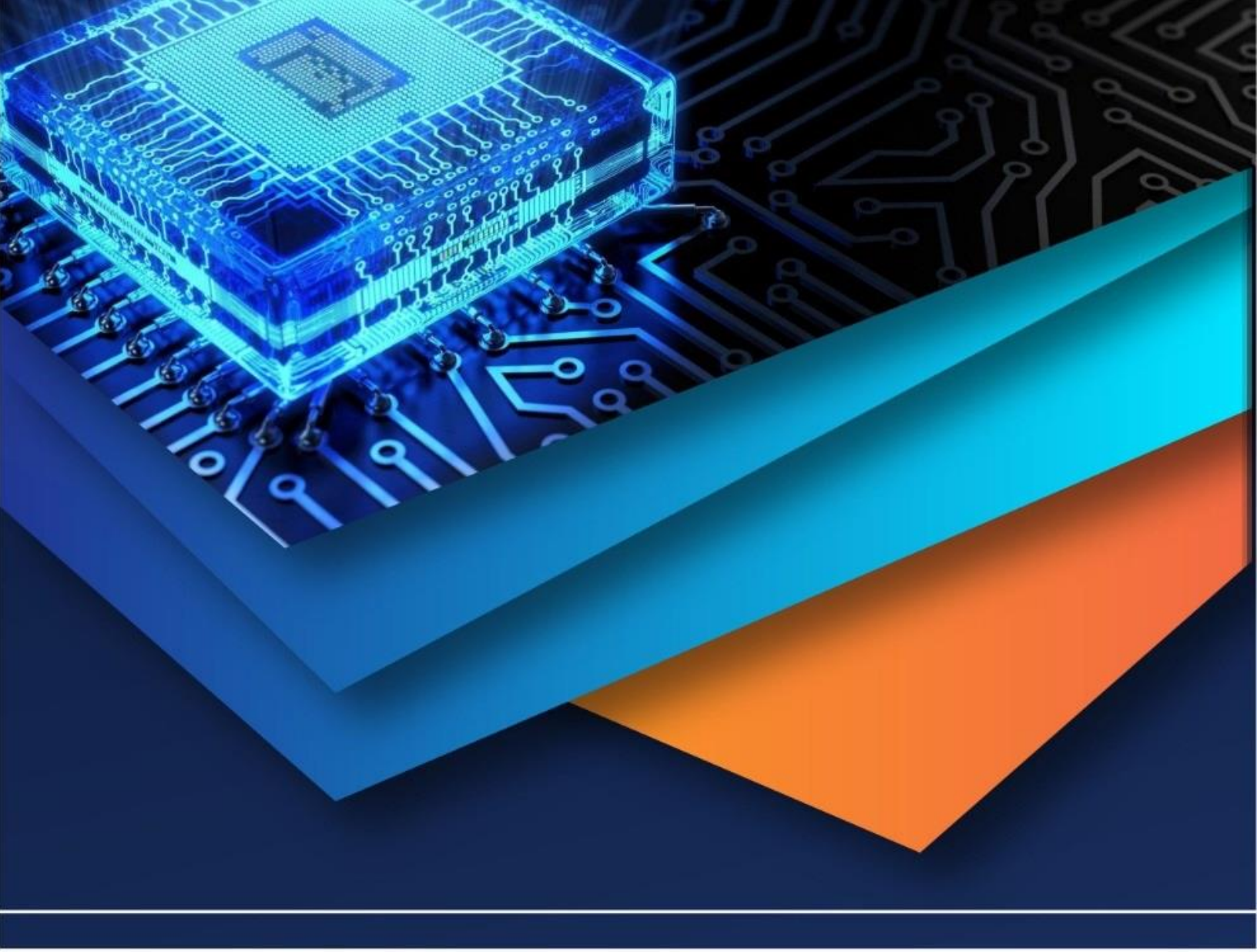

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