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Improvement of Power Quality using DVR

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Abstract: The proposed controller supplements the voltage-sag compensation control of the DVR. It does not require phase-locked loop and independently controls the magnitude and phase angle of the injected voltage for each phase. Fast least error squares digital filters are used to estimate the magnitude and phase of the measured voltages and effectively reduce the impacts of noise, harmonics, and disturbances on the estimated phasor parameters, and this enables effective fault current interrupting even under arcing fault conditions. The results of the simulation studies performed in the MATLAB/SIMULINK R2009a software environment indicate that the proposed control scheme: 1) can limit the fault current to less than the nominal load current and restore the point of common coupling voltage within 10 ms; 2) can interrupt the fault current in less than two cycles; 3) limits the dc-link voltage rise and, thus, has no restrictions on the duration of fault current interruption; 4) performs satisfactorily even under arcing fault conditions; and 5) can interrupt the fault current under low dc-link voltage conditions.
Keywords: Power Quality, Voltage Harmonics, Voltage Sag, Voltage Swells. DVR, Fault Current Interrupting

I. INTRODUCTION

With rapid developments in the industry, power quality becomes very important. Power quality is defined as any power problem manifested in the voltage, current or frequency deviations that result in failure or mal function of the customer equipment. Power quality issues can be classified as short duration voltage variations, long duration voltage variations, wave form distortions, transients, voltage imbalance and voltage flicker. Among the various power quality issues, voltage sag, voltage swell and harmonics are more dominant in the distribution system. To compensate these problems, Dynamic voltage Restorer (DVR) is used. DVR is a series compensating device to mitigate voltage sag and voltage swell. It is also used as series active filter to mitigate harmonics. Interline Dynamic Voltage Restorer (IDVR) is used to provide an economical solution for compensating voltage sag.

The dynamic voltage restorer (DVR) is a custom power device utilized to counteract voltage sags. It injects controlled three-phase ac voltages in series with the supply voltage, subsequent to voltage sag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle. Fig. 1.1 shows the main components of a (i.e., a series transformer T_S, a voltage- source converter (VSC), a harmonic filter, a dc-side capacitorC_{DC}, and an energy storage device. The line-side harmonic filter consists of the leakage inductance of the series transformer L_f and the filter capacitorC_f.

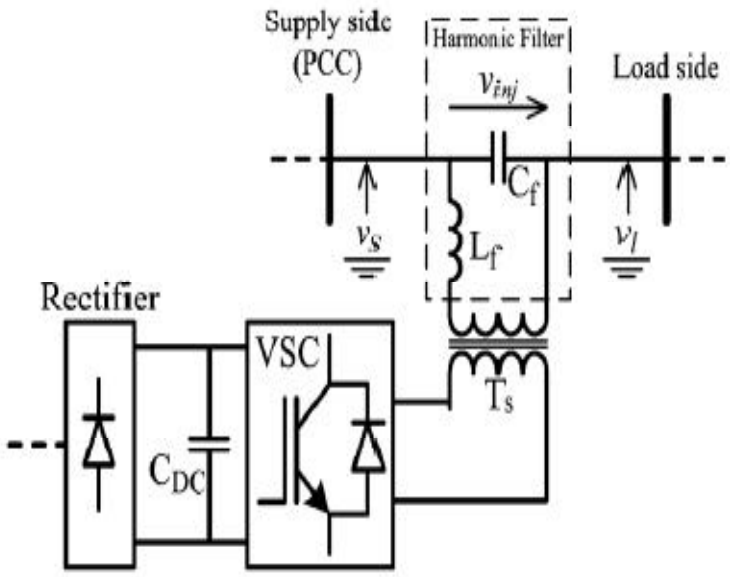
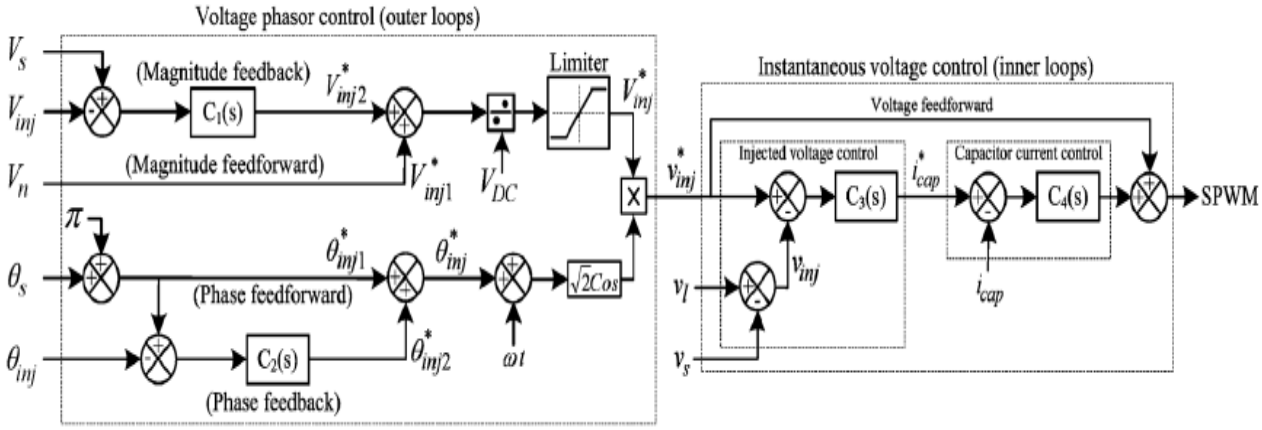


Fig.1.1.Schematic diagram of a DVR

The DVR is conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current. A technically elaborate approach to more efficient utilization of the DVR is to equip it with additional controls and enable it also to limit or interrupt the downstream fault currents. A control approach to enable a DVR to serve as a fault current limiter is provided. The main drawback of this approach is that the dc-link voltage of the DVR increases due to real power absorption during fault current-limiting operation and necessitates a switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault. The dc-link voltage increase can be mitigated at the cost of a slow-decaying dc fault current component using the methods introduced.

To overcome the a fore mentioned limitations, this paper proposes an augmented control strategy for the dvr that provides: 1) voltage-sag compensation under balanced and unbalanced conditions and 2) a fault current interruption (FCI) function. The former function has been presented. It should be noted that limiting the fault current by the DVR disables the main and the backup protection (e.g., the distance and the over current relays). This can result in prolonging the fault duration. Thus, the DVR is preferred to reduce the fault current to zero and interrupt it and send a trip signal to the upstream relay or the circuit breaker (CB).It should be noted that the fault current interruption function requires 100% voltage injection capability. Thus, the power ratings of the series transformer and the VSC would be about three times those of a conventional DVR with about 30%–40% voltage injection capability. This leads to a more expensive DVR system. Economic feasibility of such a DVR system depends on the importance of the sensitive load protected by the DVR and the cost of the DVR itself. The performance of the proposed control scheme is evaluated through various simulation studies in the MATLAB R2009a platform. The study results indicate that the proposed control strategy: 1) limits the fault current to less than the nominal load current and restores the PCC voltage within less than 10 ms, and interrupts the fault current within two cycles; 2) it can be used in four- and three-wired distribution systems, and single-phase configurations; 3) it does not require phase-locked loops; 4) it is not sensitive to noise, harmonics, and disturbances and provides effective fault current interruption even under arcing fault conditions and 5) it can interrupt the downstream fault current under low dc-link voltage conditions.



II. PROPOSED FCI CONTROL STRATEGY

A. Proposed Fault Current Interruption Control Strategy

The adopted DVR converter is comprised of three independent H-bridge VSCs that are connected to a common dc-link capacitor. These VSCs are series connected to the supply grid, each through a single-phase transformer. The proposed FCI control system consists of three independent and identical controller's one for each single-phase VSC of the DVR. Assume the fundamental frequency components of the supply voltage, load voltage, and the injected voltage, Fig. 1 are

$$v_s = V_s \times \cos(\omega t + \theta_s) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 1$$

$$v_l = V_l \times \cos(\omega t + \theta_l) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots 2$$

$$v_{inj} = v_l - v_s = V_{inj} \times \cos(\omega t + \theta_{inj}) \ldots\ldots\ldots\ldots\ldots 3$$

Two identical least error squares (LES) filters are used to estimate the magnitudes and phase angles of the phasors corresponding V_S to V_{inj} (i.e., $\overrightarrow{V_S} = V_S \angle \theta_S$) and (i.e., and $\overrightarrow{V_{inj}} = V_{inj} \angle \theta_{inj}$ respectively in 5 ms).

The fault current interruption function requires a phasor parameter estimator (digital filter) which attenuates the harmonic contents of the measured signal. To attenuate all harmonics, the filter must have a full-cycle data window length which leads to one cycle delay in the DVR response. Thus, a compromise between the voltage injection speed and disturbance attenuation is made. The designed LES filters utilize a data window length of 50 samples at the sampling rate of 10 kHz and, hence, estimate the voltage phasor parameters in 5 ms. Fig. 3 depicts the frequency response of the LES filters and indicates significant attenuation of voltage noise, harmonics, and distortions at frequencies higher than 200 Hz and lower than 50 Hz. Reference demonstrates the effectiveness of this filter in attenuating the noise, harmonics, and distortions for the sag compensation mode of operation as well. The next section shows that this filter also performs satisfactorily in the FCI operation mode, even under arcing fault conditions where the measured voltage and current signals are highly distorted.

Fig. 2 shows a per-phase block diagram of the proposed DVR control system corresponding to the FCI operation mode, where is the nominal rms phase voltage. The control system of Fig. 2 utilizes v_s,v_l , the dc-link voltageV_{DC} , and the harmonic filter capacitor current i_{cap},as the input signals. The reported studies in this paper are based on the over current fault detection method. The fault detection mechanism for each phase is activated when the absolute value of the instantaneous current exceeds twice the rated load current.

The proposed multi loop control system includes an outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control). The inner loop provides damping for the transients caused by the DVR harmonic filter, and improves the dynamic response and stability of the DVR. The inner loop is shared by the sag compensation and the FCI functions. When a downstream fault is detected, the outer loop controls the injected voltage magnitude and phase angle of the faulty phase(s) and reduces the load-side voltage to zero, to interrupt the fault current and restore the PCC voltage. The DVR "outer" voltage phasor control and "inner" instantaneous voltage control, corresponding to each phase, are described in the following two subsections.

B. Voltage Phasor Control System

In the FCI operation mode, the required injected voltage phasor is equal to the source voltage phasor, but in phase opposition [i.e., the injected phasor $\overrightarrow{V_{inj}} = V_{inj}\angle\theta_{inj}$ is controlled to be$V_S\angle(\theta_S + \pi)$]. Performance of the voltage phasor control, in terms of transient response, speed, and steady-state error, is enhanced by independent control of voltage magnitude and phase, and incorporating feed forward signals to the feedback control system. Fig. 2 shows two proportional- integral (PI) controllers (and) that are used to eliminate the steady-state errors of the magnitude and phase of the injected voltage, respectively. Parameters of each controller are determined to achieve a fast response with zero steady-state error.

The output of the phasor control system is a reference phasor denoted by$\overrightarrow{V_{inj}^*} = V_{inj}^*\angle\theta_{inj}^*$. To eliminate the effects of the dc-link voltage variations on the injected voltages, V_{inj}^* is normalized by V_{dc} . The magnitude and the phase angle of $\overrightarrow{V_{inj}^*}$ are independently calculated and the magnitude is passed through a limiter (Fig. 2). The resulting phasor magnitude and phase angle are converted to the sinusoidal signal V_{inj}^*, which is the reference signal for the instantaneous voltage control.

C. Instantaneous Voltage-Control System

Under ideal conditions, a voltage sag can be effectively compensated if the output of the phasor-based controllerV_{inj}^*, is directlyfed to the sinusoidal pulse-width modulation (SPWM) unit. However, resonances of the harmonic filter cannot be eliminated under such conditions. Therefore, to improve the stability and dynamic response of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to attenuate resonances.

The generated reference signal for the injected voltage $V_{inj}^*$is compared with the measured injected voltage V_{inj}, and the error is fed to the voltage controller. As shown in Fig. 2, the output of the voltage controller i_{cap}^* is the reference signal for the filter capacitor current control loop. It is compared with the measured capacitor current i_{cap}, and the error is fed to the current controller.

The steady-state error of the proposed control system is fully eliminated by the PI controllers in the outer control loop (i.e., C_1 and C_2), which track dc signals (magnitude and phase angle). Therefore, there is no need for higher order controllers in the inner control loop which are designed based on sinusoidal references. Thus, in Fig. 2, $C_3$and C_4 are pure gains $k_v$and K_c, respectively.

A large k_v result in amplification of the DVR filter resonance and can adversely impact the system stability. Thus, the transient response of the DVR is enhanced by a feed forward loop, and a small proportional gain is utilized as the voltage controller. A large K_c damps the harmonic filter resonance more effectively, but it is limited by practical considerations (e.g. amplification of capacitor current noise, measurement noise, and dc offset). Therefore, the lowest value of the proportional gain which can effectively damp

the resonances is utilized. The output of the current controller is added to the feed forward voltage to derive the signal for the PWM generator.

III. STUDY MODEL AND RESULT

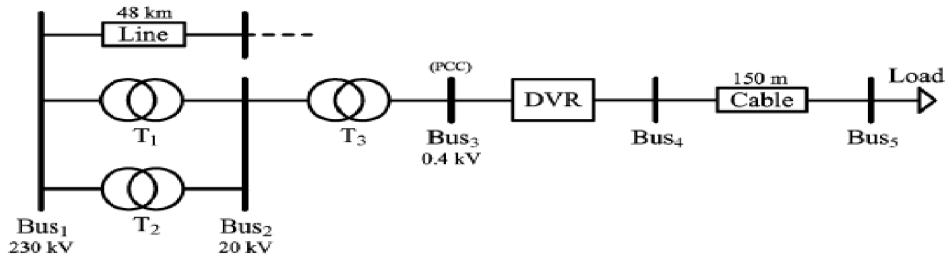


Fig.3.1. Single-line diagram of the system used for simulation studies.

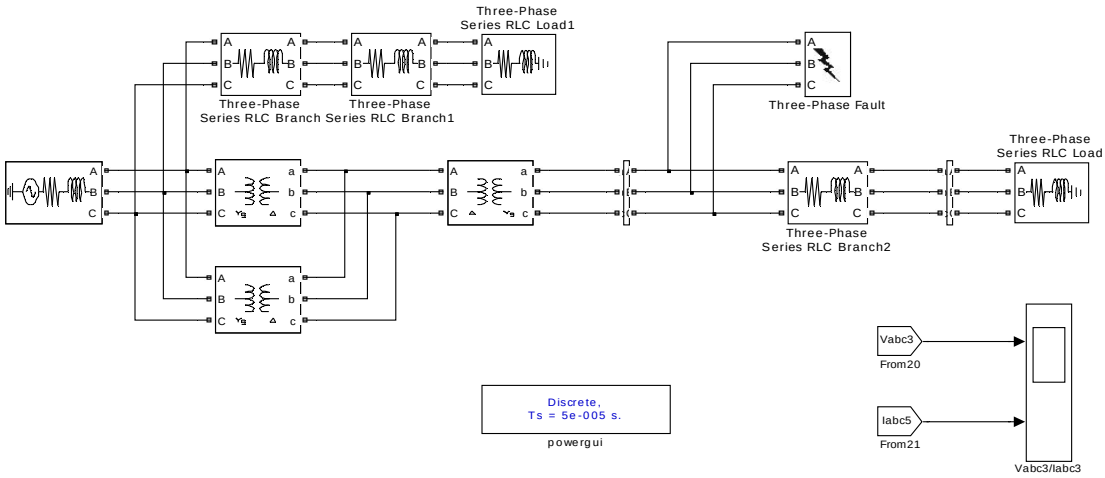


Fig.3.2. Design System for simulation studies

Fig. 3.1 depicts a single-line diagram of a power system which is used to evaluate the performance of the proposed DVR control system under different fault scenarios, in the MATLAB software environment. A 525-kVA DVR system is installed on the 0.4-kV feeder, to protect a 500-kVA, 0.90 lagging power factor load against voltage sags. Parameters of the simulated power system and the DVR are given. In the reported studies, the base voltage for per-unit values is the nominal phase voltage. Besides, voltage and current waveforms of phases A, B, and C are plotted by solid, dashes, and dotted lines, respectively.

A. Single-Phase-to-Ground Downstream Fault

Phase-A of the system of Fig. 6.2 is subjected to a fault with the resistance of 0.2Ω at 10% length of the cable connecting BUS_4 to BUS_5, at t= 20 ms. If the DVR is inactive (Fig. 9), the PCC voltage does not considerably drop and the fault current is about 2.5 p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted by the DVR to prevent possible damages to the VSC before the fault is interrupted by the relays. The reason is that the operation time of the overcurrent relays is considerable for a fault current of about 2.5 p.u.

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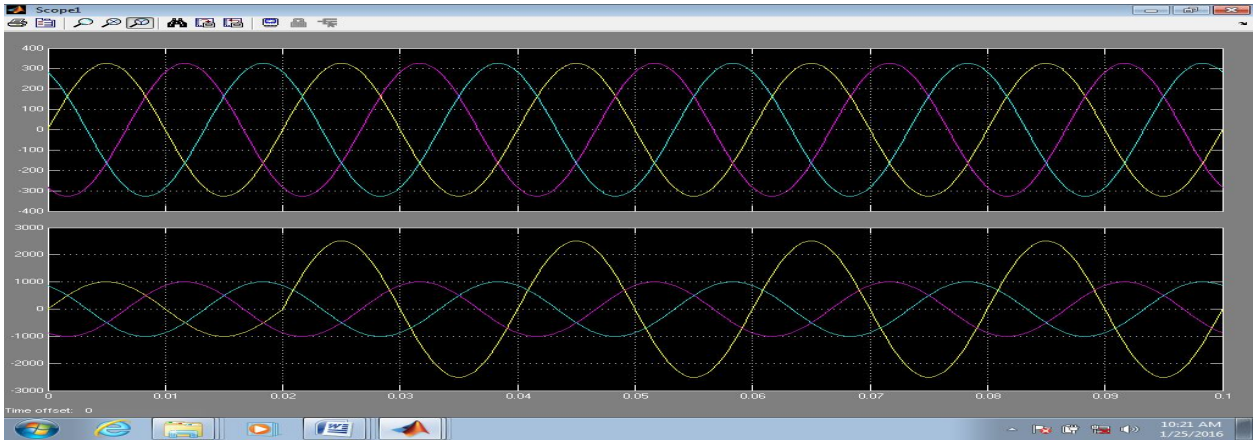
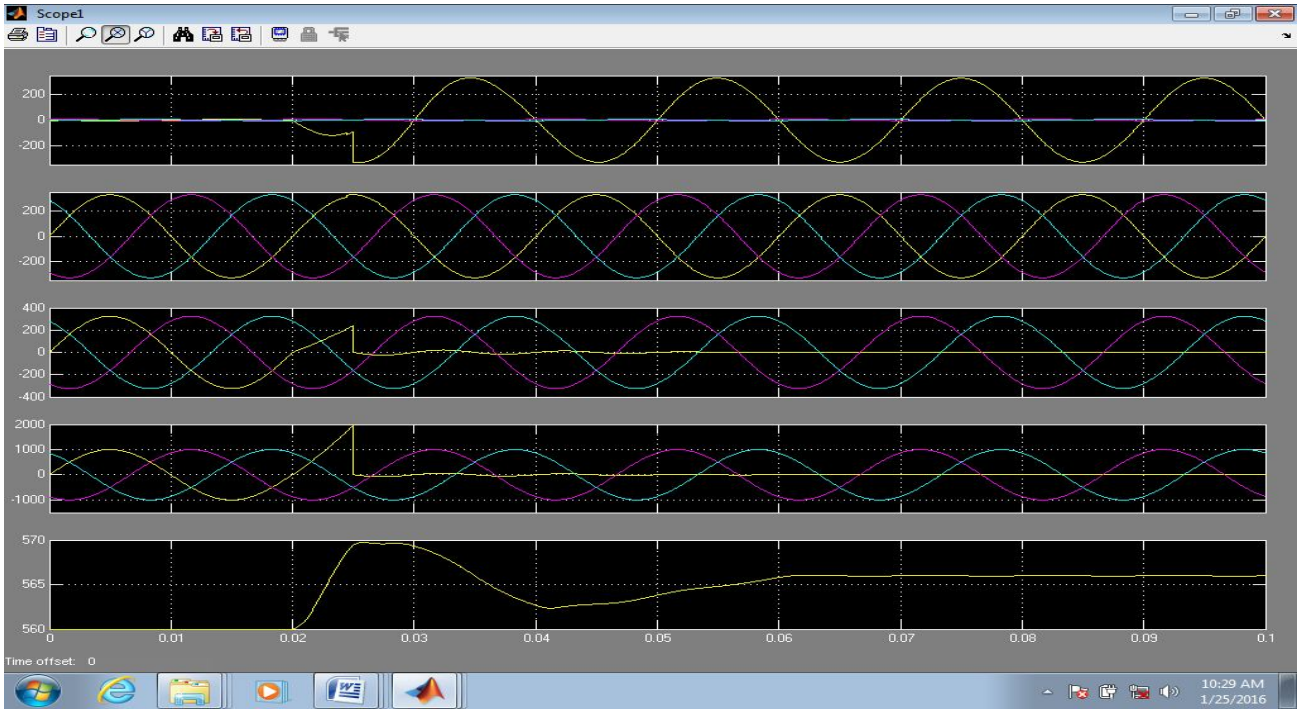


Graph.3.1.(a) Voltages at BUS_3, (b) Fault currents, during downstream phase-to phase fault

Graph 3.1.illustrates that the proposed DVR control strategy successfully interrupts the fault current in the faulty phase in about two cycles. Graph 6.6 shows that the dc-link voltage rises less than 1.8%. Graph 3.2 also shows that only the faulty phase of the DVR reacts to fault current, and the healthy phases are not interrupted.



Graph.3.2.(a) Injected voltages, (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the single phase-to-ground downstream fault.

IV. CONCLUSION

Simulation studies conclude that the dc-link voltage rise caused by the proposed FCI mode of operation is proportional to the fault current, and depends on the type of fault. The results also indicate that the maximum dc-link voltage rise occursunder the most severe three-phase fault which is about 15%, and can be tolerated based on DVR appropriate design. It must be noted that to prevent operation of three-phase induction motors under unbalanced voltage conditions, they must be equipped with protective devices which detect such conditions and disconnect the load when any of the phases is de-energized by the single-phase operation of the FCI function. Furthermore, disabling the single-phase fault current interruption capability can be provided as an operational option and the operator can decide either to use or disable this function depending on the type of load.

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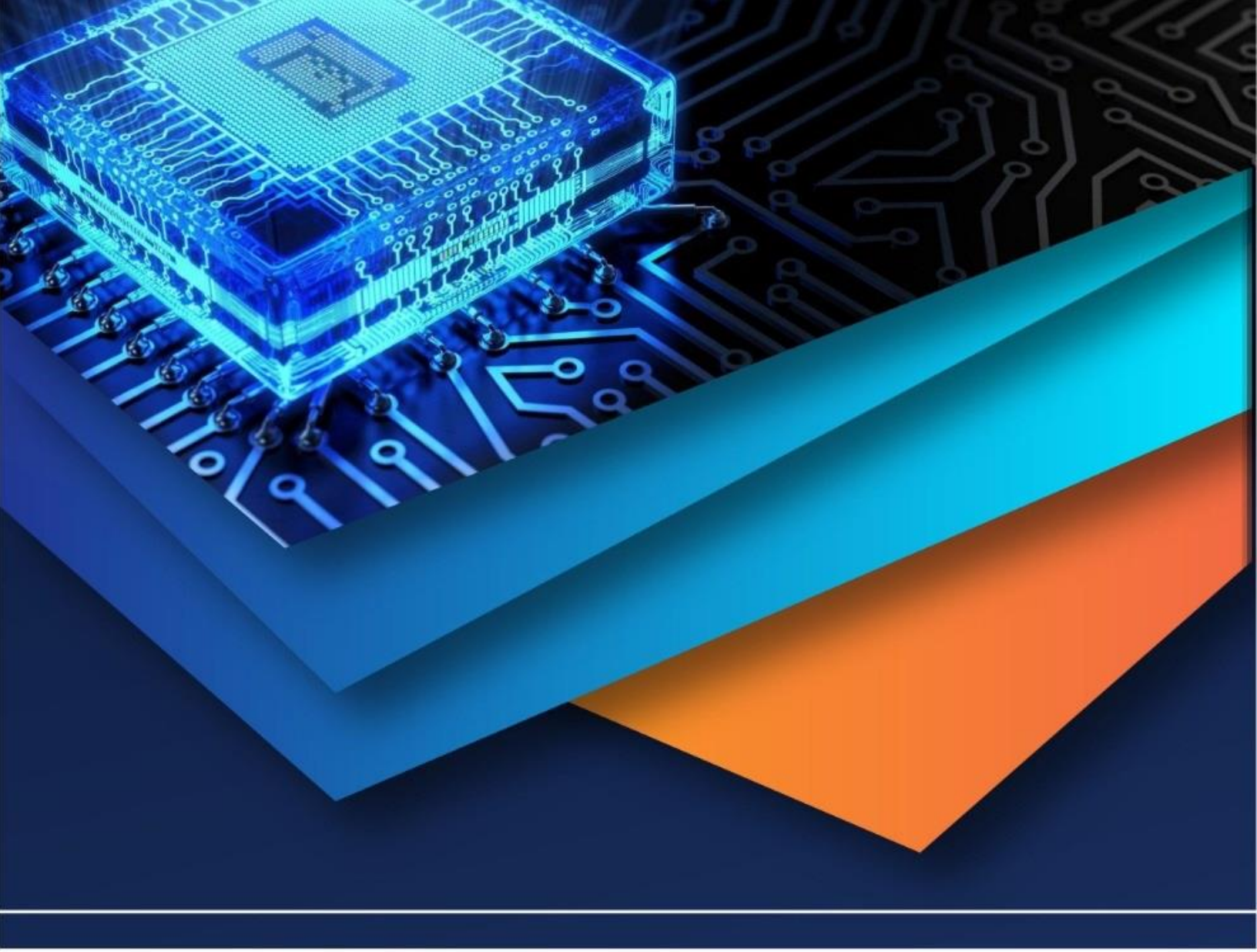

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