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Design of Efficient 32bits BCD Adders in Quantum-Dot Cellular Automata

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Abstract: In the current era of technology the size of the system needs to be reduced in order to make compact as well as portable simultaneously it must process the data at very high speed with less delay. To design such circuits we need new approach to stand with such requirements. In this paper we will present emerging technique of designing which is termed as Quantum-dot Cellular Automata (QCA). QCA is the technology where the significant improvement is possible in order to design more complicated circuits. Here we are suggesting a new approach to design QCA-based 32 bits BCD adder.

Keywords- BCD adders, decimal arithmetic, Quantum Computing, Low Power, majority gates (MG), quantum-dot cellular automata (QCA)

I. INTRODUCTION

Quantum-dot cellular automata (QCA) technology provides a promising opportunity to overcome the limits of conventional CMOS technology [1]–[2]. To designing more complicated circuits in future the QCA is getting recognition by designing engineers. In direction of QCA some arithmetic circuits and logical circuit already had been designed such as adder [3]–[4], multipliers[5]–[7], and comparators [8]–[10]. Autonomously of the performed logic function, nonelementary digital modules are designed intelligently combining inverters and majority gates (MGs), which are the basic fundamental logic gates inherently available within the QCA technology.

Numerical decimal arithmetic has currently received a great deal of attention since several financial, economical, commercial, and Internet-based applications increasingly require higher precision. In these processes, the errors coming from the conversion between decimal and binary number representations could not be acceptable and several recent microprocessors [11]–[12] include hardware decimal arithmetic units in their core based on the IEEE 754–2008 standard [13]. The design of such digital circuits requires proper planning at both logic and layout levels to improve performance and Area.

II. FUNDAMENTALS OF QCA

The most fundamental element of the QCA structure is shown in figure 1. It is the building block of the QCA technology. As we can see in the figure it is having four dots at all its corner. The structure has two free electrons. The structure of the QCA in provided in the figure 1.

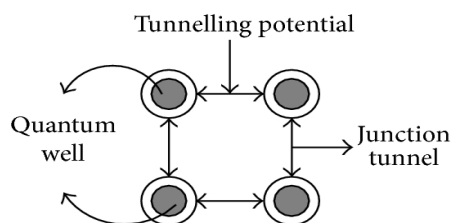


Fig. 1 Structure of a QCA Cell

Because of the coulombic repulsion these two electrons can only be placed in two stable states. The electrons are always resided in diagonally opposite corners of the QCA cell. The diagonally opposite corners are having maximum distance. The stable states also called as polarization. As per the locations of the electrons in the cell two states can be take place. These states are considered as binary states 1 and 0. For the purpose of explanation the figure 2 is shown.

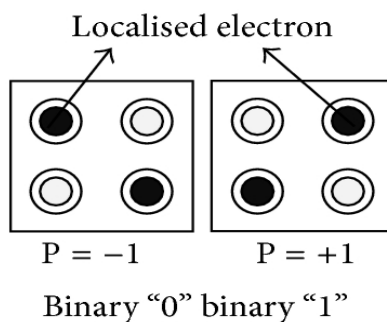


Fig. 2 Fig.2 QCA cell with two polarization

The diagonally opposite electrons interact to each other by the electrostatic forces and due to this force the electrons maintain its polarization. However the QCA cells cannot flow the data intrinsically therefore to get the control over flow of the direction of electrons the four clock zones are associated. These four clock signal have 90° phase difference. The QCA design is partitioned into clock zones. The clock scheme, named the zone clocking scheme, makes the QCA designs different polarizations intrinsically pipelined. Since each clock zone behaves like a D-latch [14]. The latter is provided by means of four clock signals clk_x (with x ranging from 0 to 3), shifted by 90° from each other [1].

The fundamental logic gates available within the QCA technology are the inverter and the majority gate (MG). Given three inputs a , b , and c , the MG performs the logic function reported in equation (1) provided that all input cells are associated with the same clock signal clk_x , whereas the remaining cells of the MG are associated with the clock signal clk_{x+1} .

$M(a, b, c) = a \cdot b + a \cdot c + b \cdot c$. (1) The 1-digit BCD adder earlier proposed in [16]–[17] use the top-level architecture in Fig. 3. In this the inputs are added in the binary format and then perform the conversion of BCD. If the output is greater than the 9 then 6 is added in it, else the addition of 0 is take place.

III. PROPOSED 32BITS BCD ADDERS IN QUANTUM-DOT CELLULAR AUTOMATA

In brief this proposes a unique approach to develop a QCA- based 32 bits BCD adder which can achieve higher computational speed than existing counterparts with occupying less area or count cell. The novel 1-digit decimal adder generates, propagates, and absorbs a carry signal with delay times up to 27%, 45%, and 44% lower than the faster existing counterparts that are those described in [8]. Differently from all previous works, we extended our work to the design of a 32-bits QCA-based BCD adder.

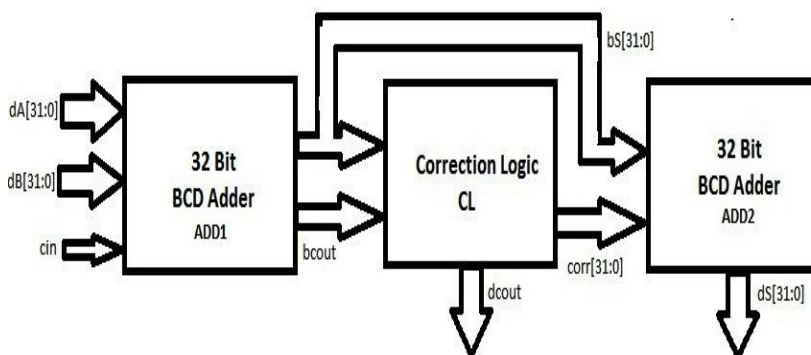


Fig 3. Structure of the 32 bits BCD adder.

The BCD adder here presented follows the traditional top-level structure illustrated in Fig. 3, but it exploits the novel logic expressions demonstrated in the following by Equations 1 and 2.

As the main result, the proposed approach leads to the best trade off between the overall occupied area and the speed performances. To understand the new design strategy, let us examine first the 4 bits binary adder ADD1. 4 bit binary adder ADD1 collects the value of input $dA(3:0)$ and $dB(3:0)$ as well as its carry “cin” and figure out its binary output as $bs(3:0)$ and “bcout”, this whole process it carried out as per the equation (2a) that introduces only one Majority gate(MG) between C_i and C_{i+1} .

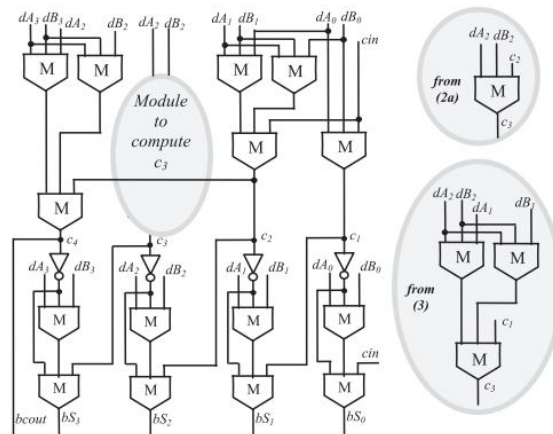


Fig. 4 New ADD1 module.

$$C_{i+1} = M(dA_i, dB_i, C_i) \dots\dots (2a)$$

$$C_{i+2} = M(C_i, M(dA_{i+1}, dB_{i+1}, g_i), M(dA_{i+1}, dB_{i+1}, p_i)) \dots\dots (2b)$$

Consequently, the propagation of C_i through two bit positions would require two cascaded MGs to obtain the carry C_{i+2} . Conversely, as discussed in [19] and given in (2b), by exploiting the auxiliary generate and propagate signals $g_i = dA_i \cdot dB_i$ and $p_i = dA_i + dB_i$, the carry C_{i+2} can be computed by propagating C_i through just one MG. Equation 1 demonstrates a novel way to propagate C_i through two consecutive bit positions that also introduces just one MG between C_i and C_{i+2} but avoiding the computation of g_i and p_i .

As a consequence of Equation 1, the 4-b adder ADD1 can be realized by computing the carries as reported in

$$C_1 = M(dA_0, dB_0, cin)$$

$$C_2 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0$$

$$C_{in} = M(C_{in}, M(dA_1, dB_1, dA_0), M(dA_1, dB_1, dB_0))$$

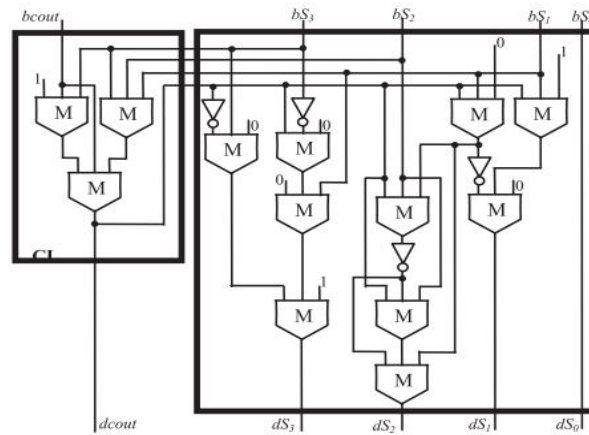


Fig. 5 Module CL and New ADD2 module.

$$C_3 = M(dA_2, dB_2, C_2) \quad C_2 C_4 = bcout = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot C_2$$

$$= M(C_2, M(dA_3, dB_3, dA_2), M(dA_3, dB_3, dB_2)). \quad (4)$$

Finally, the i^{th} bit of the binary sum $bS(3:0)$ is computed by applying the bit sum representation demonstrated in [17] and here given in

$$bS_i = M(C_i, C_{i+1}, M(dA_i, dB_i, C_{i+1})). \quad \dots (5)$$

Fig. 2 shows the QCA circuit purpose-designed for the ADD1 module exploiting the aforementioned described logic. It is worth noting that, to compute C3, both (2a) and (3) could be used. The resulting circuits are depicted in the insets of Fig. 2. The former is actually exploited since propagating C1 instead of C2 would not reduce the overall delay of ADD1. Indeed, using (3) would lead to unnecessary additional MGs.

Due to Equation 1, the novel circuit exhibits a critical computational path of five MGs and one inverter, which is one MG shorter than the conventional Ripple-Carry Adder (RCA) [18]. Moreover, the novel ADD1 module uses only 16 MGs and 4 inverters, thus overcoming also the conventional 4-b CLA [19], which is implemented using 43 MGs and 4 inverters. The decimal carryout *dcout* and the decimal sum *dS(3:0)* are then calculated following the novel approach demonstrated in Equation 2.

Equation 2: If *bcout* and *bS(3:0)* are the binary carry-out and the binary sum computed by adding the BCD digits *dA(3:0)* and *dB(3:0)* then the BCD carry-out *dcout* is given by (6) and the decimal sum *dS(3:0)* is obtained by (7).

$$dcout = M(bcout, M(1, bcout, bS3), M(bS3, bS2, bS1)) \quad \dots (6)$$

$$dS0 = bS0 \quad \dots (7a)$$

$$dS1 = M(\overline{M(0, bS1, dcout)}, M(1, bS1, dcout), 0) \quad \dots (7b)$$

$$dS2 = M(\overline{M(bS2, dcout, M(0, bS1, dcout))}, M(M(bS2, dcout, M(0, bS1, dcout)), bS2, dcout), M(0, bS1, dcout)) \quad \dots (7c)$$

$$dS3 = M(1, M(\overline{dcout}, bS3, 0), M(M(dcout, \overline{bS3}, 0), bS1, 0)) \quad \dots (7d)$$

It is worth noting that the proposed circuit allows transforming the binary results coming from ADD1 to the BCD format through only four cascaded MGs, which are well below the eight and seven required by the ADD2 adders used with the same objective in [8],[15] and [16] respectively.

This whole process has been done using verilog HDL. For writing the code we use Xilinx ISE 13.2. The simulation of the program observed in the Model Sim. The above equations are written in the algorithm to realize the functionality of the developed circuit. We got the area in terms of LUTs. And performance in form of delay timing.

IV. RESULTS

After apply such innovative to the BCD adder we got the better result in terms of performance and number LUTs. The delay is reduced to dramatically reach the new level. As mentioned the LUTs have been reduced it means that the occupied area is less than the exiting adder.

The RTL view schematic of the circuit is shown in fig. 6.

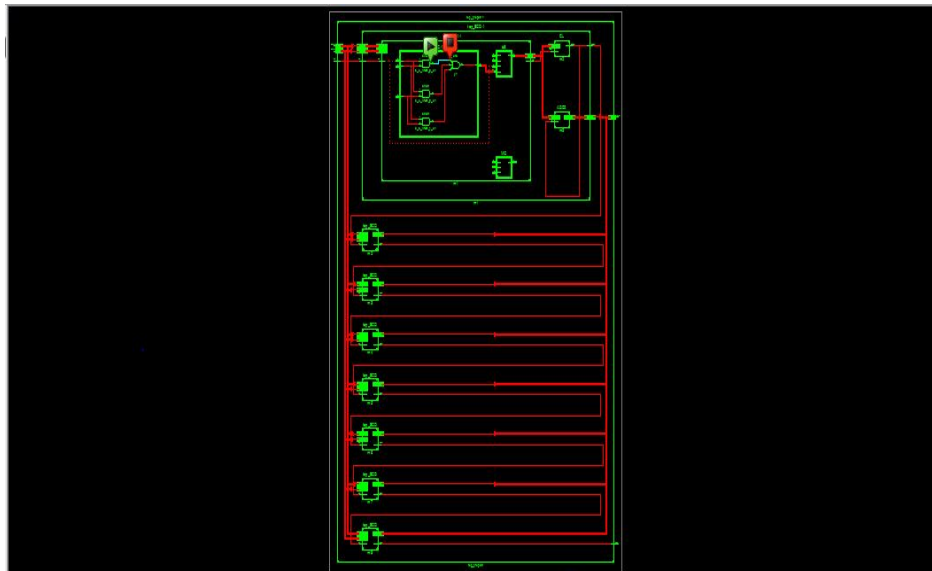


Fig.6 RTL view schematic

implemented the QCA technology in the 32bits of BCD adder. The result of the 32bits of BCD adder based of QCA have already mentioned in the last section of the result.

At last after consideration of the factor we can conclude that implementation of the QCA technology provides the better result.

Table. 2 Comparison Results of 16 bits BCD Adder.

Adder	Cells	Area[nm ²]	Clock Cycles
[16]	1348	2.28	8
[20]	1130	1.77	10
[21] CFA-based	932	1.36	4.75
[21]CLA-based	1838	1.86	2.5
[22]	1065	1.36	3.5

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