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Design and Comparative Analysis of Power Efficient 14T Mux Based CMOS Adder Cell using 22nm Technology

Shakthi Rajashekar[1]
[1]*Department of Electrical and Electronics Engineering, Dayananda Sagar College of Engineering, Bangalore-78, India*

Abstract: ***This Paper proposes a new mux based 14T adder cell designed to form a vital building block in computational systems. The performance metrics of the proposed full adder is compared by benchmarking with conventional and Shannon full adders. The designs also leverage the advantages of CMOS 22nm scaling when operated at a low power supply of 1v. Thorough simulations using HSPICE and PTM library models have been carried out on the adder cells considered and the parameters such as power, delay and PDP are investigated. The effect of temperature variation on the power consumption of proposed 14T mux based adder cell is also observed. The simulation results demonstrate that the proposed adder delivers stable output drivability with substantial diminution in the leakage power.***
Keywords: Half adder, Full adder, adder cell, CMOS 22nm, low power, delay, PDP

I. INTRODUCTION

Most of the combinational logic can be built with the use of multiplexers and it is a crucial element in building a digital computational system. Implementation of adders using multiplexers leverages the advantage of fast processing when employed in multiply and accumulate (MAC) units of SoCs. There are several variants of adders such as carry save adder, carry look-ahead adder, ripple carry adder etc., that form the important logic blocks for multi bit addition chains. This work focuses on the performance of a single bit full adder cell that performs the arithmetic operations in ALU of any processor. Though the function of full adders is to add or subtract a 1-bit binary number, the structure with which it is built is responsible for the performance metrics of it and in turn affects the entire computational block. A full adder can be implemented in many ways such as with a full custom transistor or with a logic composed of XOR/XNOR gates or by using any suitable pass transistor logic which consumes a minimum logic density. Also in conventional way a one bit full adder can be constructed from cascading two half adders and the circuits can be operated to carry out parallel addition or subtraction. The evolution of realizing different adders always tend to bring area efficient and power efficient computation under process constraints. In a typical ALU, adder cell logics are modified to operate as ripple carry counter to add an n-bit binary numbers. The speed of computation is major constraint in latest high frequency processors that are designed to be suitable for image and video processing. The rapid growth of portable electronic devices like mobile phones has driven the research towards low power implementation of the digital logic because of the lacuna in battery and power storage technology which has not advanced at the rate of microprocessor integration technology as predicted by Moore [5]. To overcome the limitation of battery technology, it is highly necessary to implement logic that consumes minimum power even under high speed computation. the conventional adder cell design using complementary MOS logic, the expressions for Sum and Carry outputs is obtained by CMOS pull up and pull down transistors and in building this cell, it is important to consider the effect of aspect ratio of the devices on the performance. This work uses CMOS 22nm process technology to attain minimum aspect ratio and low power consumption. This design work has been has been initialized with the conventional approach to construct the adder cell with CMOS adders having complimentary pull-up PMOS and pull down NMOS network. This adder required 42 transistors for generating sum and carry outputs. An alternative adder design using XOR logic and transmission gate is also investigated in which the transistor count is reduced to 30. The power consumption is also greatly reduced when operated at temperature of 26 degree Celsius. Starting from 28T conventional 1 bit full adder, researchers have designed adders using only 6T transistors Starting from 28T conventional 1 bit full adder, researchers have designed adders using only 6T transistors After the performance analysis of the above mentioned designs, in this paper it has been focused on the design of a low power mux based 14 transistor full adder based on CMOS technology and compared the same with the conventional 42 transistor full adder, transmission gate based 30 transistor full adder using XOR logic and Shannon based pass transistor full adder logic at the same process technology

II. DESIGN OF HALF ADDERS

Initially performance of half adders with CMOS implementation has been analyzed. The conventional half adder requires 18 transistors to provide sum and carry outputs. Then the half adder design is improvised by a 6 transistor implementation [2] using transmission gates to reduce the area. Comparison of conventional method and transmission gate logic base technology has yielded the inference that in transmission gate based logic to implement adders, the complex expressions can be implemented by minimum number of transistors, fetching us the reduction in logic density. The NMOS transistor has the property of signal deprivation when supplied in chain of transistors with logic"1" while PMOS degrades for transmission of logic level "0".In conventional half adder logic. If a transmission gate is employed in the design, perfect transmission can be obtained. The only problem with transmission gate are if several stages are incorporated then there is a chance of signal degradation and proper logic for on and off condition of transistors is important. The complemented bits for the inputs are obtained by implementing CMOS inverter at input stages and also for the carry logic. In Fig. 1 depicts the input to CMOS inverter i.e. if A is supplied with logic 0, the output $\bar{A}$ is pulled to Vdd by pull up (M1-PMOS device) during which the pull down (M2-NMOS device) will be shut off.[8] Similarly when the input A is supplied with logic 1, the output is pulled down to ground. The inputs are timed such that all combinations of half adder logic can be validated.

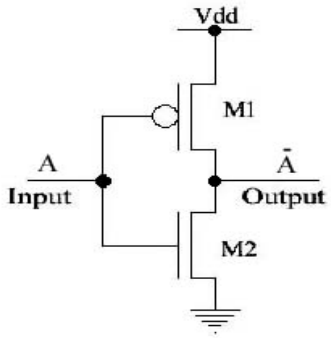

Figure 1. Conventional CMOS inverter

A. Boolean Expression For Half Adder

SUM = AB'+A'B (A XOR B) [3]

CARRY = A.B (A AND B)

The conventional CMOS circuit of half adder is depicted in figure 2. This logic implementation has 18 transistors including that of complemented inputs. Since the circuit is not found to be area efficient, A 12T transmission gate based half adder has been designed and analyzed

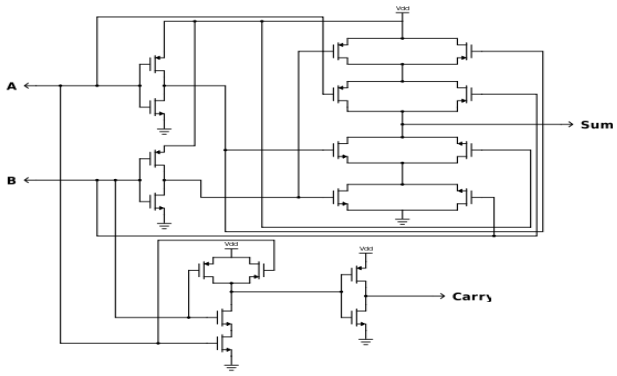

Figure 2. Conventional 18T half adder in CMOS logic.

Figure 3.depicts the half adder implementation using transmission gate. Reduction in number of transistors for one bit design infers that more transistors can be accommodated on the same die to include other logics or also in case to increase the number of input bits. Less number of transistors also reduces the switching activity of transistors and there will be lesser dynamic power

consumption. In the analysis, it has been observed that the transmission gate based half adder power consumption is reduced by 55.35 percent and also the transistor count is reduced by 33.33 percent in comparison with conventional half adder design.

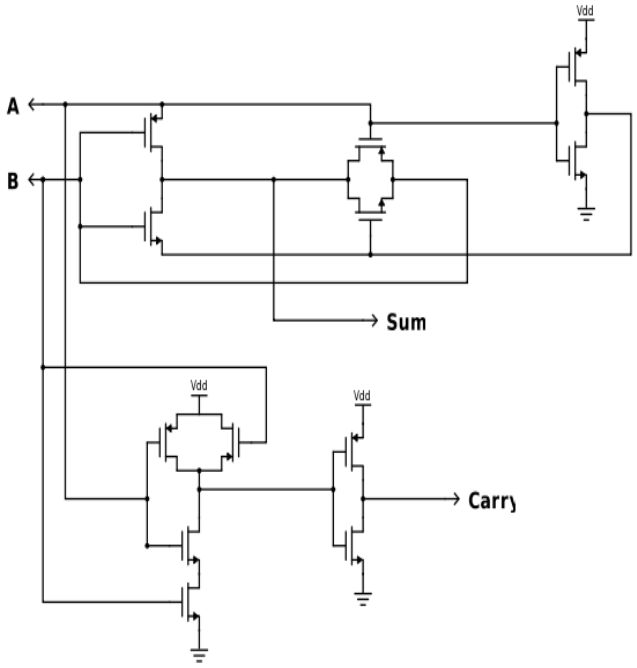

Figure 3. 12T Half adder using Transmission gate

III. A . DESIGN OF FULL ADDER

In the full adder design we incorporate an additional input carry-in along with the other two inputs of a half adder. In an n-stage addition, the carry-in (Cin) represents the output of a previous logic stage that has been fed as an input the current addition logic cell. The output of the full adder cell is designated as carry-out (Cout) that can be passed on to several stages and the Sum (S) is the resultant output of binary addition. The number of full-adders is proportional to the number of bits considered for addition. The full adder logic can be implemented by studying its truth table having all possible combination of input. The output S is an XOR operation between the input A and the half adder SUM output with B and Cin inputs. The carry out is found to be true only if any of the two inputs out of the three are high. Thus, we can implement a full adder circuit with the help of two half adder circuits. The first half adder is used to add A and B to produce a partial SUM. The second half adder is used to add Cin to the partial SUM produced by the first half adder to get the final SUM output. The carry of the half adders is ORed to get the final CARRY output. Figure 4 depicts the block diagram of a 1bit full adder.

Figure 4. Schmetic representation of full adder

A full adder can be formed by logically connecting two half adders. The block diagram depicted in figure 5 is the implementation of full adder by cascading two half adders.

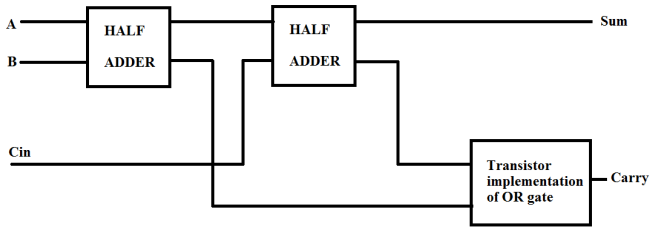

Figure 5. Implementation of Full adder using Half adders

The expressions of SUM and Cout are

$$S = A'B'Cin + A'BCin' + ABCin$$
$$Cout = AB + ACin + BCin \text{ -------(1)}$$

Equaltion 2 represnts the boolean simplification of sum

$$S = A'B'Cin + A'BCin' + ABCin$$
$$= Cin (A'B' + AB) + Cin' (A'B + AB')\text{--------(2)}$$
$$\text{Therefore } S = Cin \text{ XOR } (A \text{ XOR } B)$$

The carry expression is as follows

$$Cout = AB + ACin + BCin\text{--------(3)}$$
$$Cout = AB + ACin + BCin (A + A')$$
$$=ABCin +AB + ACin +A'BCin$$
$$= AB (1 + Cin) + ACin + A'BCin$$
$$= AB + ACin + A'BCin$$
$$= ABCin + AB + A'BCin + A'BCin$$
$$= AB (Cin +1) + AB'Cin + A'BCin$$
$$= AB + AB'Cin +A'BCin$$
$$= AB + Cin (A'B + AB')\text{---------(4)}$$
$$\text{Therefore } Cout = AB + Cin (A \text{ XOR } B)\text{-------(5)}$$

Equaltion 5 represents the boolean simplification of carry

Based on the expresssions found in equations (2) and (5) the full adder circuit can be implemented using two half adders and an OR gate. The conventional full adder design has incurred 42 transistors including that of complemented inputs. In the design of full adder by cascading two half adders stages, we need 12 transistors for each half adder stage and an OR gate logic for carry output comprising of 6 transistos as depicted in figure. 6. The transcient analysis of this conventional full adder with 42 transistors at the normal temperature of 25 degree celcius has deliverd an average time delay of 5.021 ns for the input to output propagation. The maximum power consumption of the conventional 42T full adder is found out to be around 98.79 uW because of swift swithing of transistors for different input combinations.

The improved full adder using cascading of two half adders and an OR gate implementation provides reduced power consumpation. As the transistor count is reduced to 30 the dynamic swithcing has been be reduced leading to a drastic decline in power consumption to 30.21 uW. Also The simulation of this full adder at normal temperature at 25 degree celcius has incurred an average time delay of 7.02 ns. Also reduction in transistors leads to reduced parasitic capacitance and reduced output leakage current.

IV. B: IMPLEMENTATION OF OR GATE

The carry logic is implemented by an OR gate built with CMOS inversion of universal NOR logic as depicted in Figure 6. The output of the CMOS implementation of NOR gate is high if and only if both inputs A and B are low. The worst case pull down

transistion happens when only one of the NMOS devices turn on (i,e. if either A or B is high) for the NOR gate, The output is discharged when all inputs are driven high.

Cascading the NOR output with CMOS inverter provides the OR logic suitable to offer the carryout signal computed from the cascaded half adders as described in (5)

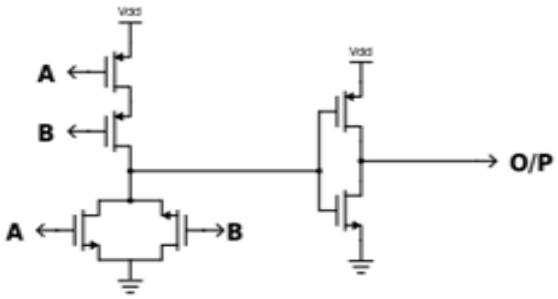

Figure 6. Implementation of or gate using transistor.

V. SHANNON'S FULL ADDER

A. SHANNON'S THEOREM

The Shannon theorem explains that the logic expressions are divided into two parts wherein in the first part a variable value is set to logic 1 and multiplied by a multiplier variable and in the next part the original variable that was set to logic 1 is then set to logic 0 followed by its multiplication with complement of multiplier variable. The entire logic can be reduced by repeating the Shannon's theorem [1]The generalized Shannon expression of many variables is as depicted below.

F(a0 ,a1, a2,y ,ai, y, an) can be written as the sum of two terms, one with a particular variable (say ai) set to 0, and one with it set to 1. [1]

f(a0,a1, a2….,ai,….,an) = ai' f(a0, a1, a2……,0,….,an)+ ai f(a0,a1,a2,…1,…an).[1]

Fig 7 depicts the Shannon's full adder network. In this (n-1) variables are used as control inputs connected to gates of the transistors based on whose value the data available at inputs of the pass transistors are transmitted towards the output[7]. In case of a one bit full adder in figure 7 the B and complement of B provide transmission path to original and complimented variables of A and Carr-in Thus realizing the sum expression in a modest transistor structure. Similarly the carry out is implemented by three control lines. In the represented structure it is important to note that control signal lines are connected to gates to control the switching and the data inputs are connected to drains of the transistors to pass the data. In carry out design we use carry in from a previous stage, Vdd logic1), and ground (logic0) as pass variables. In Shannon's full adder, the sum logic is a two input XOR operation built with multiplexer method.

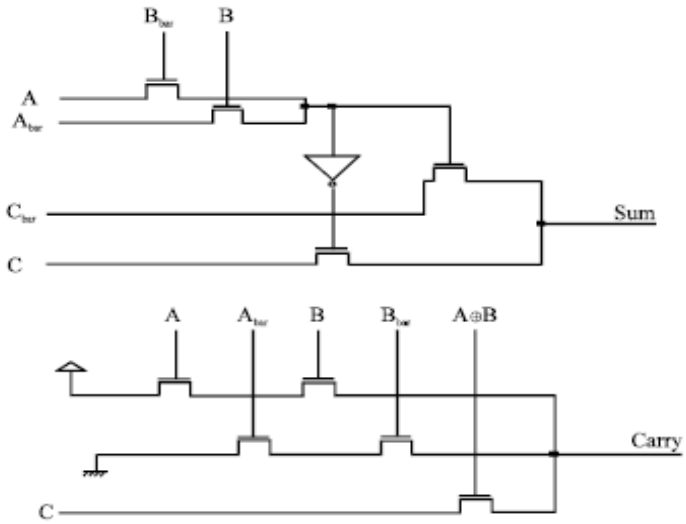

Figure 7. Shannon's based adder using pass transistor logic.

VI. 14T MUX BASED CMOS ADDER CELL

The adder implementation using multiplexers has become fascinating topic in computational research in current shrinking technology due to the significance of targeted constraints such as area, power and speed. This paper proposes a one bit full adder by using 14 transistors targeted for low power consumption. The proposed design features conventional logic inversion wherever needed and avoided the Shannon based pass transition method for sum and carry. In the proposed circuit, by not using pass transistors it has been improvised reduce the effect of signal degradation that occurs due to passing of data in a longer adder chains. Since the design incorporates a low operating voltage of 1v, and a transistor count of 14 which yields lesser power consumption and parasitic capacitances[4]. Also the problem of voltage swing restoration can be avoided. The propagation speed from any of the three inputs to sum or carry outputs is also improved. The 14 transistor mux based adder is as fast as that of 30 transistors mux based full adder discussed earlier. his is achieved because of the implementation of three multiplexers implemented with two NMOS transistors is as depicted in figure 8 to select among input combinations of A,B and Cin. The maximum power consumption is significantly reduced to 1.656uW compared to all the designs discussed.

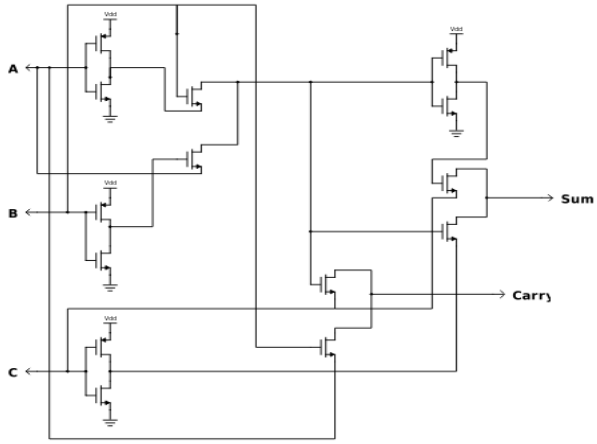

Figure 8. 14-T MUX CMOS adder circuit

The conventional 42T full adder, Transmission gate based 30T full adder, Shannon full adder and proposed 14T mux based full adder are designed and simulated in full custom method in HSPICE with CMOS 22nm PTM library models for comparison and analysis in terms of power consumption and delay.

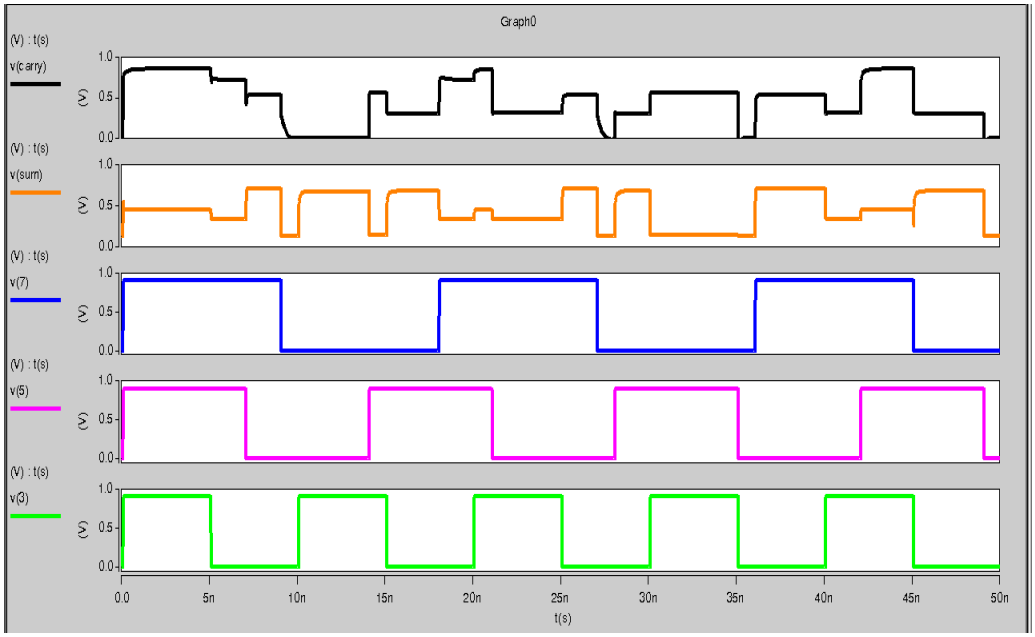

Figure. 9. Output timing waveform of 14T MUX based full adder[9].

The output waveform for design of the 14T MUX based full adder is as depicted in figure 9. The output validates the truth table of the conventional full adder. Figure 10 depicts the effect of temperature variation on the instantaneous power consumption of proposed 14T mux based adder cell.

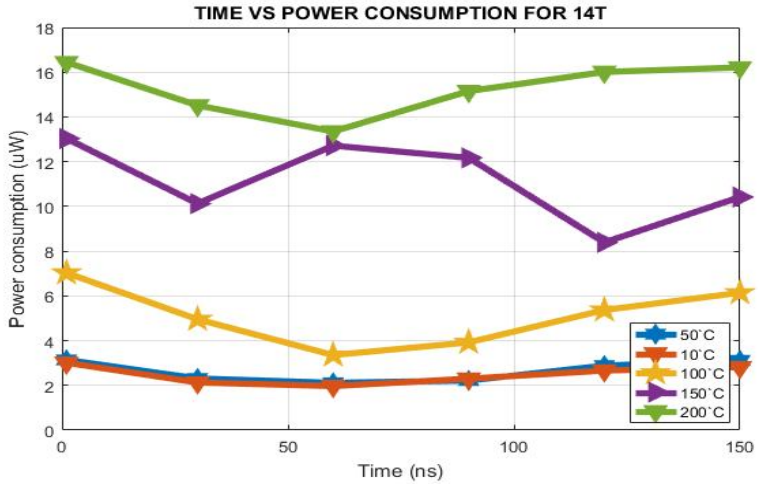

Figure 10. Graph of Time versus Maximum power consumed at different temperatures

VII. COMAPARITIVE ANALYSIS

In this section comparative analysis is carried out with respect to power and delay on the conventional 42T full adder, Transmission gate based 30T full adder and proposed 14T full adder. The below graph depicted in Figure 11 is time Vs power consumption. It infers that 14T mux based transistor has a significant reduction in power consumed

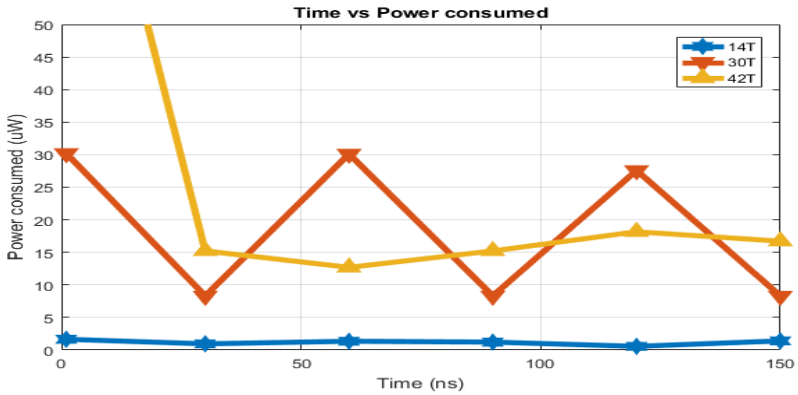

Figure 11. Graph depicts effect of variation of power on time for all the full adders

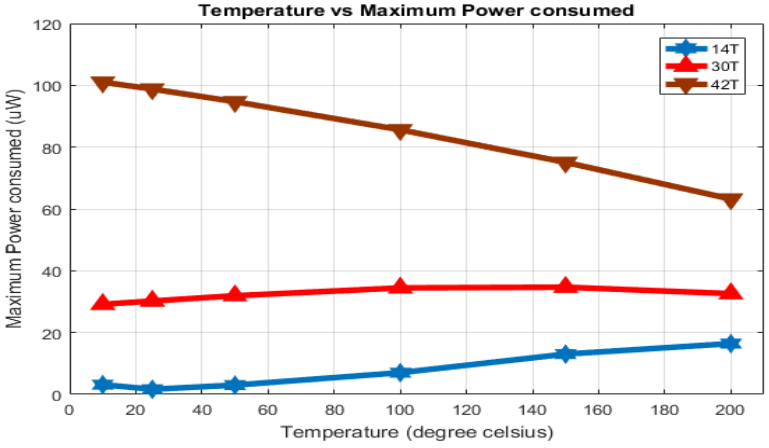

Figure 12. Graph depicts effect of temperature on Maximum power consumed for all the full adders.

Figure 12 depicts the comparison of conventional and mux based full adders with respect to increase in operating temperature, it is observed that that the power consumed by 42T conventional full adder is high because of increased dynamic power consumption with increase in temperature. The transmission gate used 30T full adder has lower maximum power consumption but it fluctuates at equal time interval. The 14T low power MUX full adder has low power consumption throughout and a steady increase at high temperatures. This establishes that the 14T full adder has greater stability to heat occurred due to process variations or device switching overhead.

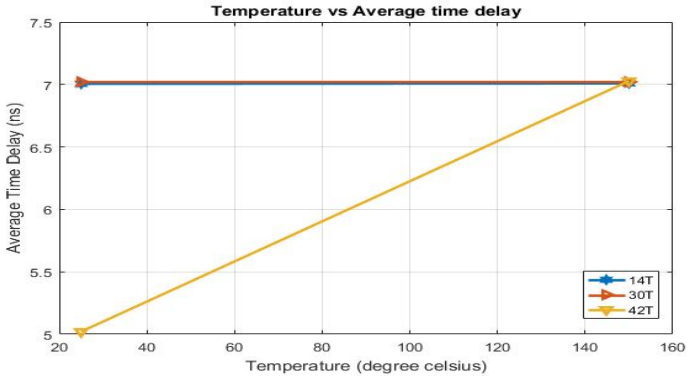

Figure 13. Graph depicts effect of variation of average time delay on temperature for all the full adders

Figure 13 depicts the effect of variation of temperature on propagation delay. It is observed that for mux based and transmission gate based adders, the delay is almost constant at 7 ns, whereas for conventional 42T full adder, there is a steady increase in delay with increase in temperature.

It is palpable that 14T mux based adder is having a stable speed of operation even under abnormal temperatures and it can be determined that the proposed adder can be incorporated high speed computation logic blocks.

VII. CONCLUSION

For low power operation and stable logic propagation this paper proposes a new 14T multiplexer based full adder designed with 22nm CMOS device scaling. The design has a maximum power supply of 1 volt and aspect ratio of 1:2 for pull up devices and 1:4 for pull down devices. The design has yielded the results that are rather less in power dissipation under linear variation of time and temperature. The adder also possesses a steady propagation delay when compared to conventional CMOS full adder, transmission gate based full adder and as well has Shannon's full adder. With just 14 transistors in its architecture the leverage of this design is to incorporate the adder cell in multi bit high speed data computation systems.

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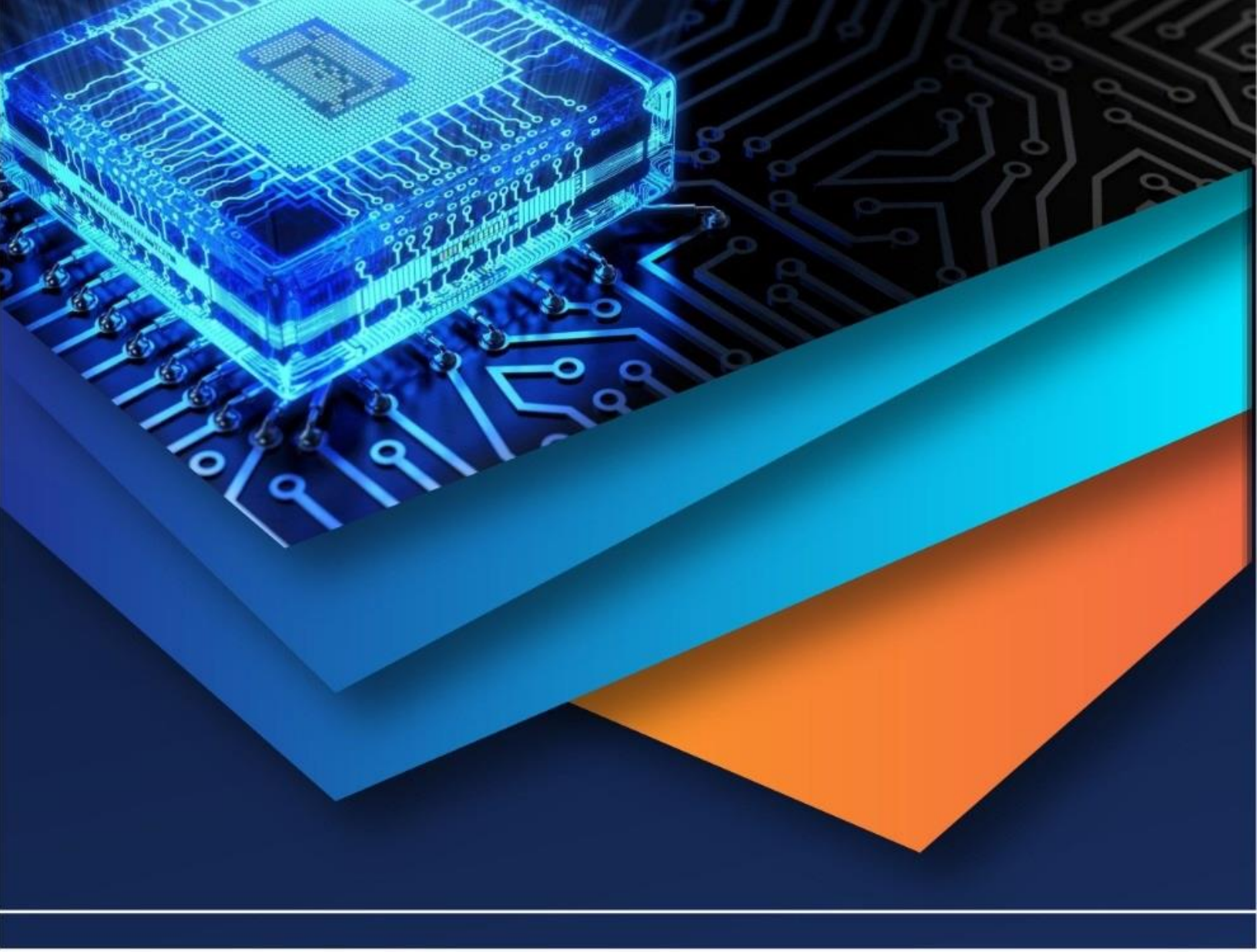

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