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Design & Analysis of Low power 10T Sram for High SNM using 45nm Design

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Abstract: In this paper a new 10T static random access memory cell having decoupled 5T write port with single bitline and single ended read-bitline (RBL) with 5T read port for low power operation. The RBL is precharged upto cell's supply voltage, and is allowed to charge and discharge according to the stored data bit. A read-enable(RE) signal is used to drive read port inverter, which connects the RBL to the virtual power rails through a transmission gate during the read operation. RBL remains at VDD or increases toward the VDD level for a read-1, and ground or discharges toward the ground level for a read-0. Read-Enable(RE) signal is kept at low level during the write and the hold mode, and connected to high level only during the read operation. The proposed 10T cell in a commercial 45 nm technology provides 420mv read static noise margin, and reduces the write power dissipation by 30.47% and read power dissipation by 23.6% than that of 6T.

Keywords: 10T, low power, precharging, single ended (SE) read bitline (RBL), static random access memory (SRAM), virtual rails, Read Enable.

I. INTRODUCTION

Requirement of fast and low power primary memory for all battery operated device is increasing very rapidly. So we need SRAM's which are faster and dissipate less power. Hence, power dissipation has become a first class design constraint [1], as static random access memory (SRAM) is the most important digital macro and its portion on a system-on-chip (SoC) is ever increasing [2]. Reducing the SRAM power dissipation will lower the whole system power dissipation and SoC reliability will increase. Supply voltage reduction is one of the straightforward way to reduce the power consumption because reducing supply voltage improves dynamic and leakage power significantly.

Although the six transistor (6T) SRAM cell is mostly used standard in industry, it has many limitations like poor read stability, read static noise margin (RSNM) degradation [3].

In past decades, many efforts have been taken to model a stable SRAM for low power systems. Researchers have presented many configurations for SRAM and adopted different methods which includes negative bitline voltage [5], write back schemes, Dual rail supply power [8], isolating read path from storage node whereas they all have two complementary bitlines which consumes more power during switching.

The SRAM cell single ended (SE) 8T, 9T, 10T and differential 7T , 8T , 9T and 10T eliminates the stability problem by separating the storage nodes from the bitlines yet leakage power is high. Furthermore, to reduce power there are many 5T – 10T SRAM cells have been explored. They use single bitlines to reduce power and to minimize the area.

A 10T cell in uses virtual ground rail for read port to achieve lower BL leakage and differential, while Kanda et al. used row-by-row dynamic control of cell supply voltage and negative wordline voltage for 2 orders of magnitude reduction in leakage currents. In this paper, we present single bitline(BL) 5T for write operation and. A 5T read port is designed to employ VDD precharge and charge recycling technique for low power read operation the proposed technique.

Read BL (RBL) is charged and discharged through the read port according to stored bit. Read port is activated by read activate line(RA) and virtual power rails that run horizontal and are shared by the cells of a word. So RBL leakage is reduced due to dynamic control of read port.

This paper is organized as follows. In Section II, we review the conventional 6T SRAM. Section III presents the proposed cell and its associated scheme. The simulation layout and results are represented in Section IV. Finally, a brief conclusion is presented in Section V.
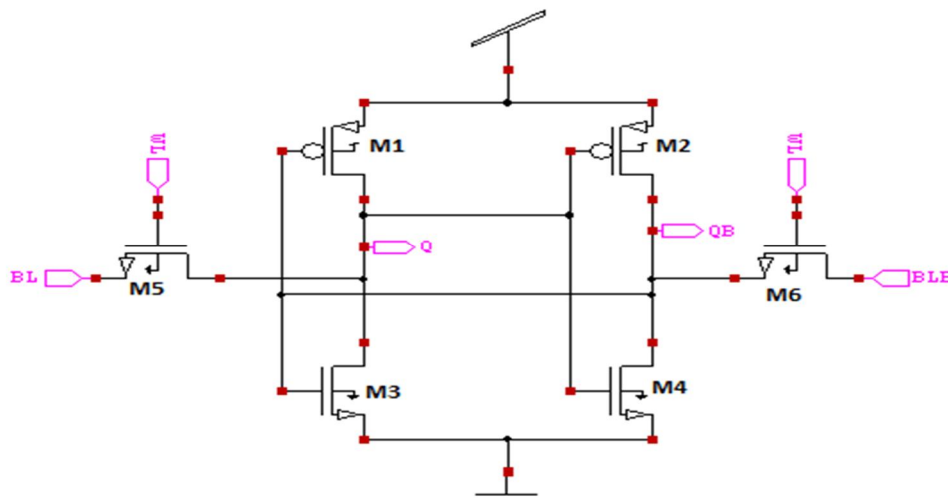
II.   CONVENTIONAL 6T SRAM

Fig 2.1 Circuit Diagram of 6T SRAM

In SRAM there are three mode of operation i.e. write,read,hold. Basically, cross-coupled inverters with positive feedback are used to store single bit data in complementary mode.In conventional 6T SRAM as shown in Fig. 1, for write operation BL is charged '1' or down to '0' regarding the data to be stored .BLB is charged by inverted voltage of the bitline (BL). To write '1' BL is charged to Vdd and WL is made high such that the current passes through M3 and M4 transistors and '1' gets stored in node Q through M3 and M4 and '0' stored in the node QB, which makes the transistors M1 and M6 ON.To write '0' BL is retained at ground and BLB id charged to Vdd so that '0' is stored at Q and '1' at QB. During read phase BL and BLB are precharged to Vdd and then WL is made high such that the transistors M3 and M4 turns ON. For read '1' BLB gets discharged to ground through the M6 transistor. BL is not discharged and remains in Vdd since the M5 transistor is OFF. And it is read through the sense amplifiers.

III. DESIGN OF LOW POWER 10T SRAM

For read stability , high SNM and low power, we proposed a new 10T SRAM as shown in figure. This new 10T SRAM has single bitline(BL), wordline(WL), Read port consists of an INV P1-N1 driven by node read access(RA), and a transmission gate (TG) P2-N2. The output (H) of the INV is connected to RBL during the read operation through TG, which is controlled by (read) control signals. Furthermore, read port is powered by virtual power rails. Use of TG is to improve the efficiency of read-1operation,as the single nMOS could not charge well the RBL through P1.
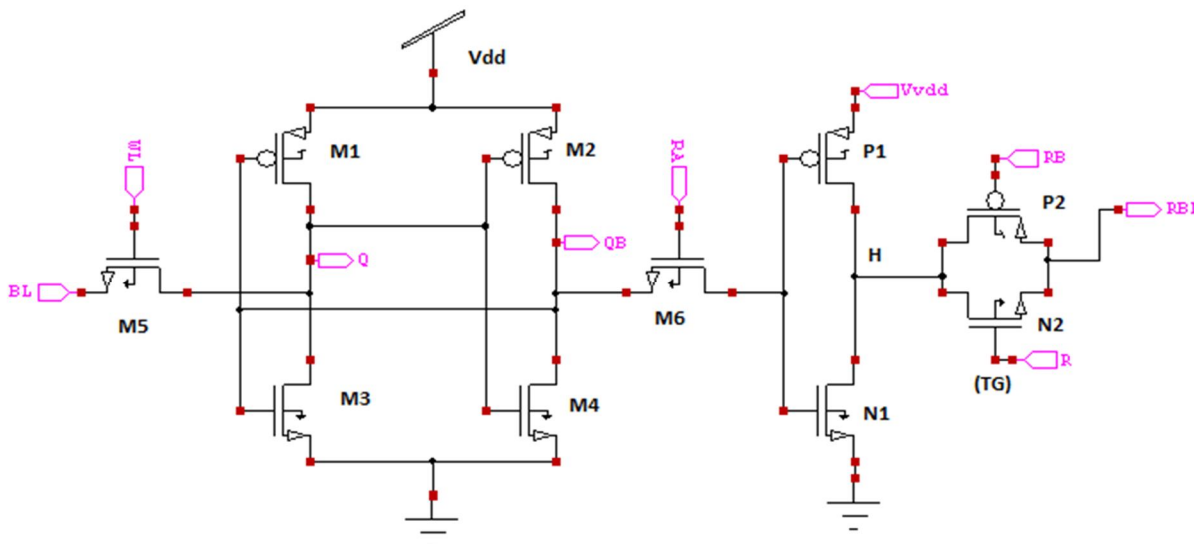

Fig 3.1 Circuit Diagram of proposed 10T SRAM

A. Write Operation

To write data in sram BL is charged correspondingly and then WL is loaded to Vdd. Strong access transistor N3 allows bit line to over power the cell, so that required data will be written into the cell. During write operation RA will be kept at logic '0' i.e. inactive.

B. Read Operation

In proposed 10T SRAM, RBL is precharged to Vdd. For the read operation, RA is High so that INV P1-N1 is driven by QB and R kept high and RB low and thus the TG is activated to connect RBL to the node H. If QB is 0, then N1 is OFF and P1 connects node H to the VVDD, which is high for the read operation. Thus, the no current will flow from VVDD (having value of vdd) to RBL (which is precharged to Vdd) through P1-TG. Hence, the RBL voltage remains at vdd level. Now, for a read-0 operation (i.e., QB=1), P1 is turned OFF and N1 connects node H to the GND. Thus, the read current flows from RBL (having value vdd) to the GND through TG-N1, and hence RBL voltage decreases toward 0 V.

1V.   SIMULATION RESULT

A. Power Calculation

Total power consumed by SRAM is sum of the power drawn from source used as main supply and sources used to charge and discharge the bit line BL and BLB(in case of 6T)and word line (WL) and sources used for read port in proposed 10T SRAM cell.

TABLE I: Comparative analysis of 6T and proposed 10T SRAM

Topology	Power (μW)		Delay(ps)		Power-Delay Product
	Write	Read	Write	Read	($\times$ 10^{-15} watt-sec)
6T (β=2)	17.26	12.3	152	40	5.67
Proposed 10T	12	9.4	167	20	4.00

Here by assuming equal probabilities of write '0' and write '1' operations. During write operation of conventional 6T SRAM cell, BL and BLB are loaded with complementary data and after that charged values are floated. During write operation, it is assumed that the one of the charged value is discharged.. So during a write operation power dissipation happens twice. In case of write operation of proposed 10T SRAM cell, single bit-line is used and it is charged if the data need to be written is '1' and it is not charged to write '0'. After the write '1' operation, BL is discharged. So power dissipation is almost half as compared to conventional 6T SRAM Cell. During read operation of 6T SRAM Cell, both the bit-lines are charged to VDD and one of the bit lines will discharge regarding to the value stored in the cell and remaining bit line will be discharged after the operation is completed. So in read operation power dissipation is four times. In proposed 10T SRAM cell seperate 5T is used for read operation. Hence power consumed during read operation is half compared to power consumption in conventional 6T SRAM cell.

B. Static Noise Margin(SNM)

The term SNM defines the immunity of cell to noise and defined as maximum amount of noise voltage that can be tolerated by the cell without flipping its data [8] [9]. To determine the SNM various methods are present. we used graphical approach in which 'Butterfly' curve is drawn by superposing static voltage transfer characteristics(VTC) of one inverter to the inverse VTC of the other inverter of the SRAM cell inverters as shown in Fig 4 [10]. SNM value is defined as the length of largest side of the largest square that can be fitted inside the "butterfly" curve. Comparative Analysis of RSNM, WM and HSNM between conventional 6T and proposed 10T SRAM cells architectural designs at 1.2V at 45nm
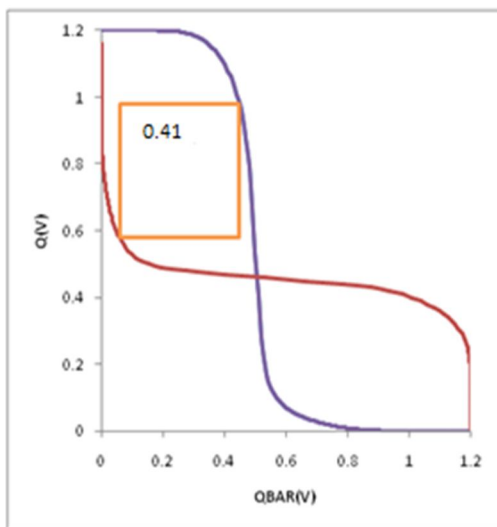
Figure 4.1(a) Butterfly curve to evaluate
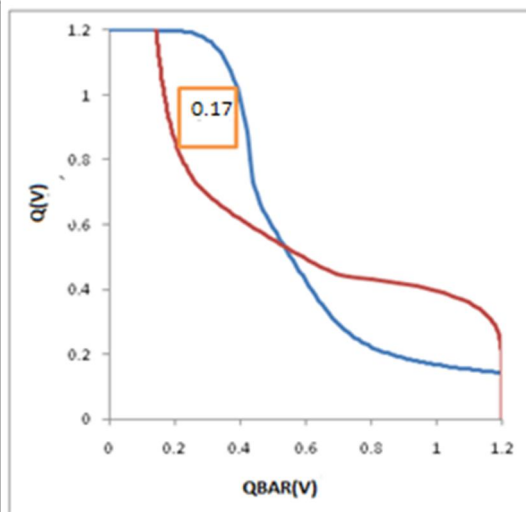RSNM for proposed 10T SRAM cell

Figure 4.1 (b) Butterfly curve to evaluate RSNM
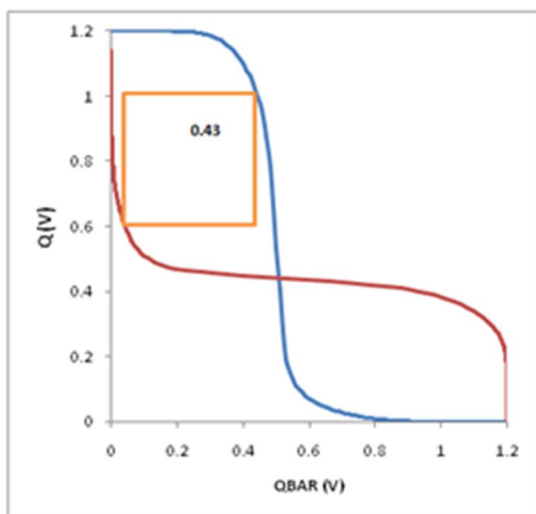for conventional 6T SRAM cell.

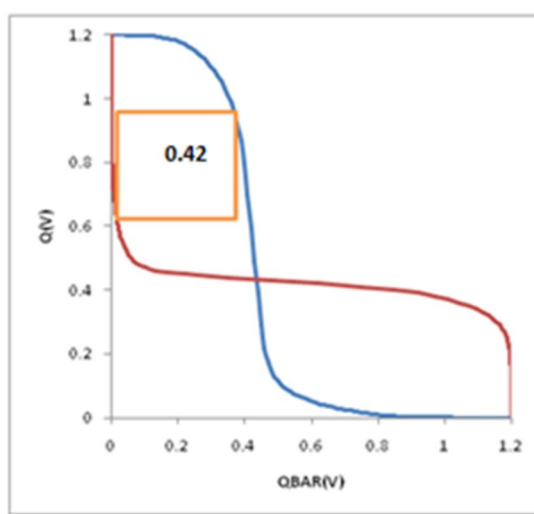Figure 4.2 (a) Butterfly curve to evaluate HSNM for
10T SRAM cell

Figure 4.2 (b) Butterfly curve to evaluate HSNM of proposed
6T SRAM cell

In this work, for WM calculation bit-line voltage sweep method has been chosen. WM is defined as the value of bit-line voltage where Q and Q_{BAR} flip. The final WSNM is the minimum value of WM for writing logic "1" and writing logic "0". If lower is the final WM value, harder is to write the cell and smaller is the write margin
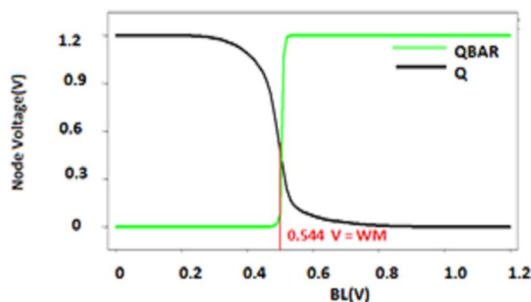

Figure 1.6 WM of proposed 10T SRAM

TABLE Comparative Analysis of RSNM, WM and HSNM between conventional 6T and proposed 10T SRAM cells architectural designs at 1.2V at 45nm

Topology	RSNM (mV)	WM (mV)	HSNM (mV)
6T (β=2)	170	460	420
Proposed 10T	420	544	430

V.   CONCLUSION

With the aim of low power and high SNM, proposed 10T and conventional 6T SRAM cell architectural designs are simulated, analysed and compared. 10T SRAM cell with single bitline consumes 21.4µW power which is 38.1% less than conventional 6T SRAM cell with 29.56µW power. In case of read power consumption, 10T SRAM cell with single bitline consumes 9.4µW which is 23.57% less than conventional 6T SRAM cell with 12.3 µW. 10T SRAM cell with single bitline has quite high RSNM that is 420mV which is 2.47 times more than 6T SRAM cell with 170 mV. The WM of 10T SRAM cell with single bitline is 544mV which is 1.14 times more as compared to conventional 6T SRAM cell with 460mV. The HSNM of 10T SRAM cell with single bitline is 430 mV which is 1.05 times more as compared to conventional 6T SRAM cell with 420mV

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