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Design and Analysis of Row Bypass Multiplier using various logic Full Adders

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Abstract*: *The key structure for designing an energy-efficient processor is Multipliers, which decides the efficiency of Digital Signal Processors and it is commonly used in digital devices. The critical path that affects the overall speed of the system is Adders. Multipliers are the main sources and Full adder is the main block of power dissipation in DSP blocks. In this project, a Row Bypassing Multiplier using Full Adders that have various transistor count is analysed. The parameters like area, power, delay, PDP and transistor count is compared. The designs are implemented using Tanner EDA with IBM 130nm CMOS technology.

Keywords*: *Multiplier, full adder, row bypass, power dissipation, Digital Signal Processors.

I. INTRODUCTION

The multiplier is the main block in arithmetic unit and it is used in many DSP applications. A multiplier is designed in such a way that it reduces power dissipation [1]. The multiplier typically operates at high system clock rate, reduces its delay since it is a complex circuit and it is an essential part of the design. Multipliers and their associated circuits (adders and accumulators) along with registers consumes significant portion of power for most of the DSP applications. Therefore, it makes sense to increase their performance by customization and architecture optimization. So in this work, bypassing technique is adopted and it is almost critical design. This bypassing technique would result into much lesser power consumption even though architecture is bigger than the usual. This technique also reduces power, area and quantum cost of the design. This bypassing technique does low power design at architecture level.

Row and column bypass multiplier is a new design which reduces the switching activities with architecture optimization:

Row bypassing technique is based on number of zeros in the multiplier bits [2]. In this multiplier operation, some rows of adders in the basic multiplier array are disabling during operation to save the power. Row bypassing multiplier consumes lesser power than the Braun multiplier at higher frequency of operation. It consists of the rows of the ripple carry based full adder cells.

Column bypassing technique is based on number of zeros in the multiplicand bits. In this multiplicand operation, some columns of adders in the basic multiplier array are disabled during operation to save power [2]. At high frequency of operation it consumes less power compared to the Braun multiplier and also it eliminates the extra correcting circuit, skipping the cell of a full adder. The rows of carry save adders are present in this multiplier. The reduction of switching transitions is required to perform the computations of the Column Bypass Multipliers.

Thus in this Row Bypassing Multiplier has been taken.

II. LITERATURE SURVEY

In this paper, the various types of Multiplier techniques are surveyed.

A. Array Multiplier

The structure of array multiplier is regular. The algorithms for multiplier circuit is based on add and shift algorithm. The partial products are generated by the multiplication of the multiplicand with one multiplier bit. According to the bit orders, the partial products are shifted and then it is added. The array multiplier composition is shown in Fig.1. A one to one analytical correspondence between the structure of hardware and the manual multiplication is shown in figure. The X*Y AND gates (two bit) are required for the n partial products generation. The adding of n partial products, which requires X-1, Y-bit adders consumes large area in the multiplier. The simple routing is performed for the shifting of the partial products for their proper alignments and no logic is required. The overall structure can be easily being compacted into rectangle, resulting in very efficient layout.

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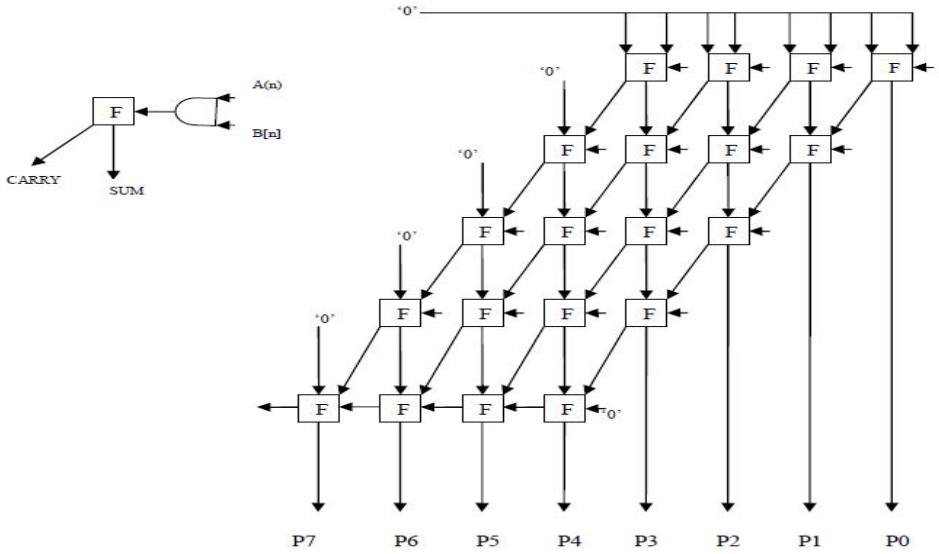

Fig.1.Array Multiplier Architecture

B. Baugh Wooley Multiplier

In signed multiplication, the length of the partial products and the number of partial products will be very high. So an algorithm was introduced for signed multiplication called as Baugh Wooley algorithm. The Baugh-Wooley multiplication is one amongst the cost-effective ways to handle the sign bits. This method has been developed so as to style regular multipliers, suited to 2's compliment numbers Baugh – Wooley algorithm for the unsigned binary multiplication is based on the concept shown in Fig.2. According to the algorithm all possible AND terms are created first, and then it is sent through an array of half-adders and full-adders with the Carry-outs are chained to the next MSB at each level of addition. A Baugh-Wooley multiplier is used to multiply negative operands.

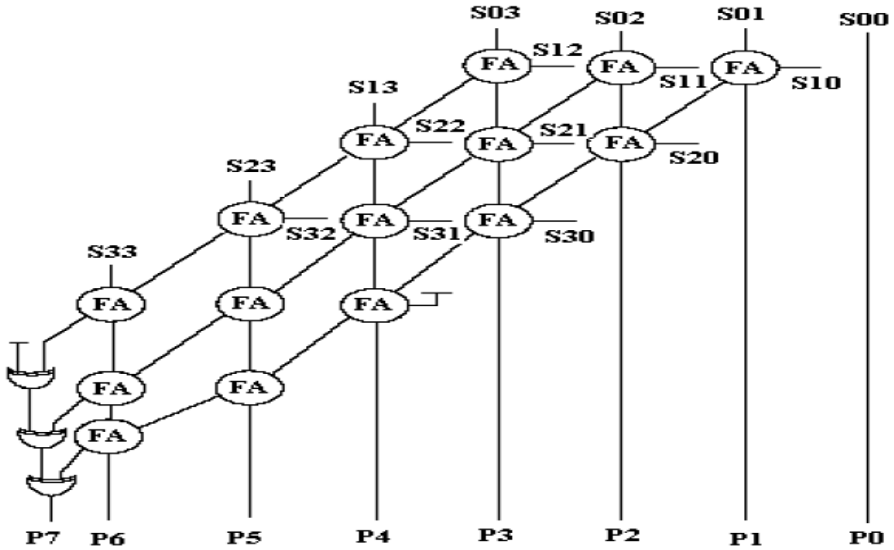

Fig.2. Baugh Wooley Multiplier Architecture.

C. Braun Multiplier

It is a simple parallel multiplier which is generally called as carry save array multiplier. It is restricted to perform signed bits. The structure of the Braun multiplier consists of array of AND gates and adders arranged in the iterative manner and no need of logic registers. This can be called as non –addictive multipliers. All the partial products are computed in parallel form, and then it is collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the Carry Save array, and by the propagation of carry in the adder. This multiplier is suited only for positive operands. The Braun Multiplier algorithm structure for the unsigned binary Multiplication is shown in Fig.3.

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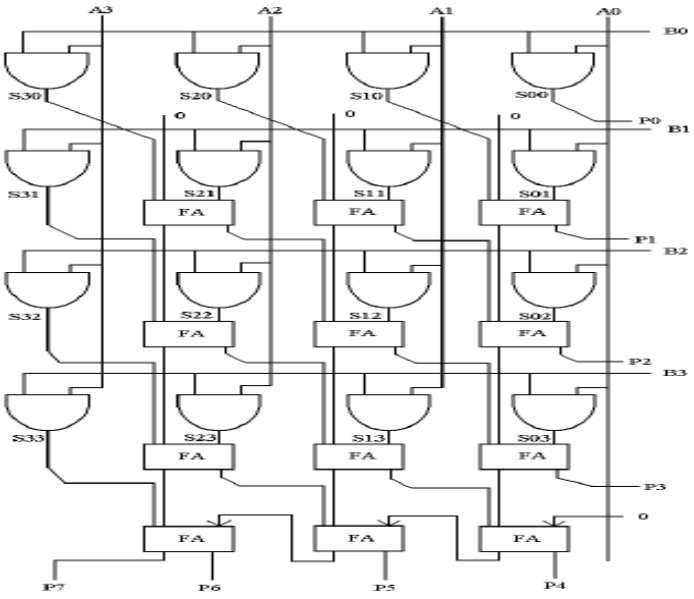

Fig.3.Braun Multiplier Architecture

D. Reversible Multiplier

In this design, Reversible logic has been used as one of the application approaches for the power optimization with its application in low power requirement of VLSI circuit design. Modification of Reversible logic circuits design have theoretically zero internal power dissipation because they do not lose information, the classical set of gates such as AND, OR, and EXOR are not reversible. TSG gate is used in place of Full Adder, capable of implementing all Boolean functions and can also work singly as a reversible Full Adder. The 4 bit Reversible logic Multiplier is illustrated in Fig.4.

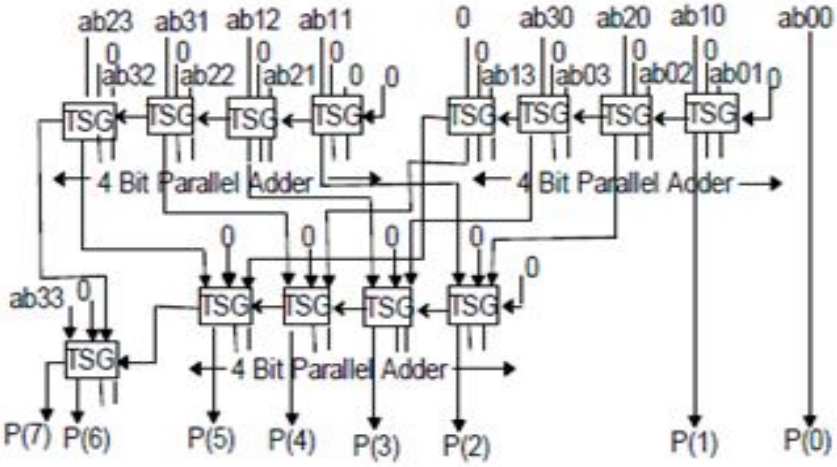

Fig.4.Reversible Multiplier

III. PROPOSED ROW BYPASS MULTIPLIER USING VARIOUS ADDERS

Row bypassing circuit comprises of half adder, multiplexers and various full adders. In this we have chosen 4x4 row bypassing multiplier with reduced switching activities [3]. The corresponding partial product is zero, the FA & unnecessary transitions is disabled and bypasses the inputs to outputs. Two multiplexers augmented to the outputs of the adder transmit the input-carry bit and the input-sum bit of the previous addition to the outputs. The tri-state buffers placed at the input side of the adder cells disables the signal transitions in the adders which are by passed, and then the input-carry bit and input-sum bit are passed downwards. If the switching activity is reduced, the power consumption can also be reduced. An another method to reduce the switching activity is to shut down the idle part of the circuit which is not in operating state. (n-1)(n-1) full adders, 2× (n-1)×(n-1) multiplexers, and 3×(n-1)×(n-1) three state gates are included in this design. The full adder cell of row bypassing multiplier is shown in Fig.5.

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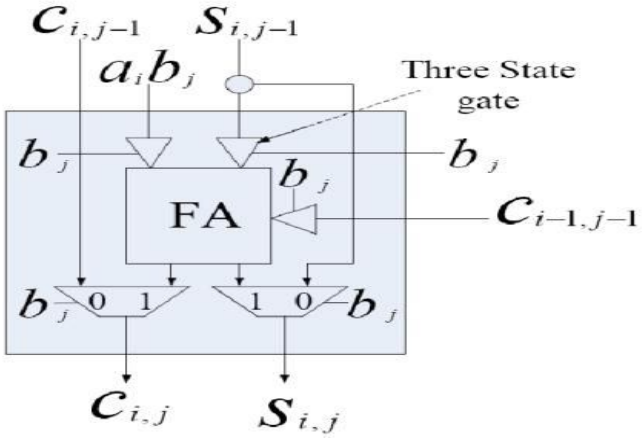

Fig.5.Row Bypassing Full Adder cell.

A detailed Row Bypass Multiplier using various Full adders with different transistor count, their bypassed designs and output waveforms are given below:

A. 8t Row Bypass Multiplier

Three transistor XOR gates are used in this proposed full adder. The silicon area is less. The power dissipation of 4T XOR gate is slightly less than the 3T XOR gate but the 3T XOR gate has less delay than 4T XOR gate and so it has less power delay product [4]. The parameter, noise margin is better for 3T XOR gate compared to 4T XOR gate. The Boolean equations for 8T full adder design is,

$$Sum = A \oplus B \oplus Cin$$
$$Cout = Cin\,(A \oplus B) + AB$$

The cell having less number of transistors using 3T XOR gate of 8T full adder is shown in Fig.6. By cascading exclusive Oring of 3 inputs, the sum output is obtained. According to the Boolean equation, the carry output is obtained. Using wired OR logic the final sum product is obtained. At most two stage delays are required to obtain the carry output and delays of 2 stages is obtained for sum output. This design is best on delay, power dissipation and threshold loss.

The simulation of 8T Full Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of 8T Full Adder cell is shown in Fig.6 and Fig.7 respectively.

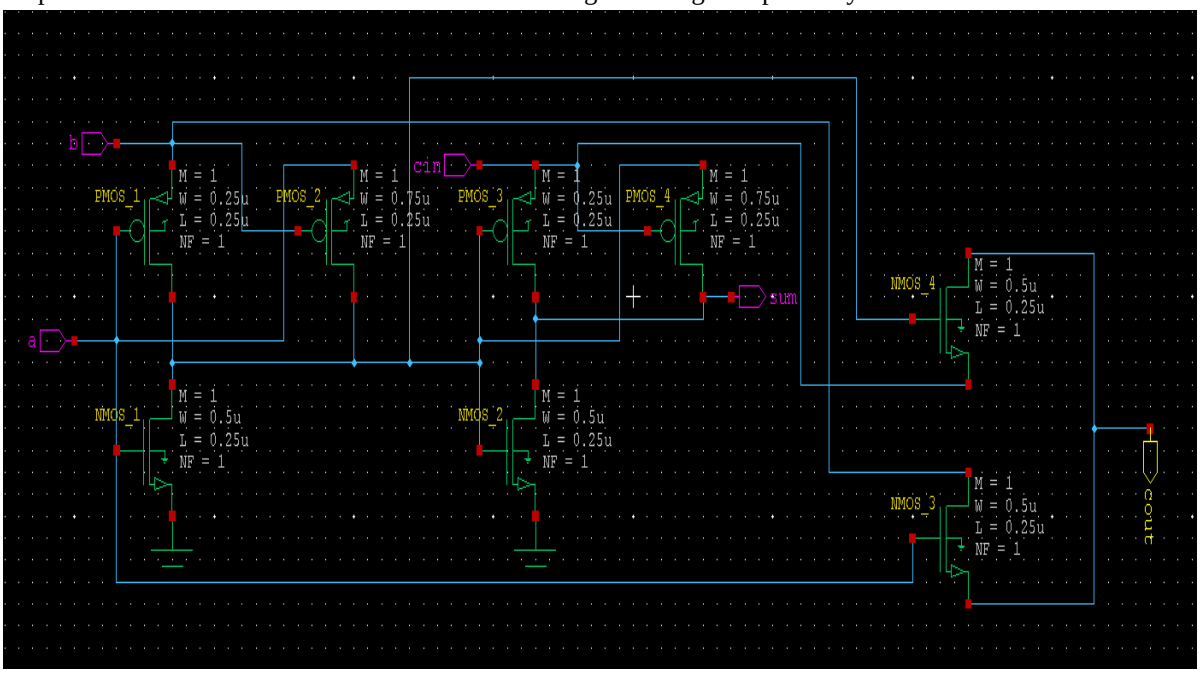

Fig.6. S-edit schematic cell of 8T full adder.

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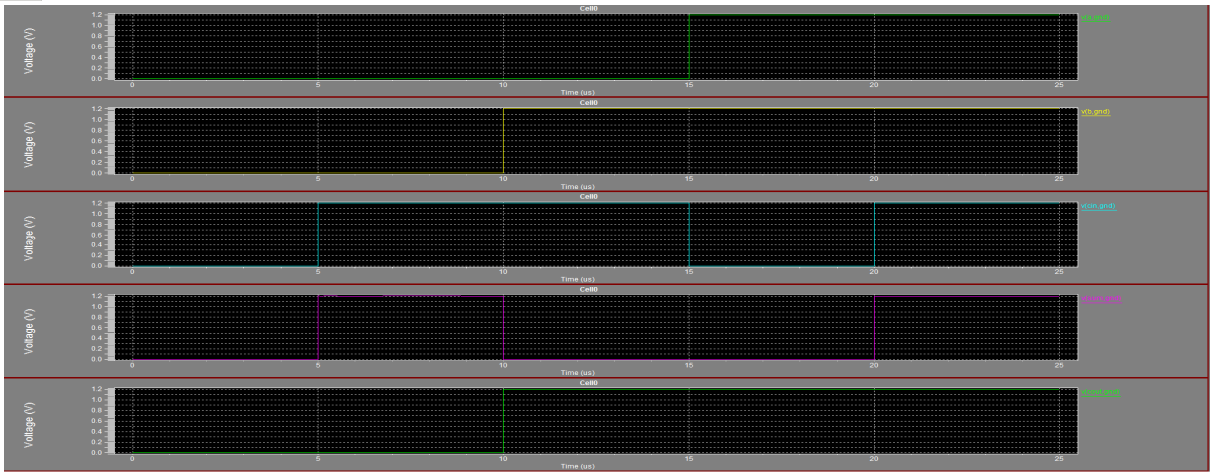

Fig.7. W-edit output waveform of 8T Full Adder.

The simulation of Row bypass multiplier using 8T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in Fig.8 and Fig.9 respectively.

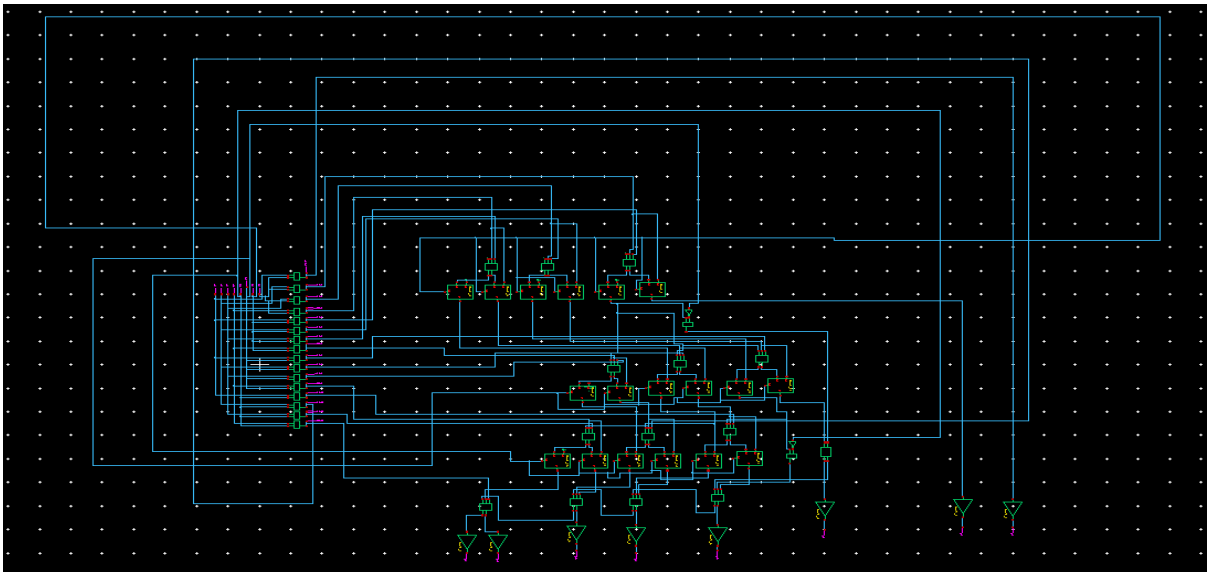

Fig.8. S-edit schematic cell of 8T Row Bypass multiplier.

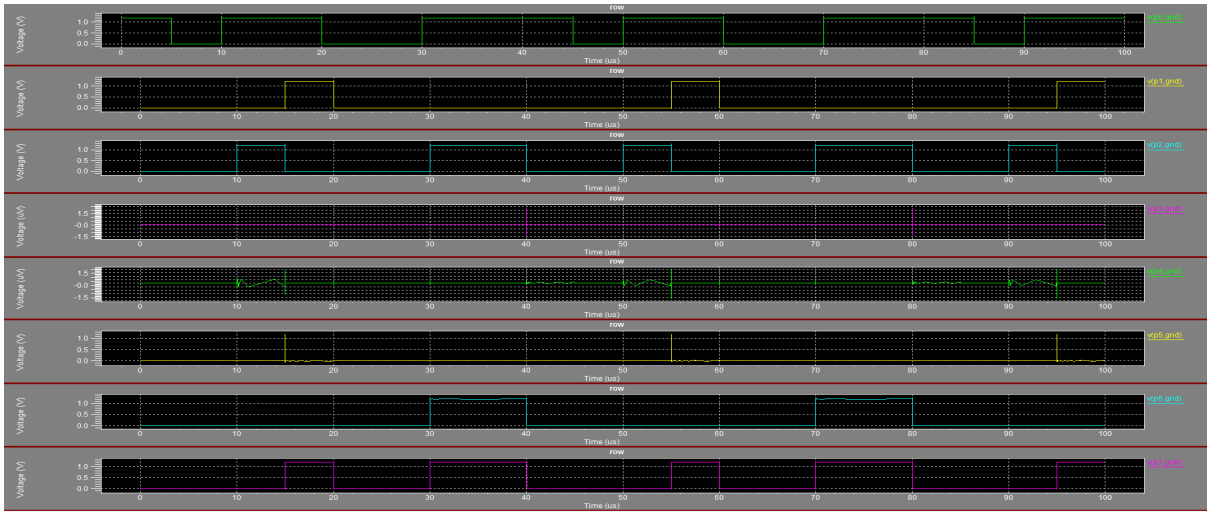

Fig.9 W-edit output waveform of 8T row bypassing multiplier.

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B. 10t Row Bypass Multiplier

Here, 10T is implemented using CMOS logic. In this circuit, VDD and GND connections are given. This design shows the comparative study of advancement over active power leakage current and delay with power supply [5]. Full adder with 10T is presented and the same is compared with the other circuits.

The simulation of 10T Full Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of 10T Full Adder cell is shown in Fig.10 and Fig.11 respectively.

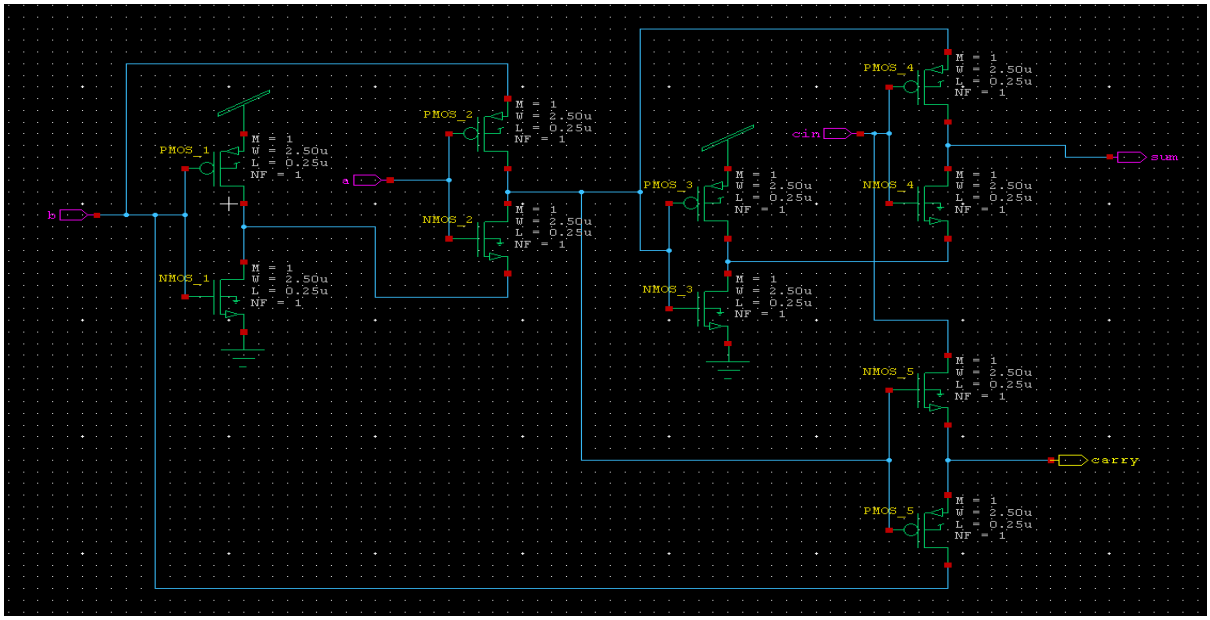

Fig.10 S-edit schematic cell of 10T full adder.

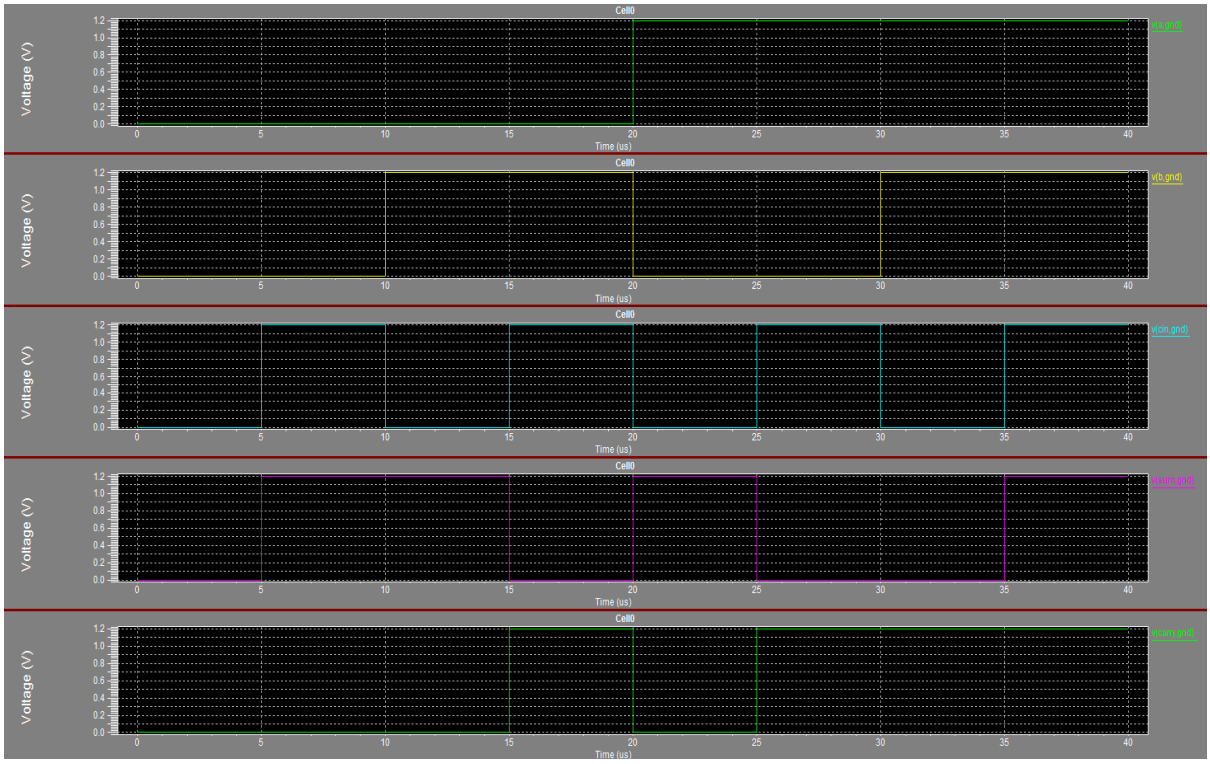

Fig.11 W-edit output waveform of 10T Full adder.

The simulation of Row bypass multiplier using 10T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in Fig.12 and Fig.13 respectively.

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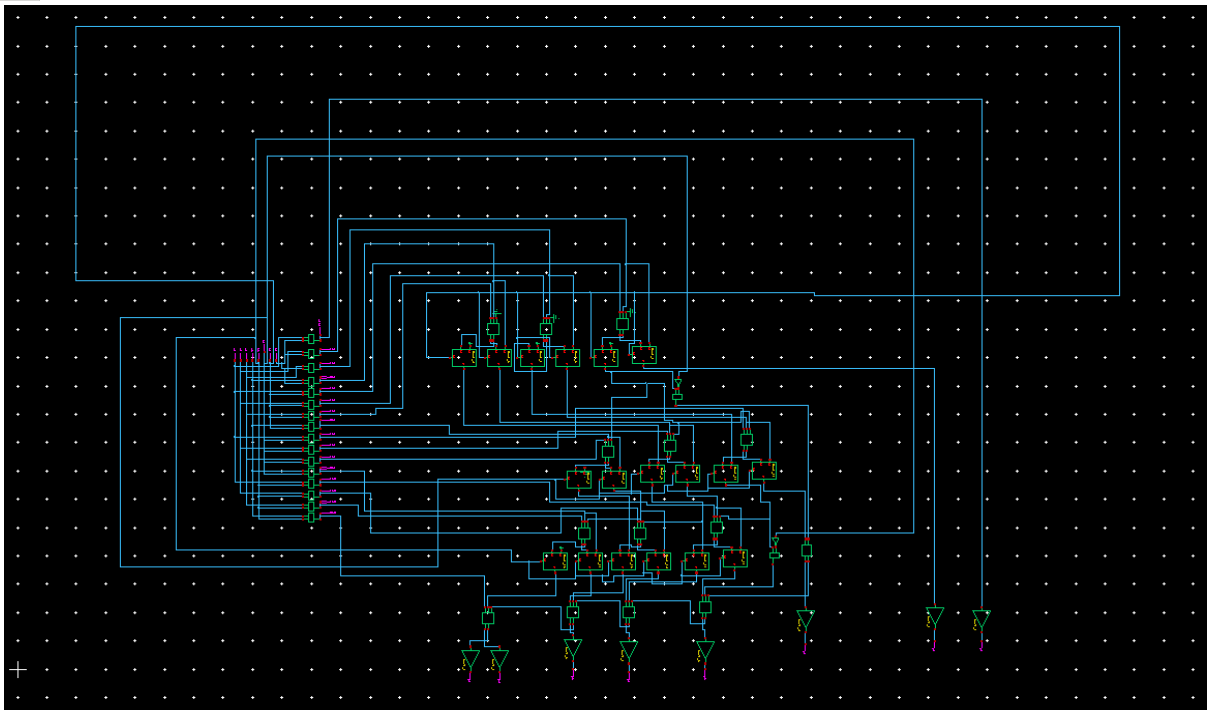

Fig.12 S-edit schematic cell of 10T Row bypass multiplier.

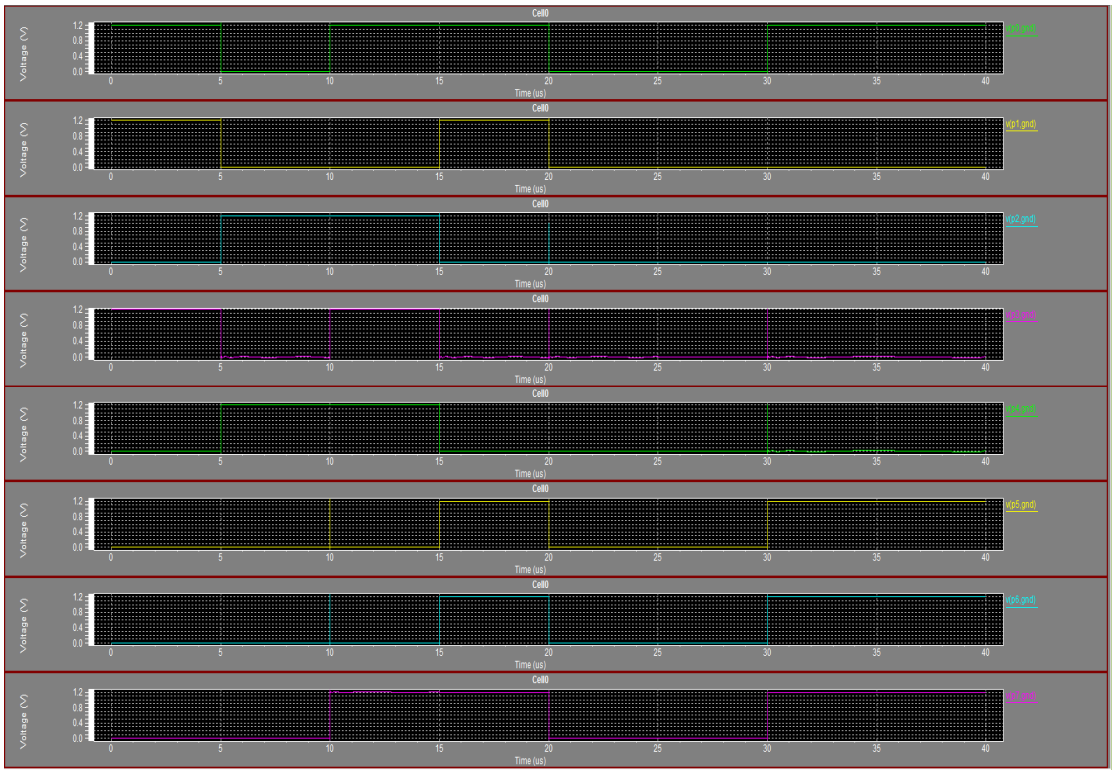

Fig.13 W-edit output waveform of 10T row bypass multiplier.

C. 12t Row Bypass Multiplier

12T is implemented using six multiplexers and 12 transistors. Each multiplexer is implemented by pass- transistor logic with two transistors. In this circuit, there is no VDD or GND connection. There are some paths containing three serried transistors [6]. The delay is increased while producing SUM signal. The size of each transistor in mentioned path should be three times larger to balance the output and optimize the circuit for PDP. Therefore, the area of the circuit is increased.

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The simulation of 12T Full Adder is performed using Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform of 12T Full Adder cell is shown in Fig.14 and Fig.15 respectively.

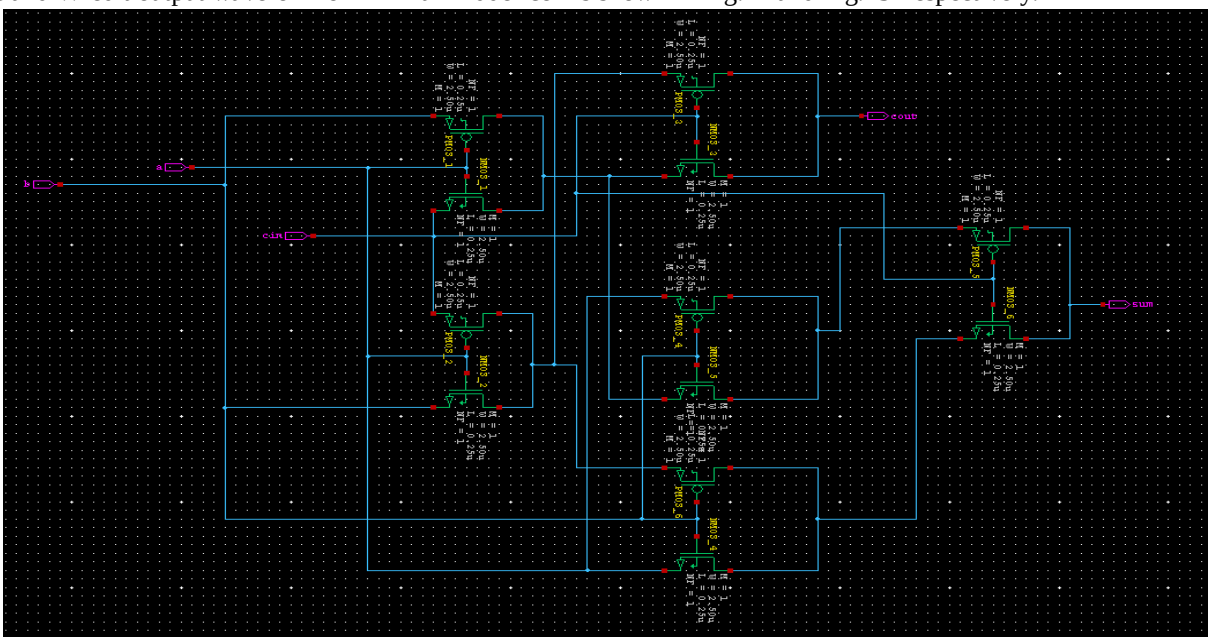

Fig.14 S-edit schematic cell of 12T full adder.

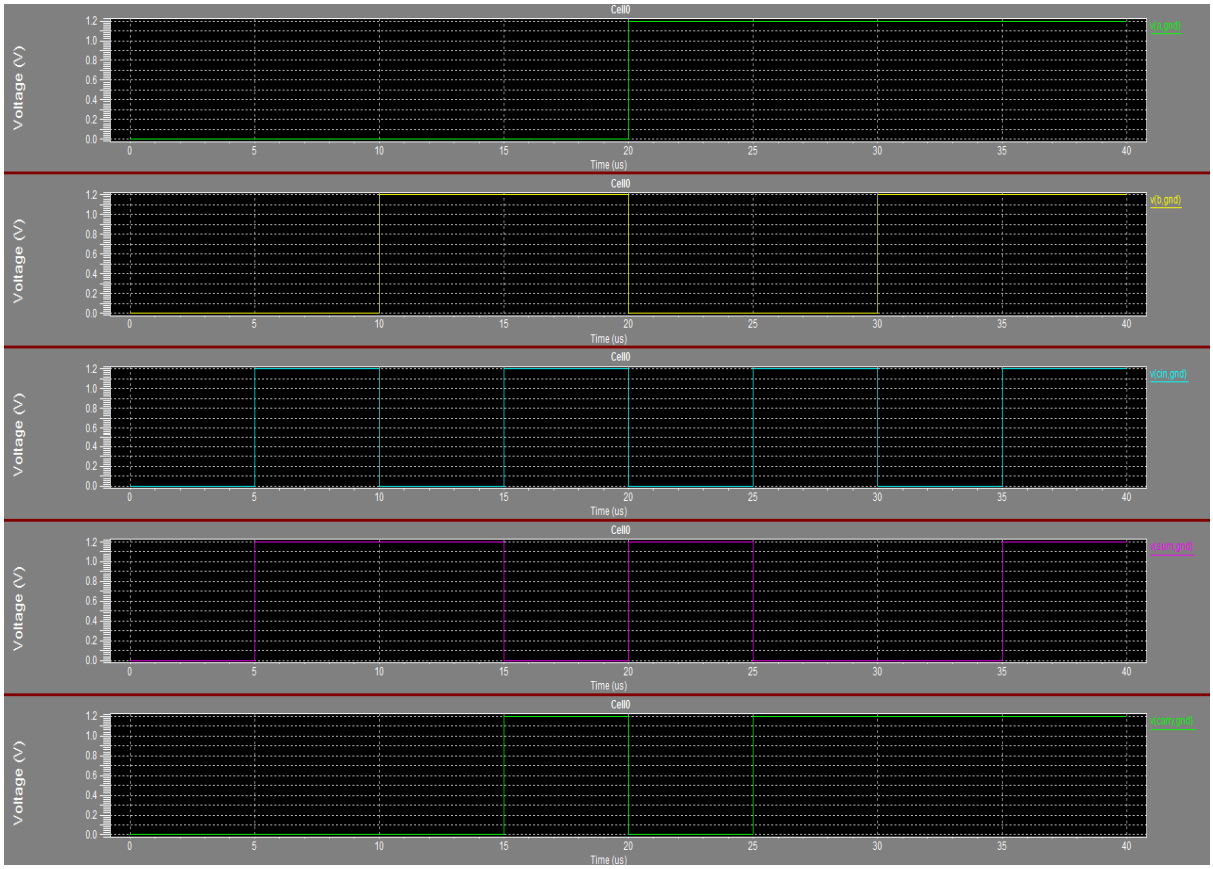

Fig.15. W-edit output waveform of12T Full adder.

The simulation of Row bypass multiplier using 12T Full Adder is performed in Tanner EDA 13.0 using CMOS 130nm technology files. The S-edit schematic and W-edit output waveform is shown in fig.16 and fig.17 respectively

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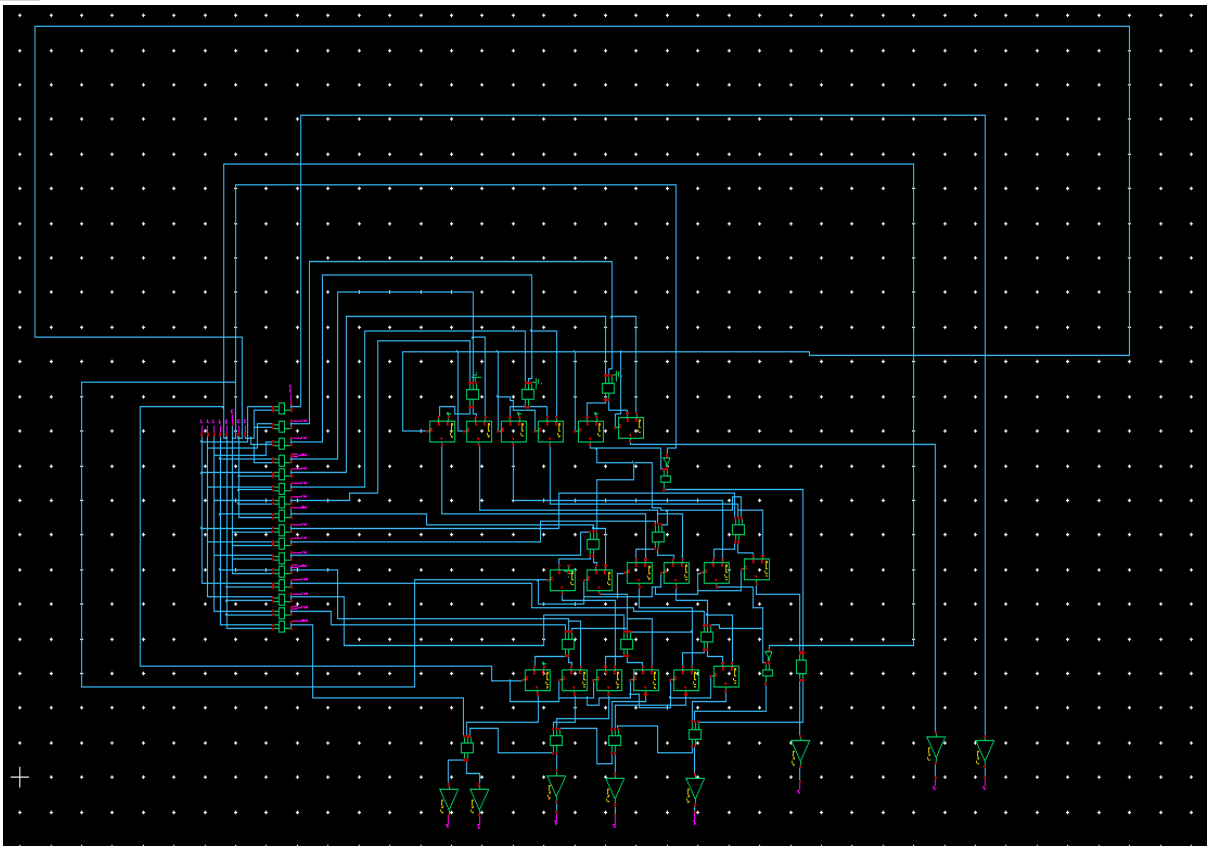

Fig.16 S-edit schematic cell of 12T row bypass ultiplier.

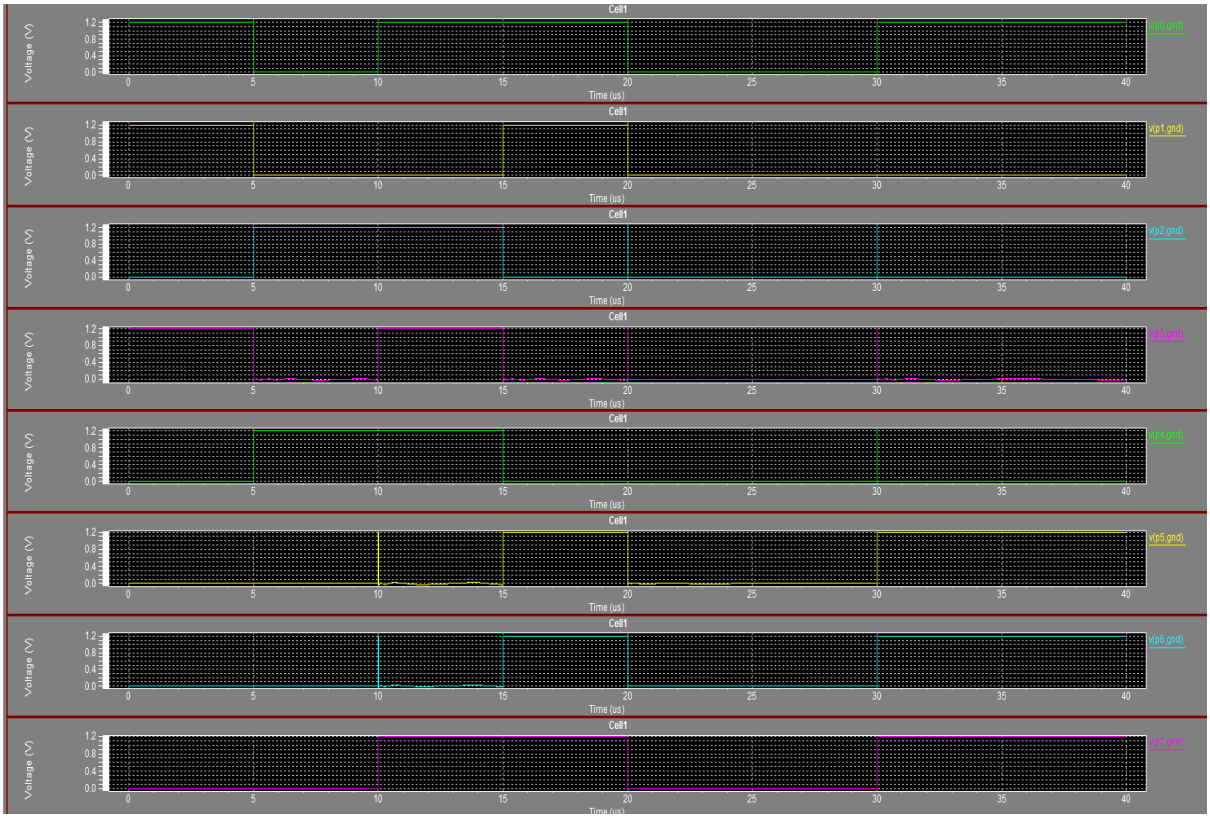

Fig.17 W-edit output waveform of 12T row bypass multiplier.

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IV. SIMULATION RESULTS AND COMPARISON

Simulations are performed using Tanner EDA using 130nm technology nodes. The analysis shows reduced power, delay, PDP, area and transistor count for proposed row bypass multiplier using 8T full adder is compared with row bypass multiplier using 10T, 12T full adders. The simulation results are tabulated in table 1.

TABLE I
SIMULATION RESULT COMPARISON

Parameters	Various Row bypass Multipliers		
	8T	10T	12T
Power (µw)	23.69	38.26	48.25
Delay (µs)	1.6	2.2	2.6
PDP (ps)	37.90	84.17	125.45
No of transistors	594	620	646
Area(µm²)	74.25	387.5	403.75

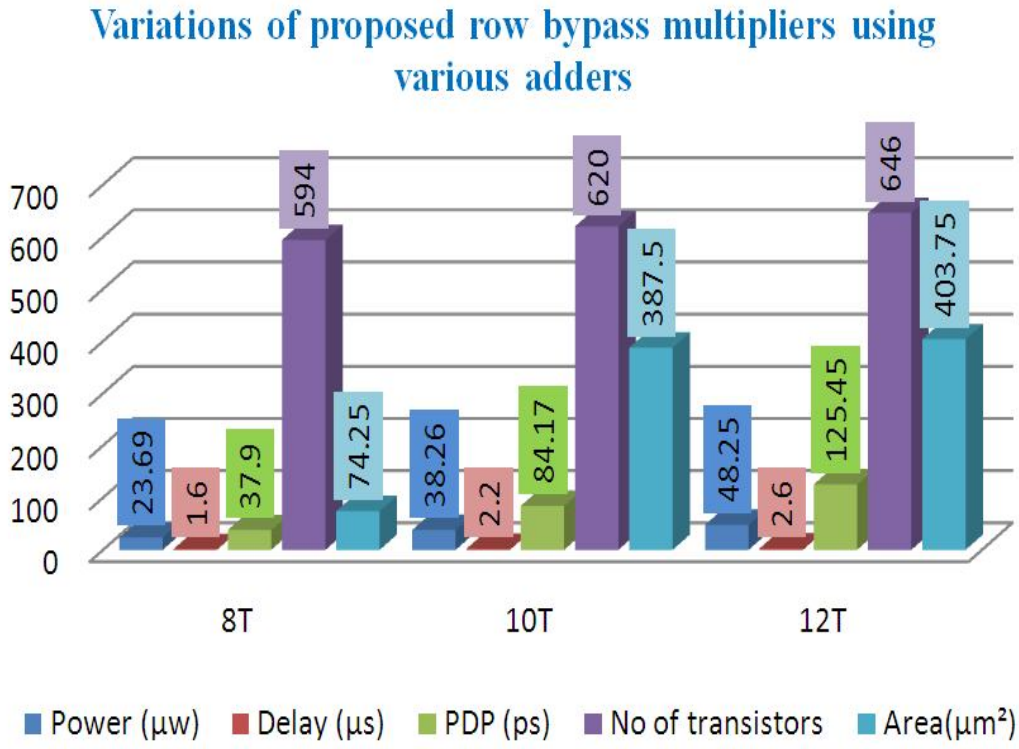

Fig.18 Variations of proposed row bypass multipliers using various adders

V. CONCLUSIONS

Various adders were surveyed based on their architecture involving transistor count. Three full adders namely 8T, 10T and 12T adders are designed. All these full adders are implemented in row bypass multiplier. The proposed design is compared with existing multipliers such as array multiplier, Baugh Wooley multiplier, Braun multiplier and reversible multiplier. Simulations are performed

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using Tanner EDA using 130nm technology nodes. The analysis shows reduced power, area, transistor count, delay and PDP for proposed row bypass multiplier using 8T full adder. The same logic can be implemented in higher architectures in future for desired output.

VI. ACKNOWLEDGMENT

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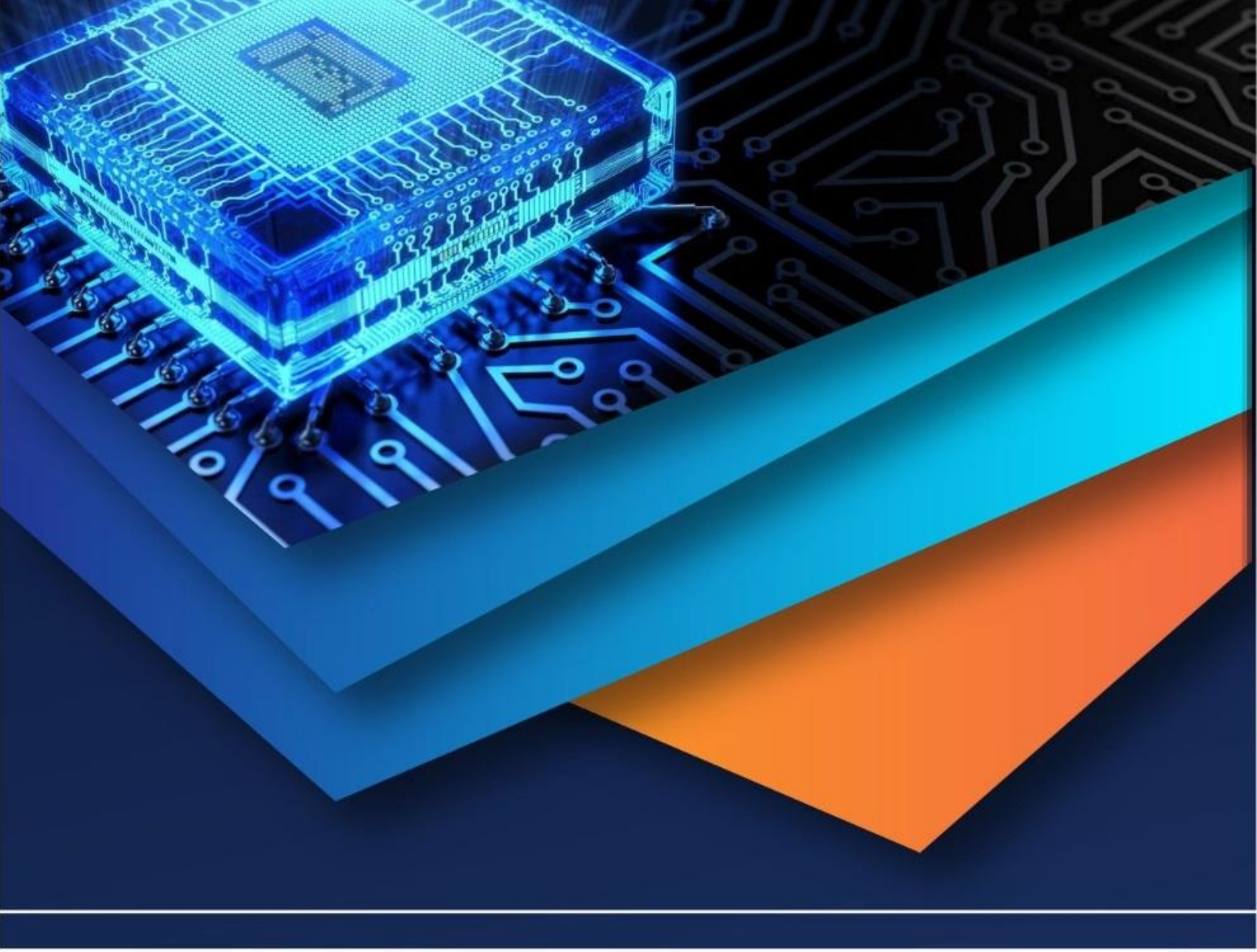

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