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Analysis Of Novel Comparator Design Using Quantum Dot Cellular Automata (QCA).

Abhisekh Banerjee[1], Dipak Kumar Mahato[2], Ratna Chakraborty[3]
[1, 2]*Mtech student in Microelectronics and VLSI Department of Electronics and Communication*
[3]*Professor, Department of Electronics and Communication Institute of Engineering & Management Kolkata-700091, India*

Abstract: ***Quantum Dot Cellular Automata is one of the new approach of nanotechnology that uses quantum dots to design various digital circuits as alternate of conventional transistor based CMOS technology. A QCA is projected as a emerging field in the area of nanotechnology for future IC's in near future .Quantum Dot Cellular Automata has incorporated both the features of quantum mechanics and cellular automata .This paper has demonstrated the design of novel comparator used in A/D converter with help of majority gate based on Quantum Dot Cellular Automata. The calculation of kink energy has determined the robustness of the circuit. The simulation results have been captured and verified using the CAD tool QCA Designer.***
Keywords: QCA, quantum dot, majority gate, QCA designer etc.

I. INTRODUCTION

Due to the rapid development of technology, the conventional CMOS technology faces major physical limits of the technology like excessive power dissipation, short channel effects, tunnelling currents etc in the nano domain. Quantum Dot Cellular Automata is a new approach in the area of nanotechnology that uses quantum dots to design various digital circuits to overcome the physical limitations of the conventional transistor based CMOS technology. A QCA is an array of structures known as quantum dots.[1] Dots are quantum particles confined in three dimensions. QCA technology encodes information by changing the charge configuration instead of transferring information through current and voltage. The advantages of QCA technology include high device density, small circuit size, low power consumption etc[1][2][3].

II. QCA PRELEMINARIES

A. QCA Cell

The fundamental unit of QCA is a cell. A cell looks like a square. Each cell contains four quantum dots at the four corners of a square shaped cell. The two mobile electrons can occupy any of the two quantum dots. The two electrons can quantum mechanically tunnel between the dots but cannot come out from the cell.[2]-[4] Dots are the places where electrons can sit. If a cell is charged with two excess electrons each free to tunnel to any site in the cell, these electrons will try to occupy the furthest
possible site with respect to each other due to mutual columbic repulsion. Therefore, two different cell states exist. A cell state is called its polarisation. The polarisation P=+ 1 is used to represent logic '1' and polarisation P=-'1' is used to represent to logic '0'.[1]-[8][11]. The following fig 1 and fig 2 shows the structure of a QCA cell and two possible minimum energy states of a QCA cell respectively.

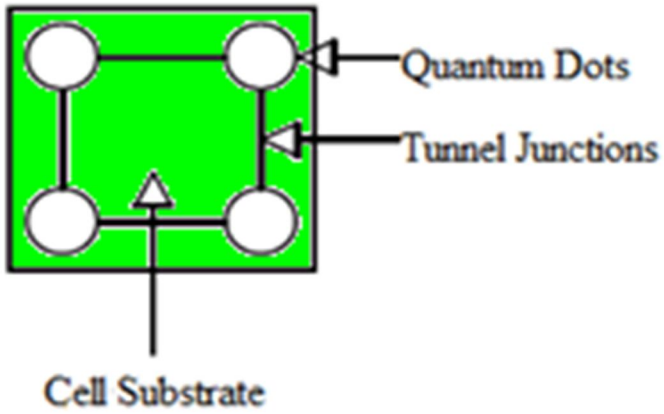
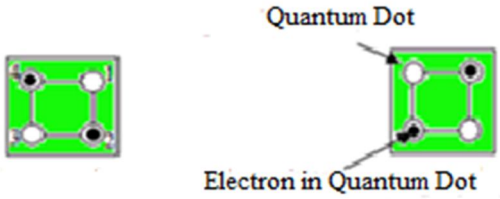


Fig 1. Structure of a QCA cell



Binary '0' Binary '1'
Polarisation=-1 Polarisation=+1

Fig 2. Two possible energy states of a QCA cell

The polarisation P is defined by[1][2]-

$$P = \frac{(p_1+p_3)-(p_2+p_4)}{p_1+p_2+p_3+p_4}$$

B. Majority Gate

A majority gate is composed of five QCA cells. One of the five cells is set as a fixed polarisation and the other two act as two inputs and the remaining one serves as a driver cell. By changing the value of polarisation we can built an AND gate or OR gate. The generalised expression of majority gate is –

$$M(A, B, C) = AB+BC+CA$$

By assigning the value of C as 0, we can easily construct an AND gate

$$M(A, B, 0) = AB$$

By assigning the value of C as 1, we can easily construct an OR gate.

$$M(A, B, 1) = A+B$$

The following fig 3 shows the generalised structure of a 2 input AND & OR gate.

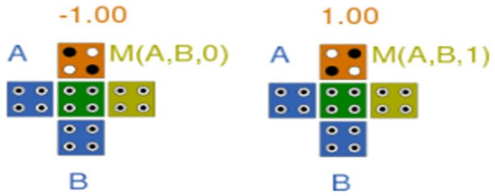


Fig3.Structure of 2 input AND & OR gate.

C. QCA Wire

An array of QCA cells is called a QCA wire. In order to transmit the information from one point to another a QCA wire is used. In QCA wire the way of transfer of information from source end to destination occurs by electrostatic repulsion. The propagation in 90˚ and 45˚ QCA wire is shown in following fig 4 and fig 5.

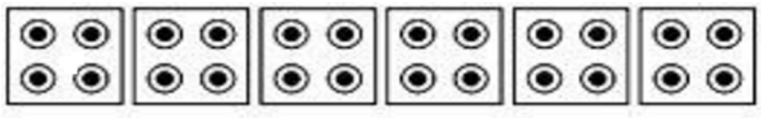


Fig 4. 90˚ QCA wire

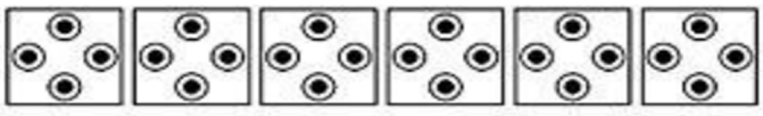


Fig 5. 45˚ QCA wire

D. QCA Clocking

The QCA circuit require clocking not only to control flow of information and synchronisation but actually provides power to run the circuit as there is no external power to drive the cells.[5] Clock is used to push the information from on cell to another. The

adjustment of tunnelling barriers between quantum dots for transfer of electrons between dots occurs by the application of proper clocking. There are mainly four types of clocking namely, switch, hold, release and relax shown in fig 6.

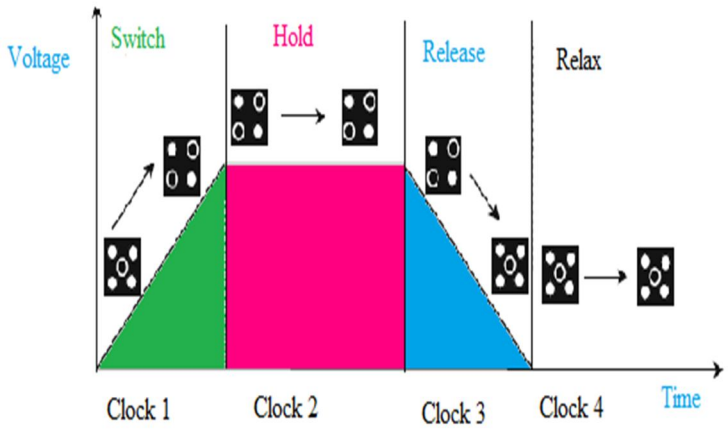


Fig 6. Four stages of Clocking

III. PRESENTATION OF COMPARATOR

A magnitude comparator is a combinational circuit that compares the magnitude of two numbers (A and B) and generates one of the following outputs: A=B, A<B and A>B. The block diagram of a single-bit comparator is shown in fig 7.

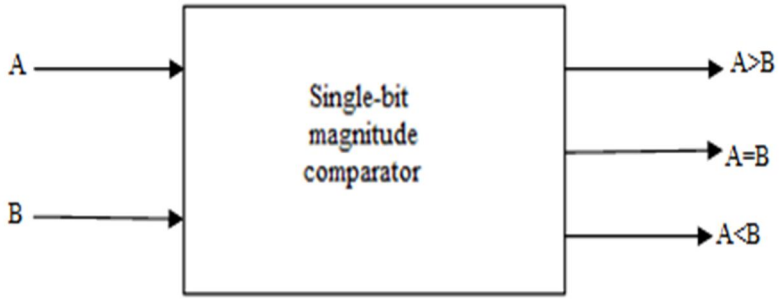


Fig 7. Block diagram of comparator

To implement the magnitude comparator, the EX-NOR gates and AND gates are used. The property of the EX-NOR gate can be used to find whether the two binary digits are equal or not, and the AND gates are used to find whether a binary digit is less than or greater than another bit. The following diagram shows two AND gates, one with A and B as inputs and another with A and B as their inputs. The first AND gate 1 output is 1 if A > B (i.e. A=1 and B=0) and 0 if A < B (i.e. A=0 and B=1).Similarly, the second AND gate 2 output is 1 if A < B(i.e. A=0 an B=1) and 0 if (i.e. A=1 and B=0)[14][15].

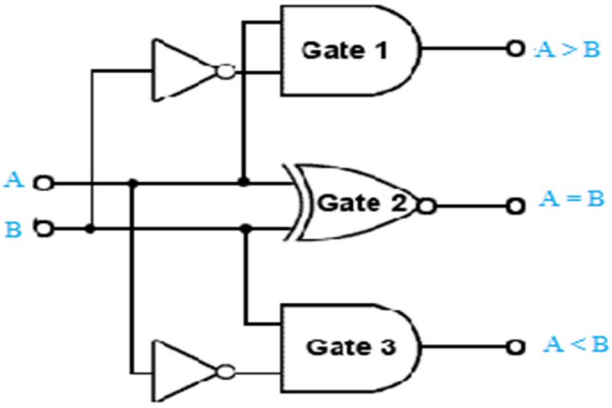


Fig 8. Logic diagram of comparator

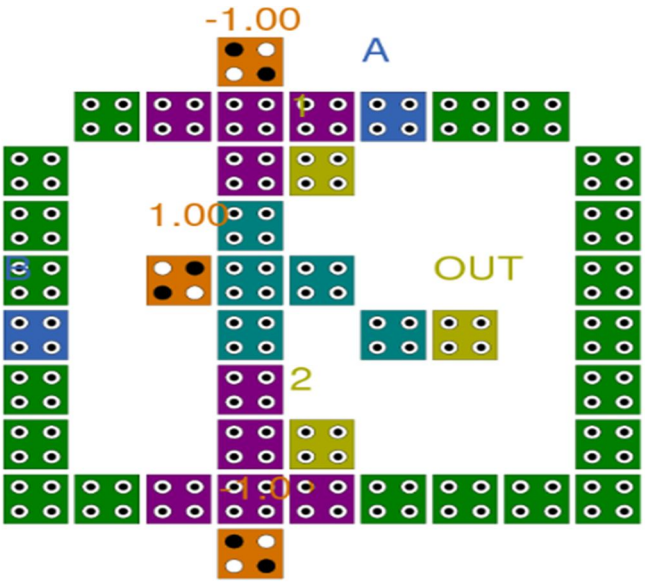


Fig 9. Layout of a comparator.

IV. SIMULATION RESULTS

An optimized design of 1- bit comparator has been presented here. The comparator is built with 42 cells having a approximate area of 0.04 um^2. The proposed circuit has been simulated using the CAD tool QCA Designer[16] with version 2.0.3. The default parameters have been considered for the bistable approximation shown in fig 10 below:-

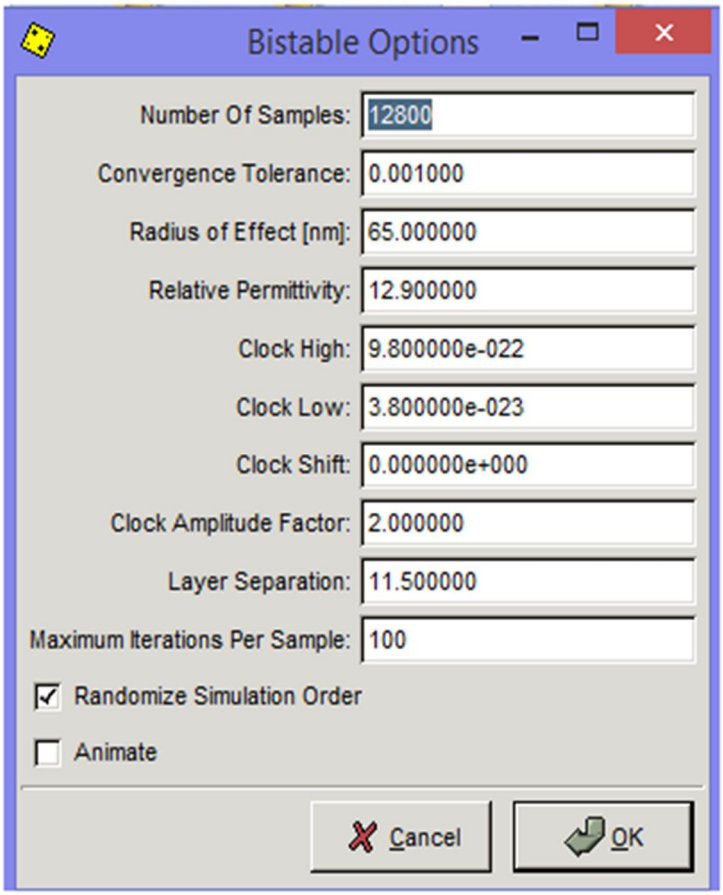


Fig 10. Default parameters for bistable approximation

Comparator is a combinational circuit that determines whether the two inputs are greater, equal or less than each other. The simulation results have been verified and captured for the three conditions of a comparator when A = B, A > B, A < B taking A and B as inputs. The logic function of the comparator[13]-[15]-

$F_{A>B}=A.\overline{B}$

$F_{A=B}=\overline{A}\overline{B}+\overline{A}B$

$F_{A<B}=\overline{A}.B$

The input-output waveforms for the proposed comparator have been shown in figure 11 below:-

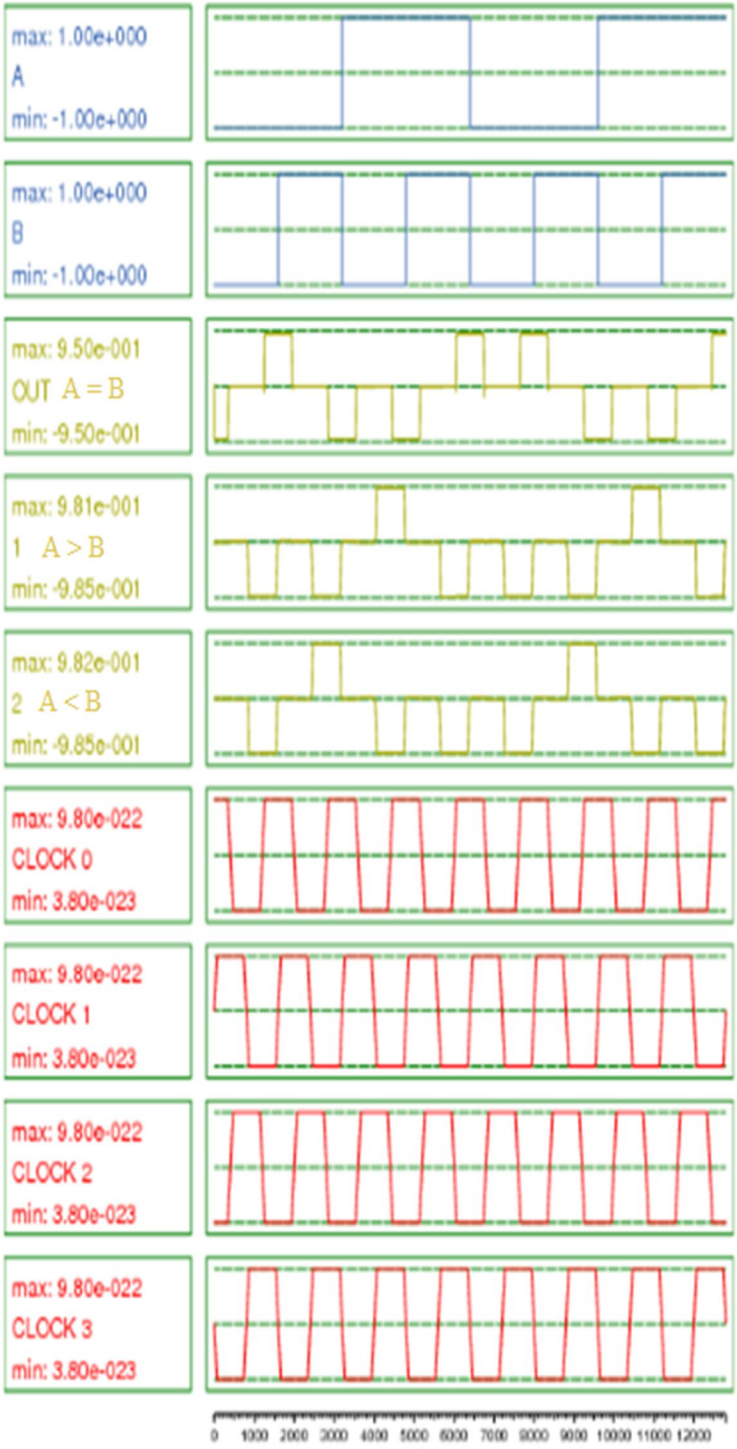


Fig 11. Simulation results of 1 –bit comparator

V. COMPLEXITY OF PROPOSED COMPARATOR

The proposed comparator has been built with 42 cells with area of about 0.04 um^2 and is compared with the previous designs described in table 1.

	CELL COUNT	AREA(um^2)	LATENCY
Conventional Design[13]	117	0.182	1
Conventional Design[14]	95	0.103	1.25
Conventional Design[15]	73	0.06	1
Proposed Design	42	0.04	0.75

Table 1. Comparisons in terms of cell count, area, latency

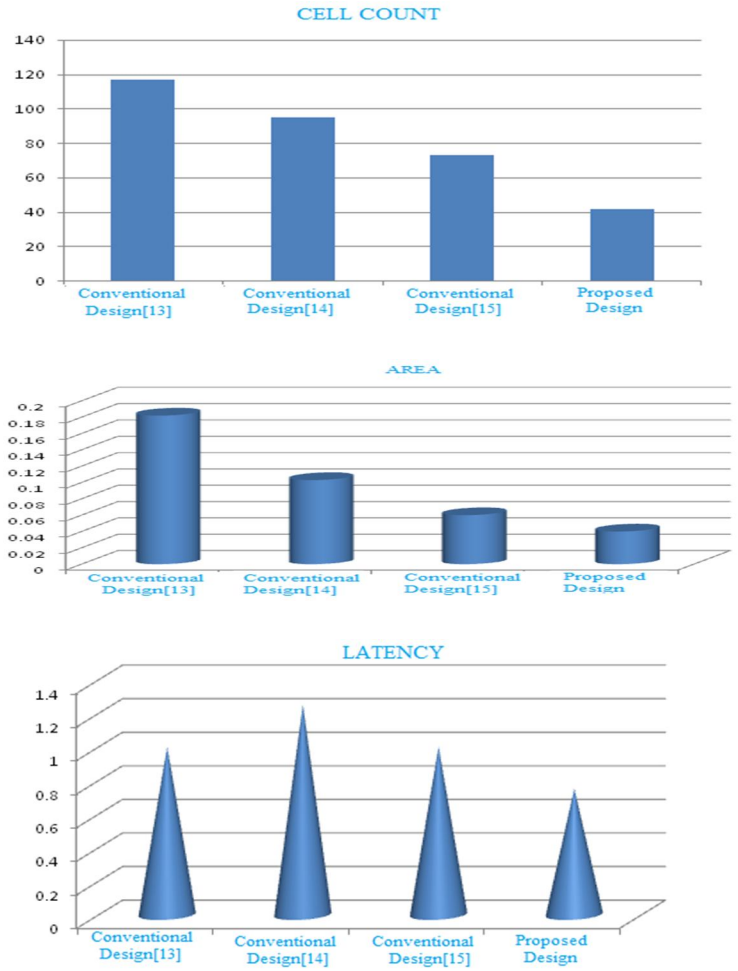


Fig 11. Graphically observation in terms of cell count, area &latency of proposed design with previous design described in [13],[14],[15].

VI. CALCULATION OF KINK ENERGY

The energy difference between two neighbouring or adjacent cells is known as kink energy. Kink energy depends on the spacing between two neighbouring cells but does not depend on the temperature. We have calculated the kink energy using the formula[12]-

$$U=K\frac{Q_1 X Q_2}{r}$$

Where, U is the kink energy, K is a constant given by $K=1/4\pi\varepsilon_0\varepsilon_r=9 \times 10^9$ and Q_1 & Q_2 are the electronic charges and r is the distance between them and r is the distance between them.

$$U=\frac{23.04 \times 10^{-29}}{r} J$$

We have assumed that all the cells are identical and square shaped with length of each side equal to 18 nm. Interspacing distance between the cells is 2 nm.

The kink energy of the output cells has been determined below when the condition of the logic function is A=B. Similarly the kink energy of the other two conditions i.e. A>B & A<B can be found out.

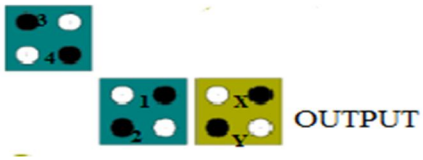


Fig 13: Output cells for calculation of kink energy

Calculation of kink energy for electron 'x'	Calculation of kink energy for electron 'y'
$U_{1=}$ (23.04 X 10^{-29}) /(20 X 10^{-9})=1.152 X 10^{-20} J	$U_{1=}$ (23.04 X 10^{-29}) /(26.90 X 10^{-9})=0.856 X 10^{-20} J
$U_{2=}$ (23.04 X 10^{-29}) /(42.04 X 10^{-9})=0.548 X 10^{-20} J	$U_{2=}$ (23.04 X 10^{-29}) /(38 X 10^{-9})=0.606 X 10^{-20} J
$U_{3=}$ (23.04 X 10^{-29}) /(61.35 X 10^{-9})=0.375 X 10^{-20} J	$U_{3=}$ (23.04 X 10^{-29}) /(69.33 X 10^{-9})=0.332 X 10^{-20} J
$U_{4=}$ (23.04 X 10^{-29}) /(40.04 X 10^{-9})=0.575 X 10^{-20} J	$U_{4=}$ (23.04 X 10^{-29}) /(42.94 X 10^{-9})=0.536 X 10^{-20} J
U_{Total}=2.65 x 10^{-20} J	$U_{Total=}$2.33 x 10^{-20} J

Table 2. Calculation of kink energy

VII. CONCLUSIONS

In this paper, we have designed our proposed comparator design using Quantum Dot Cellular Automata. The QCA circuit design provides a new functional platform for information transmission. In addition, QCA binary logic function and the associated new nanotechnology will provide high speed computing, high density application in comparisons to traditional transistor based CMOS technology. The proposed comparator is superior to previous designs in terms of cell count, area ,and latency. The simulation results have been captured and verified using the QCA Designer tool

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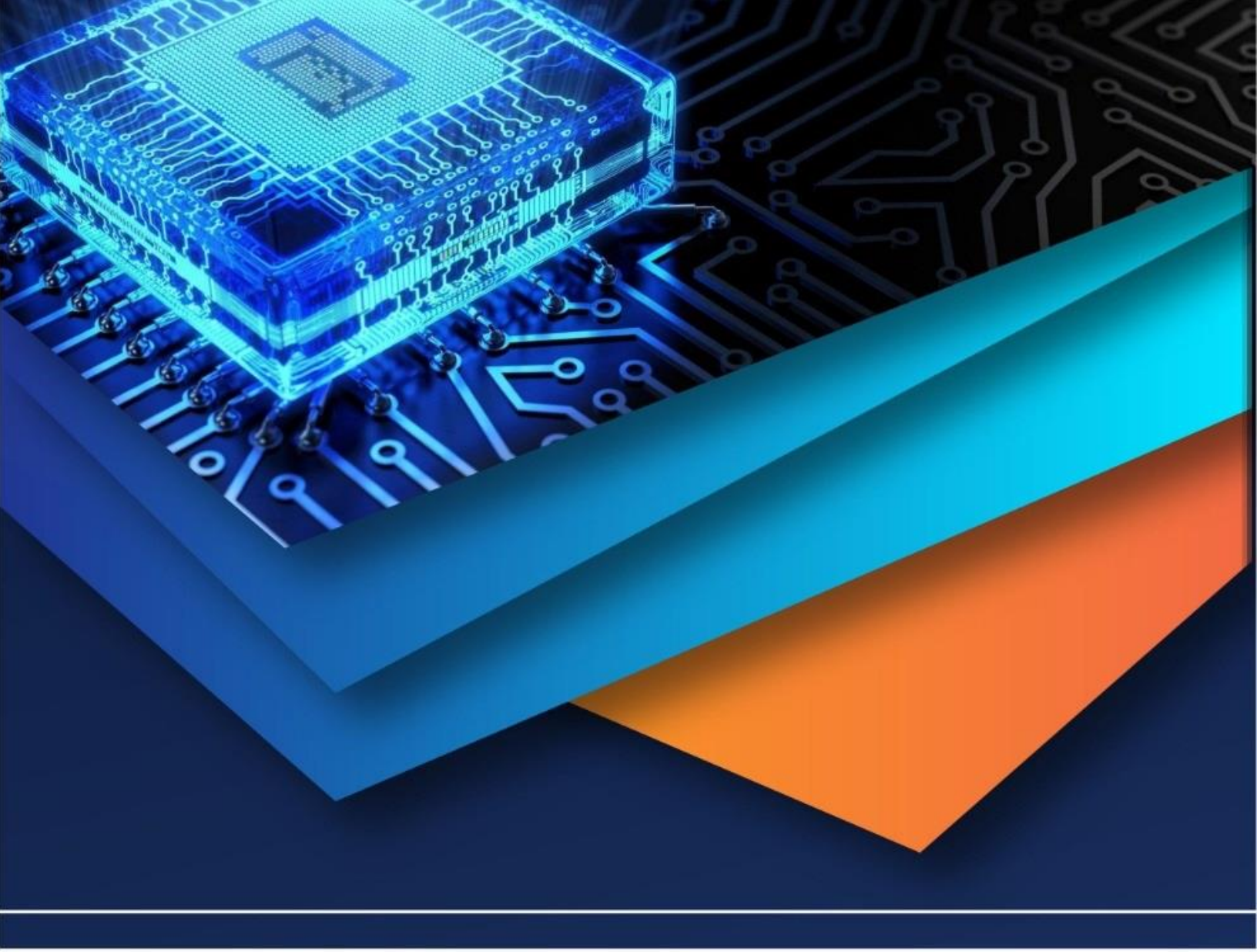

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