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# Simulation and Synthesis of Heterogeneous Adder Using VIVADO

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***Abstract:*** ***An adder is one of the significant hardware blocks in most digital systems such as digital signal processors and microprocessors etc. Over the last few decades, lots of researches have been carried out in order to design an efficient adder circuits in terms of compactness, high speed and low power consumption using Xilinx. We studied different available parallel, synchronous adders and proposed a new adder based on combination of them. In this paper, we proposed a new type of adder architecture known as heterogeneous adder that consists of concatenation of sub-adder (homogeneous adder) of different types. The heterogeneous adder architecture is based on Very High Speed Integrated Circuit Hardware Description Language (VHDL) and compared for their performance using VIVADO 2016.1. Simulation, Synthesis, RTL Implementation is carried out in order to obtain the utilization report and power report summary.***
***Keywords: Adder, Carry Look-Ahead Adder, Ripple Carry Adder, Simulation, VHDL etc.***

## I. INTRODUCTION

Arithmetic operations such as addition, subtraction, multiplication and division are widely used and play an important role in various digital systems such as digital signal processor (DSP) architecture, microprocessor and microcontroller and data process unit. Adders are the logic circuits designed to perform high speed arithmetic operations and are important components in digital systems because of their extensive use in other basic operations such as subtraction, multiplication and division [1].
Efficient low power and area design techniques are required to avoid these problems. Therefore, the area efficient design makes the chip size smaller, reduces cost and weight making the devices handy. Reducing a circuit's average power consumption typically improves the circuit's reliability. This leads to a reduction in cooling requirements, which in turn reduces the packaging and cooling costs [2]. In this paper, heterogeneous adder architecture is proposed and designed with the help of different homogeneous adder architectures. Thereafter, the designed adder is compared with each other in terms of area and power along with the simulation result and implementation using VIVADO 2016.1.

## II. RELATED WORKS

### *A. Homogeneous Adder-Ripple Carry Adder*

Ripple carry adder can be designed by cascading full adder in series i.e. carry from previous full adder is connected as input carry for the next stage. Full adder is a basic building block of Ripple carry adder. Therefore, to design n-bit parallel adder, it requires n full adders. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. The layout of a ripple-carry adder allows fast design time. However, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder [3].

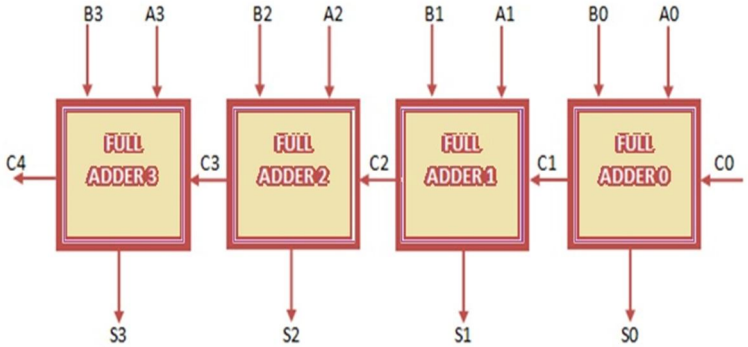


Fig.1 4-Bit Ripple Carry Adder

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In the above Fig. 1, A, B are the 4-bit input, C0 is Carry in and S is the 4-bit output, C4 is Carry out. The remaining C1, C2, C3 are intermediate Carry. They are called signals in VHDL Code.

In our design we use 4 numbers of full adders to design a 4-bit parallel adder. The major limitation of Ripple carry adder is that as the bit length goes on increases, delay also increases. Therefore, Ripple carry adder is not suitable if large number bits are to be added.

The major element that causes delay is carry propagation. Hence it is important to calculate carry delay from input to output. For n-bit Ripple carry adder, delay for carry can be calculated as: -

$$T_C = T_{FA}((A0, B0) \text{ to } C0) + (n-2) \times T_{FA}(\text{Cin to Cout}) + T_{FA}(\text{Cin to Sout } (n-1))$$

where $T_{FA}$ (input to output) represent the delay of full adder on the path between its specified input and output [4].

*B. Homogeneous Adder - Carry Look-Ahead Adder*

A carry look-ahead adder improves speed by reducing the amount of time required to determine carry bits. It is slower than ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry look-ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. The working of this adder can be understood by manipulating Boolean expressions dealing with full adder [5]. The propagate 'Pi' and generate 'Gi' in a full adder is given by

Pi = x_in xor y_in Carry Propagate

Gi = x_in and y_in Carry Generate

Both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay. The new expressions for the output sum and the carryout are given by:

sum = Si = Pi xor Ci -1

carry_out = Ci +1 = Gi + Pi and Ci

These equations show that a carry signal will be generated in two cases:

- ✓ If both bits x_in and y_in are 1
- ✓ If either x_in or y_in is 1 and the carry_in is 1.

Let's apply these equations for a 4-bit adder

C(1) = G(0) + P(0)C(0)

C(2) = G(1) + P(1)C(1) = G(1) + P(1) [G(0) + P(0)C(0)]

= G(1) + P(1)G(0) + P(1)P(0)C( 0)

C(3) = G(2) + P(2)C(2) = G(2) + P(2)G(1) + P(2)P(1)G( 0) + P(2)P(1)P( 0)C(0)

C(4) = G(3) + P(3)C(3) = G(3) + P(3)G(2) + P(3)P(2)G( 1) + P(3)P(2)P( 1)G(0)

+ P(3)P(2)P( 1)P(0)C(0)

Similarly we can write the general expression

Ci + 1 = Gi + PiGi - 1 + PiPi - 1Gi - 2 + ……. PiPi - 1….P2P1G0 + PiPi - 1….P1P0C0.

Carry look-ahead adder's structure can be divided into three parts: the propagate/generate generator, the sum generator, carry generator. The architecture of 4-bit Carry Look-Ahead adder is shown in Fig. 2., the architecture of 4-bit Carry Look-Ahead adder is shown in Fig. 2 [1].

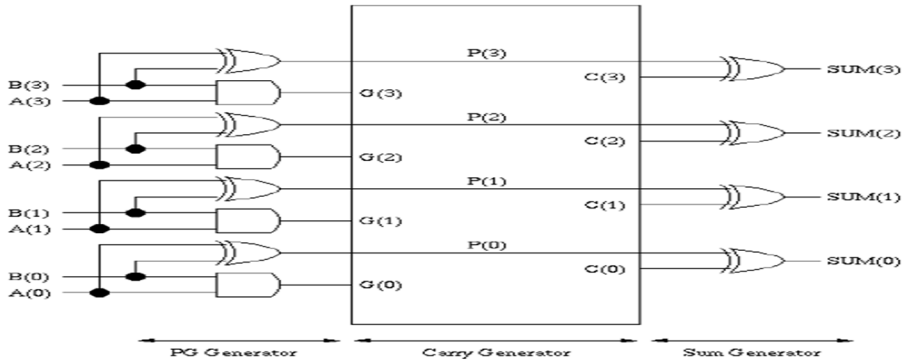


Fig. 2. 4-bit Carry Look Ahead Adder

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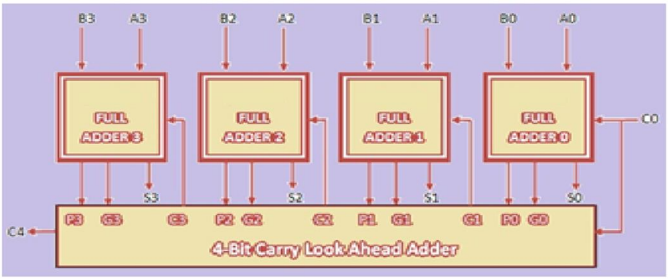


Fig. 3. 4-Bit Carry Look Ahead Adder

*C. 16 Bit Heterogeneous Adder*

16-bit Heterogeneous adder proposed in [6], consists of four sub adders SA1 (Ripple carry adder), SA2 (Carry skip adder), SA3 (Carry select) and SA4 (Carry look ahead adder).Initially, equal bit-width for each sub-adder i.e. 4-bit as shown in Fig. 4 is chosen. All these four sub adders are concatenated to form a 16-bit heterogeneous adder.

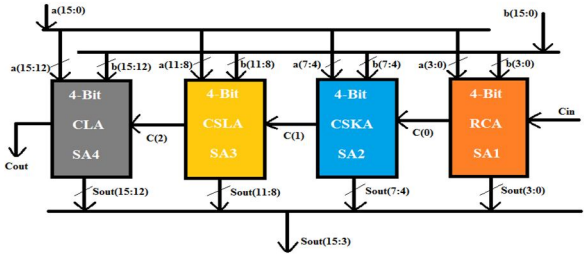


Fig. 4. 16-Bit Heterogeneous Adder

*D. 32-Bit Heterogeneous Adder*

The architecture of a heterogeneous adder includes different types of adder implementations. 32-bit heterogeneous adder proposed in this work consists of four sub adders (SA), 8-bit carry look-ahead adder, 8-bit carry skip adder, 8-bit carry select adder and 8-bit ripple carry adder. Bit size selection for each sub-adder can be done on the basis of requirements (i.e. Area, Speed and Power constraints) of particular application where the design is to be implemented. For example, ripple carry adder cover small area and less power consumption but at the cost of large operation delay whereas carry skip adder gives high speed of operation but at the cost of large area. Therefore in order to optimize adder design as per requirement [7], 32-bit heterogeneous adder is designed as shown in Fig. 5.

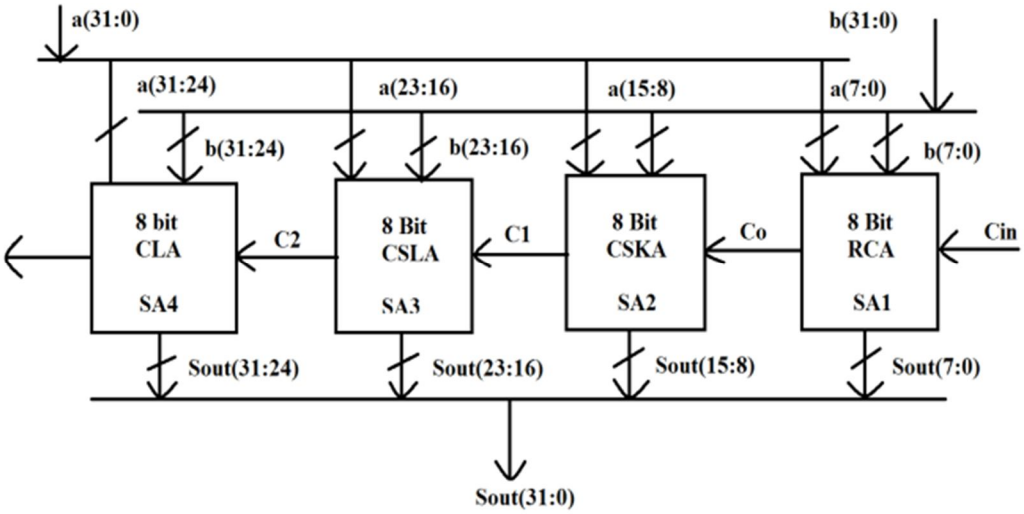


Fig. 5. 32-bit Heterogeneous Adder

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## III. PROPOSED MODEL

The Heterogeneous adder proposed in this paper consists of two sub adders SA1 and SA2. Sub adder (SA1) consists of 4- bit Ripple Carry Adder architecture and Sub adder SA2 consists of 8-bit Carry look-ahead adder architecture as shown in Fig. 6. Both sub adders concatenates to form a heterogeneous adder.

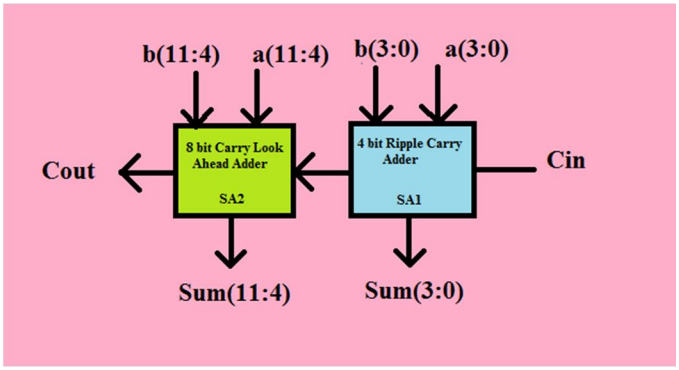


Fig. 6. Heterogeneous Adder of Proposed Model

## IV. RESULTS ANALYSIS

### A. *Ripple Carry Adder (RCA)*

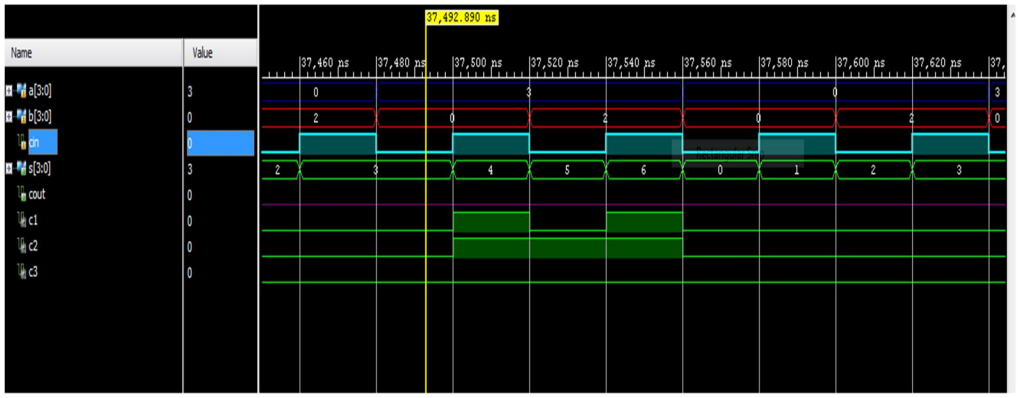


Fig.7 Simulation Results of Ripple Carry Adder

TABLE I
OUTPUT SUMMARY FROM SIMULATION OF RIPPLE CARRY ADDER

| A[3:0] | B[3:0] | Cin | S[3:0] | Cout | Expected Output |
|---|---|---|---|---|---|
| 3 | 0 | 0 | 3 | 0 | 3 |
| 3 | 0 | 1 | 4 | 0 | 4 |
| 3 | 2 | 0 | 5 | 0 | 5 |
| 3 | 2 | 1 | 6 | 0 | 6 |

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*1) Implementation of RCA*

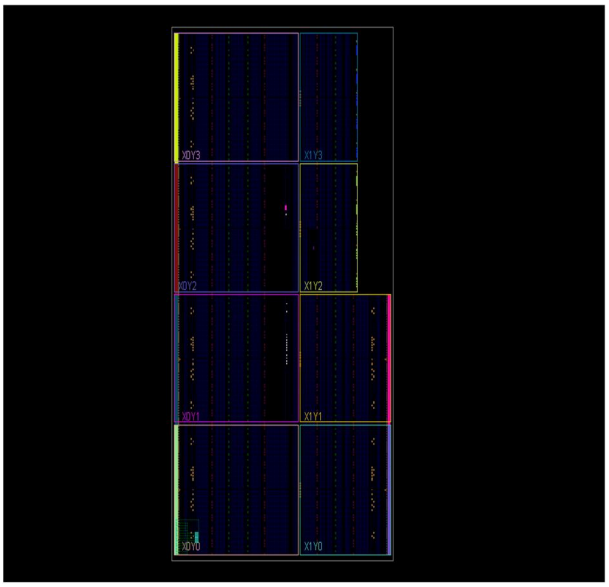

Fig.8 Device Synthesis of Ripple Carry Adder

*2) Synthesis for RCA*

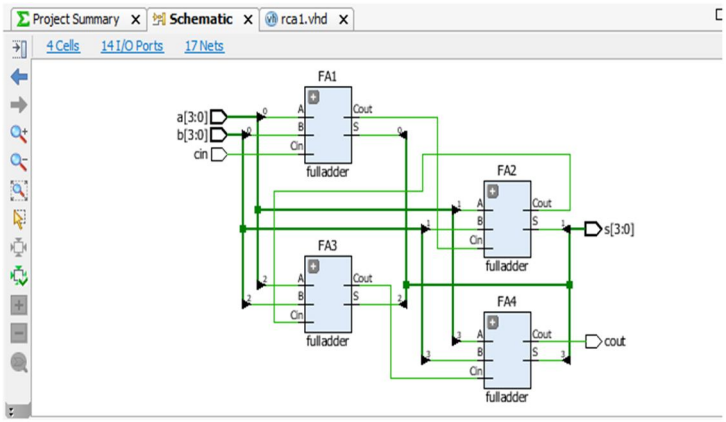


Fig.9 RTL Schematic of Ripple Carry Adder

*B. Design Summary of RCA*

*1) Utilization*

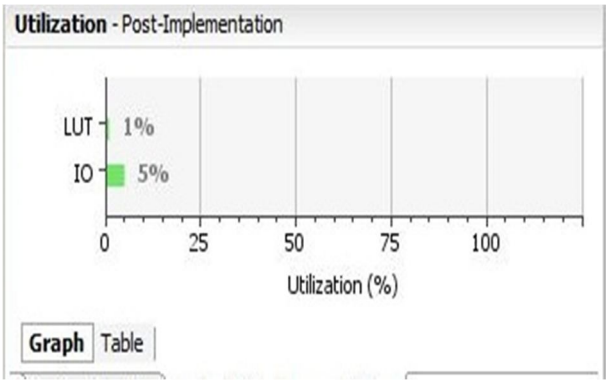


Fig.10 Utilization Graph of RCA

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**Utilization** - Post-Implementation

| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 4 | 41000 | 0.01 |
| IO | 14 | 300 | 4.67 |

Graph **Table**

Fig.11 Utilization Table of RCA

Hierarchy

| Name | Slice LUTs (41000) | Slice (10250) | LUT as Logic (41000) | Bonded IOB (300) |
|---|---|---|---|---|
| rca1 | 4 | 2 | 4 | 14 |

Fig.12 Utilization Report of RCA

*2) Power Summary*

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

| | |
|---|---|
| **Total On-Chip Power:** | **2.959 W** |
| **Junction Temperature:** | **30.6 °C** |
| Thermal Margin: | 54.4 °C (28.7 W) |
| Effective ϑJA: | 1.9 °C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

On-Chip Power

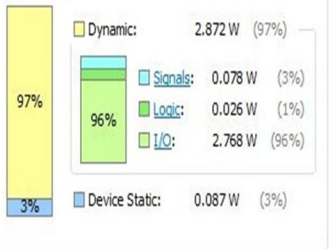


Fig.13 Power Summary of RCA

*C. Carry Look Ahead Adder (CLA)*

*1) Simulation result for CLA*

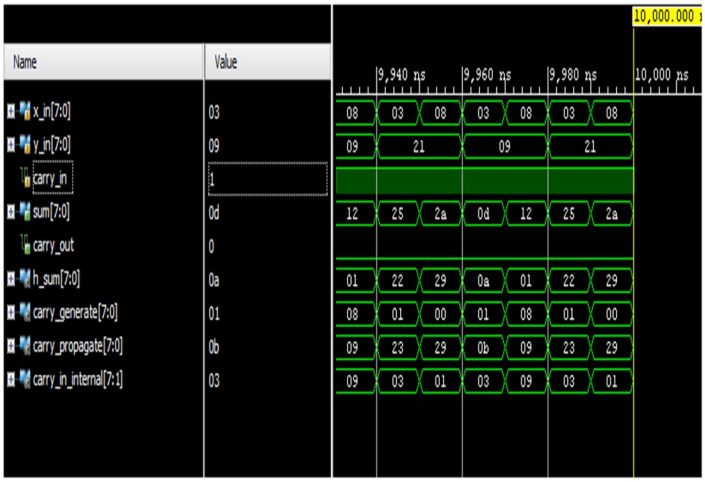


Fig.14 Simulation Results of Carry Look Ahead Adder

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TABLE II
OUTPUT SUMMARY FROM SIMULATION OF CLA

| X_in | Y_in | Carry in | Sum | Carry_out | H_sum | Carry_generate | Carry_propagate | Carry_in_interval |
|---|---|---|---|---|---|---|---|---|
| 3 | 9 | 1 | 0d | 0 | 0a | 01 | 0b | 03 |
| 8 | 21 | 1 | 2a | 0 | 29 | 00 | 29 | 01 |
| 3 | 21 | 1 | 25 | 0 | 22 | 01 | 23 | 03 |
| 8 | 9 | 1 | 12 | 0 | 01 | 08 | 09 | 09 |

*2) Implementation of CLA*

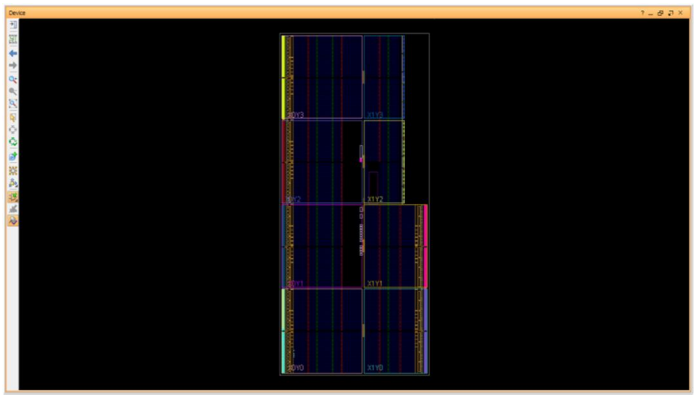

Fig.15 Device Synthesis of Carry Look Ahead Adder

*3) Synthesis of CLA*

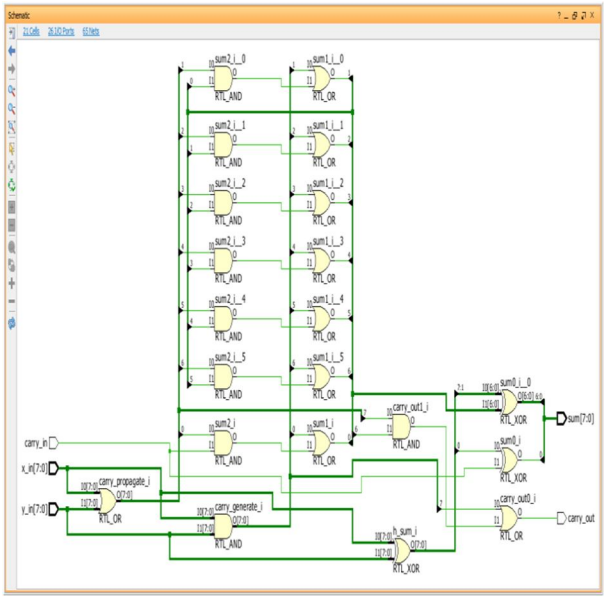

Fig.16 RTL Schematic of Carry Look Ahead Adder

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*D. Design Summary of CLA*

*1) Utilization*

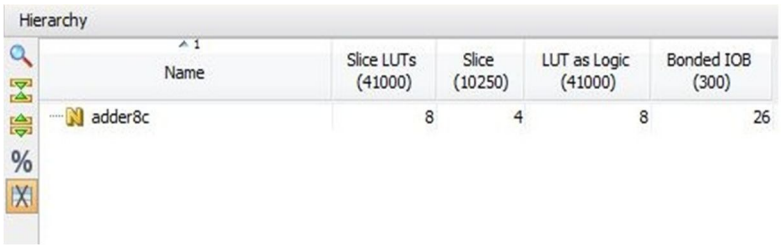


Fig.17 Utilization Report of CLA

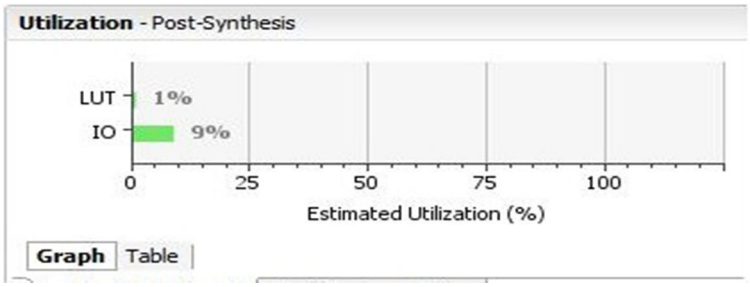


Fig.18 Utilization Graph of CLA

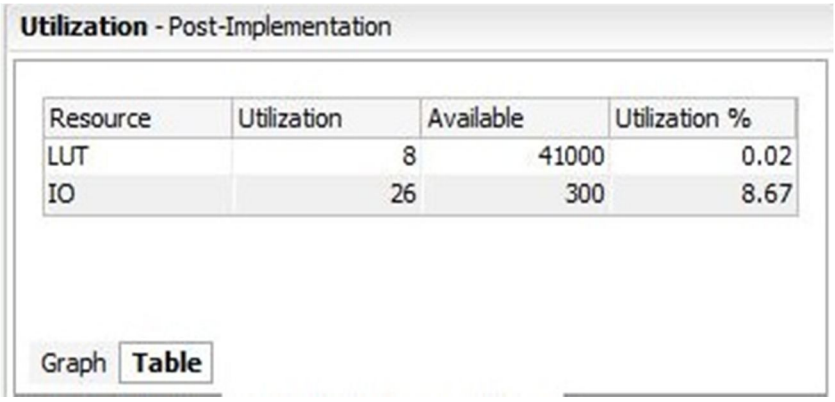


Fig.19 Utilization Table of CLA

*2) Power Summary*

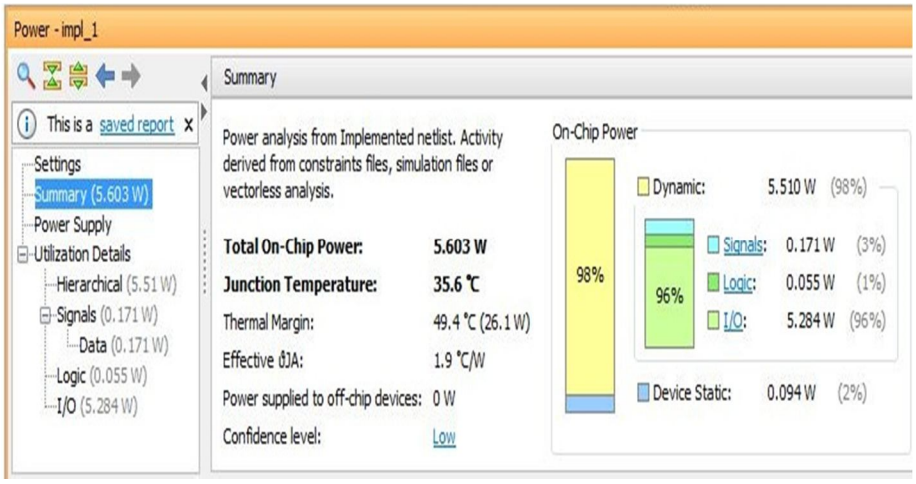


Fig.20 Power Summary of CLA

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*E. Proposed Heterogeneous Adder Model*

*1) Simulation Result for Proposed Model*

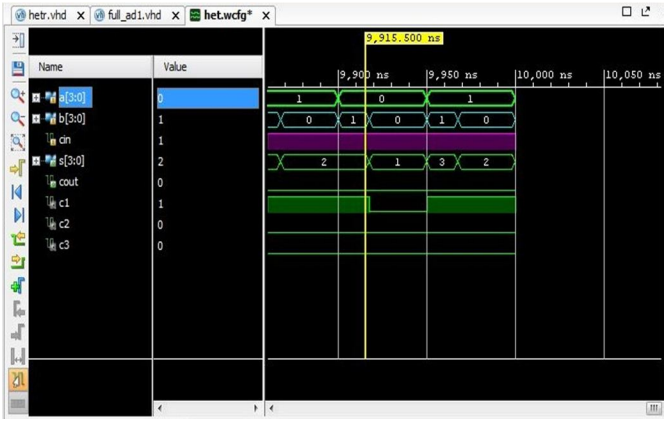


Fig.21 Simulation Results of Proposed Heterogeneous Adder

TABLE III
OUTPUT SUMMARY FROM SIMULATION OF PROPOSED HETEROGENEOUS ADDER

| a[3:0] | b[3:0] | cin | s[3:0] | carry | Expected Output |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 2 | 1 | 2 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 3 | 1 | 3 |

*2) RTL Schematic for Proposed Model*

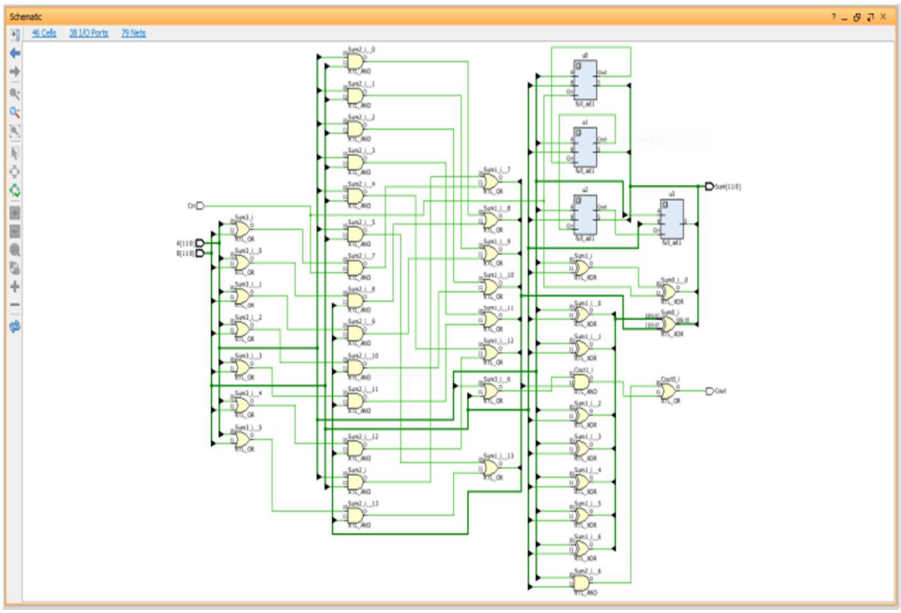


Fig.22 RTL Schematic of Proposed Heterogeneous Adder

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*3) Implementation of Proposed Model*

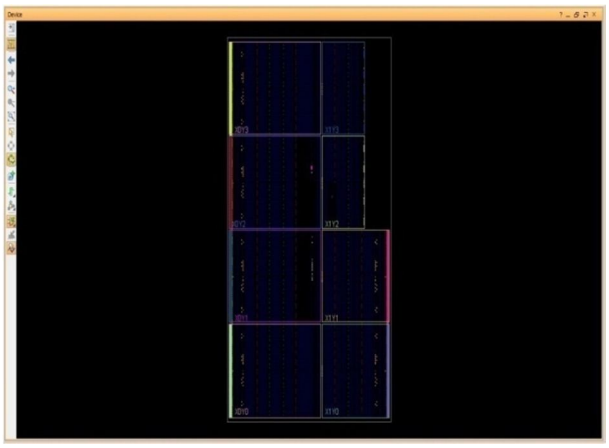

Fig.23 Device Synthesis of Proposed Heterogeneous Adder

*F. Design Summary of Proposed Model*

*1) Utilization*

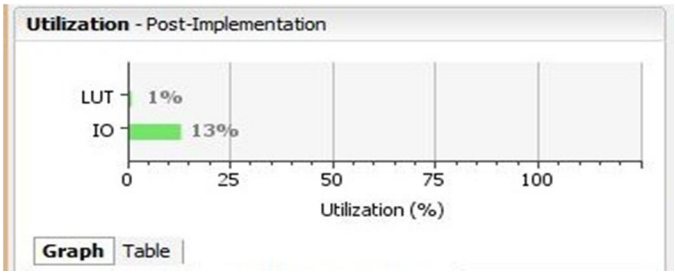


Fig.24 Utilization Graph of Proposed Heterogeneous Adder

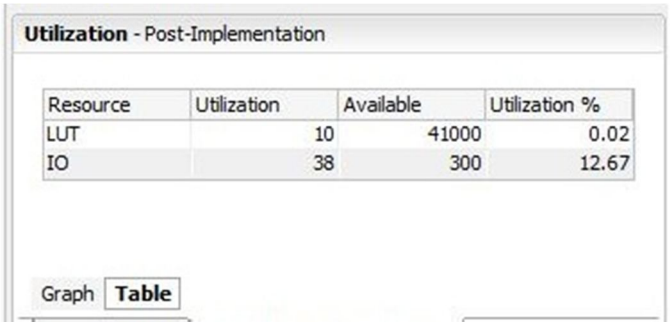


Fig.25 Utilization Table of Proposed Heterogeneous Adder

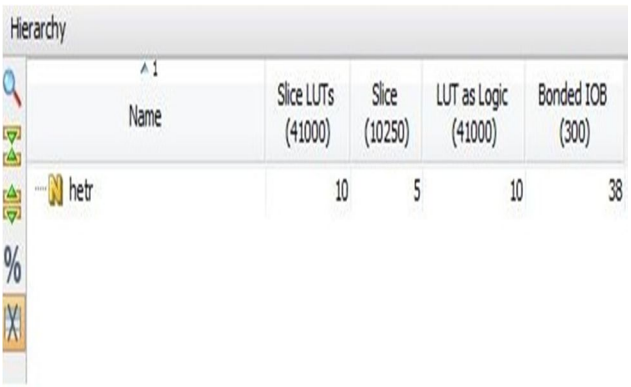


Fig.26 Utilization Report of Proposed Heterogeneous Adder

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*2) Power Summary*

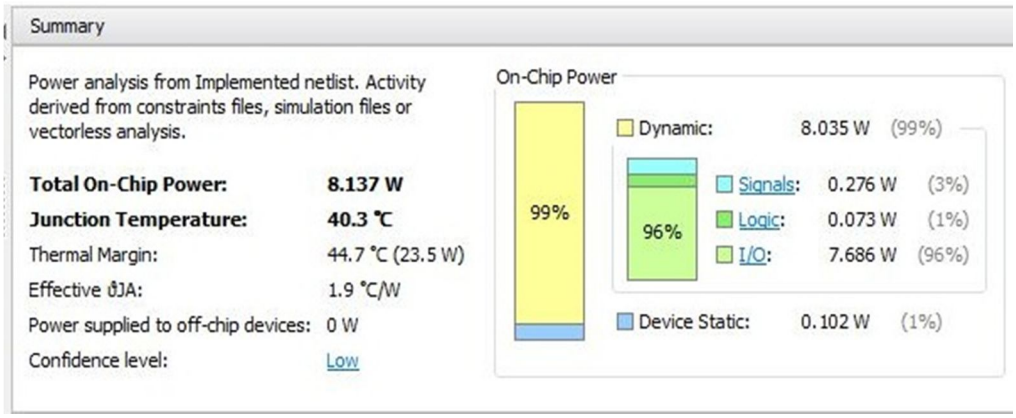


Fig.27 Power Summary of Proposed Heterogeneous Adder

## V. COMPARISON AND TABULATION

TABLE IV

COMPARISON OF UTILISATION BETWEEN 4-BIT RCA, 8-BIT CLA AND PROPOSED HETEROGENEOUS ADDER MODEL

| | 4-Bit RCA | 8-Bit CLA | Proposed Heterogeneous Adder |
|---|---|---|---|
| Slice LUTs(41000) | 4 | 8 | 10 |
| Slice(10250) | 2 | 4 | 5 |
| Bonded IOB(300) | 14 | 26 | 38 |
| Utilisation %(LUT) | 0.01 | 0.02 | 0.02 |
| Utilisation %(IO) | 4.67 | 8.67 | 12.67 |

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TABLE V
COMPARISON TABLE FOR POWER SUMMARY BETWEEN 4-BIT RCA, 8-BIT CLA AND PROPOSED HETEROGENEOUS ADDER MODEL

| | 4-Bit RCA | 8-Bit CLA | Proposed Heterogeneous Adder |
|---|---|---|---|
| Total On-Chip power | 2.959W | 5.603W | 8.137W |
| Junction Temperature | 30.6˚C | 35.6˚C | 40.3˚C |
| Thermal Margin | 54.4˚C(28.7W) | 49.4˚C(26.1W) | 44.7˚C(23.5W) |
| Hierarchial | 2.872 W (97%) | 5.51 W (98%) | 8.035 W (99%) |
| Signal(Data) | 0.078 W (3%) | 0.171W (3%) | 0.276 W (3%) |
| Logic | 0.026 W (1%) | 0.055 W (1%) | 0.073 W (1%) |
| I/O | 2.768 W (96%) | 5.284 W (96%) | 7.686 W (96%) |
| Device Static | 0.087 W (3%) | 0.094 W (2%) | 0.102 W (1%) |

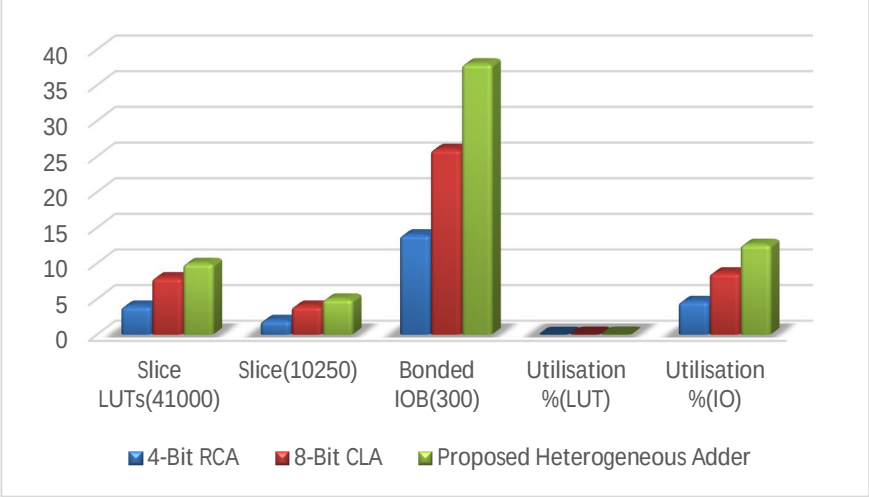


Fig.28 Comparison Graph of Utilization of Adders

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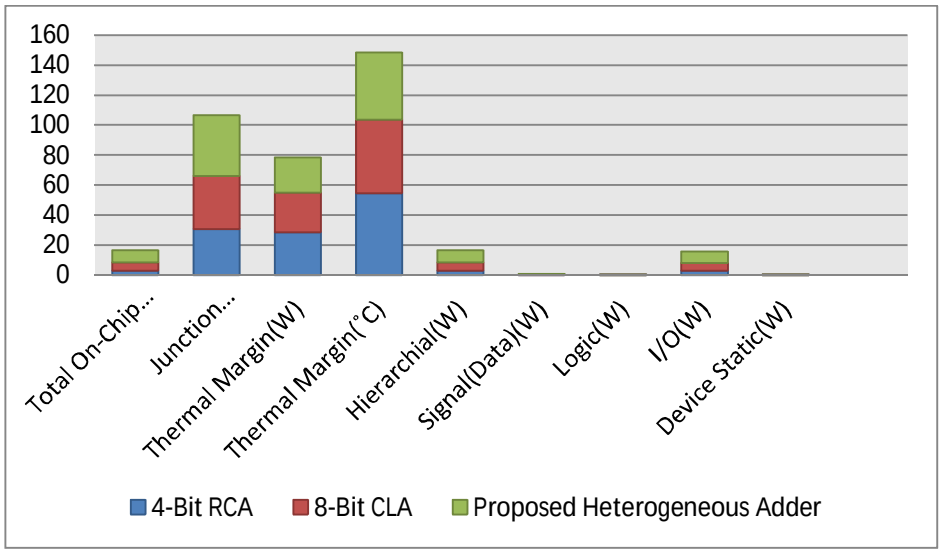


Fig.29 Comparison Graph of Power Consumption in Adders

## VI. CONCLUSION

This paper introduces and validated Heterogeneous Adder using the 4-bit Ripple Carry Adder and 8–bit Carry Look Ahead Adder and its modeling and simulation according to its properties using VHDL in VIVADO 2016.1. This model has less thermal margin under power consumption. It has a minimum area and delay which proves to be an easy solution in improving speed of an adder circuit over other conventional adder circuits in discussion suffering from either occupying more number of slices or look up table per unit cell or having highest minimum propagation delay owing to either critical carry path for some power(in mW). The respective utilization and power summary of the proposed model and the 4-Bit Ripple Carry adder and 8-Bit Carry Look Ahead Adder was found and compared using bar-graph.

## VII. ACKNOWLEDGMENTS

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## REFERENCES

[1] Rajender Kumar, Sandeep Dahiya, "Performance Analysis of Different Bit Carry Look Ahead Adder Using VHDL Environment," International Journal of Engineering Science and Innovative Technology(IJESIT), vol. 2, no. 4, July 2013.

[2] Aishwarya T, Arvind Prasad L, Nikith G S, Ahish S, "FPGA Implementation of Optimized Heterogeneous Adder for DSP Applications," International Journal of Engineering Research & Technology (IJERT), vol. 3, no. 5, May 2014.

[3] Nagaraj Y, Shrinivas K, Veeresh K, Veeresh A, Madhu Patil and Dr. Chirag Sharma, "FPGA implementation of different adder architectures," International Journal of Emerging Technology and Advanced Engineering, vol. 2, no. 8, pp. 362-364, August 2012.

[4] Raminder Preet Pal Singh, Ashish Chaturvedi, Onkar Singh, "Trade-offs in Designing High-Performance Digital Adder based on Heterogeneous Architecture," International Journal of Computer Applications (0975 – 8887), vol. 56, no. 13, October 2012.

[5] Y. T. Pai and Y. K. Chen, "The fastest carry-lookahead adder," Proceedings of the second IEEE International Workshop on Electronic Design Test and Applications (DELTA), 2004.

[6] K.Gowthami, Y.Yamini Devi, "Design of 16-bit Heterogeneous Adder Architectures Using Different Homogeneous Adders," International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 5, no. 10, October 2016.

[7] Neha Agarwal and Satyajit Anand, "Logical Effort to Study the Performance of 32-bit Heterogeneous Adder," International Journal of Computer Applications, vol. 65-No.16, March 2013.

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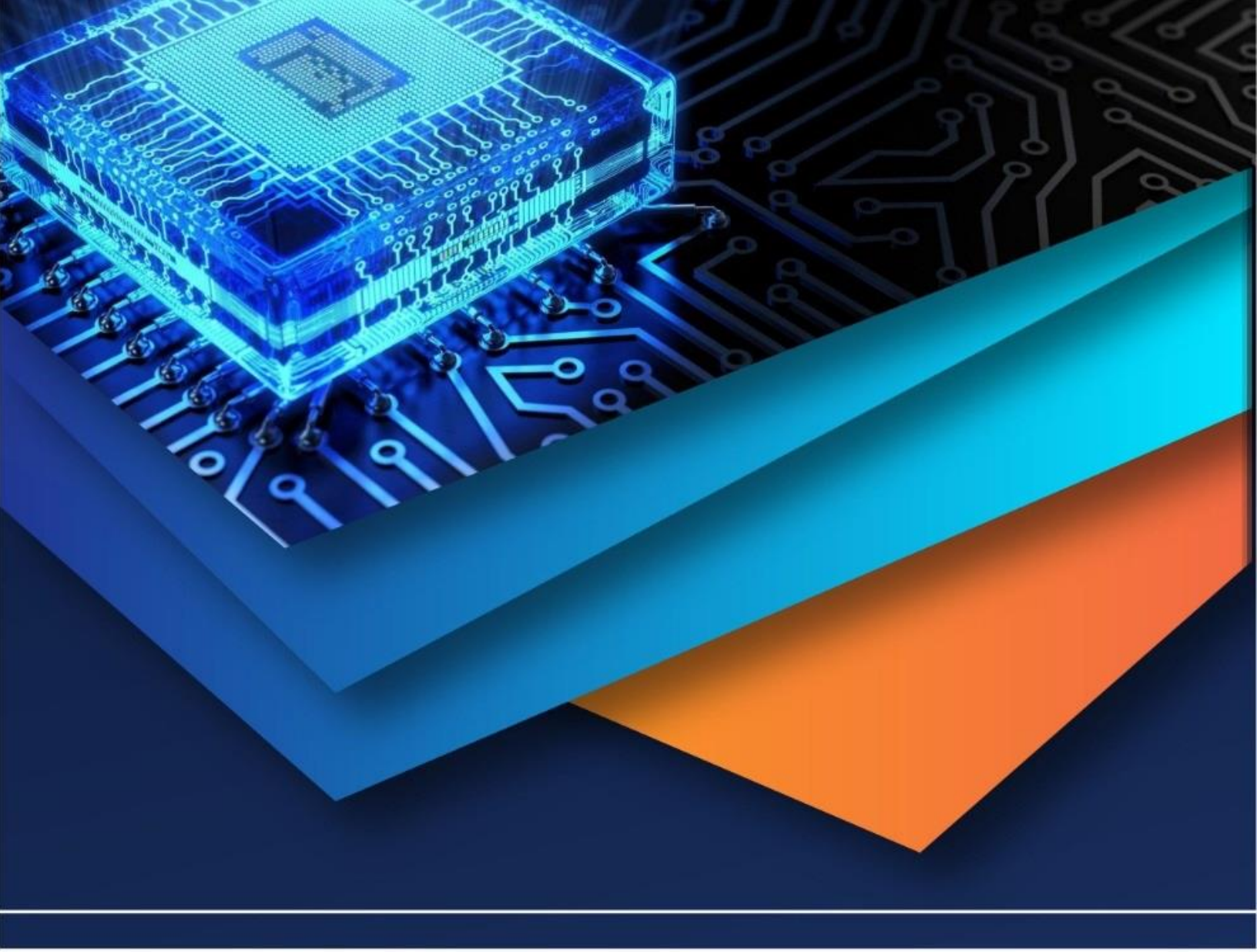

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