iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 6 **Issue:** III **Month of publication:** March 2018

DOI: http://doi.org/10.22214/ijraset.2018.3276

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue III, March 2018- Available at www.ijraset.com

Performance Evaluation of Buffer under Load Balancing in High Speed Network

Arpit Mishra[1], Sanjay Kumar Yadav[2]
[1, 2] *Department of Computer Science and Information Technology, Sam Higginbottom University of Agriculture, Technology and Sciences, Allahabad*

Abstract: ***Need of more bandwidth is increasing day by day. To fulfill this demand high speed fiber optical communication can be used. In fiber optic networks buffering is a phenomenon, by which except one other contending packets are stored in fiber delay lines. In network due to random connections among the nodes, path traverses from a source node to destination node varies, thus cost also varies. More over intermediate nodes also affect the performance of the networks. Therefore in past study both buffering and deflection routing for load balancing was suggested to tackle contention problem. In this work it is shown that in network deflection will increase un-necessary traffic in the networks and contention problem become more severe. Therefore, it is concluded that buffering of contending packets in better choice.***
Keywords: OPS ; Buffering ; Networks

I. INTRODUCTION

The use of internet and data centric application is increasing at a rapid pace. To cater to such demand optical packet switching in optical network will play vital role. The Fig. 1 illustrates the generic design of the network. The structure of the network comprises client and core networks. We also have the edge routers that functions as an interface between these two networks. The position of the above mentioned edge routers are at the network cloud fringe. In terms of nature, as of now, both of these routers are electronic. One drawback with the electronic switches/routers is their quite slow speed [1-4]. Hence, these electronic routers are not able to deal with data of high rate. Due to this limitation, we introduced optical networks. The basic problem with the optical network lies with the structure of the switch/routers which is capable of functioning properly at the high data rates [5]. We can group them as 'all'-optical or photonic switches. In the case of first group, we assume that the propagation and the processing of data in optical domain [6]. As of now, because of the inaccessibility of the optical RAMs, it is not possible to have technical feasibility of all-optical switches. If we talk about second mode (photonic), information stays in the optical domain and does not have any O/E and E/O change at the intermediate nodes, yet control operation is carried out in electronic space. The second mode gives fast, format straightforwardness, productivity and adaptability in the setup because of the switching operation in physical layer [6].

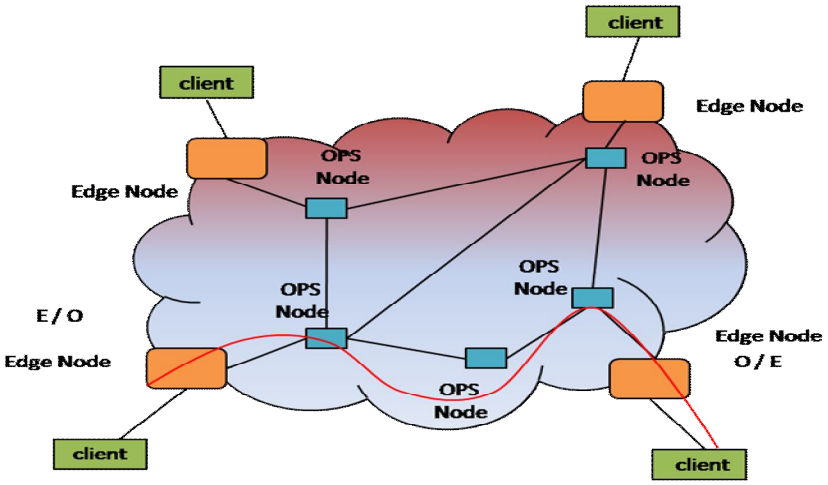


Fig. 1: Generic layout of the OPS system

Data, in optical communication, is produced with the help of electronic sources, and consequently, inspiration to fabricate the optical packet switch is at that point when ingress routers (edge router from where data inter in core network) collect the huge

number of packets optically and generates a high bit rate payload. This can be connected with a low rate header and pushed into core network. The packet header is converted into the electronic domain by the switch input interface while the payload will remain in optical form. We use the data kept in the header in order to route the packet to destination from source. No sooner did the packet reaches the egress node (edge router from which packet exit the core network), then the collected packet can be isolated optically and made to go onto the client network. This kind of networking design is alluded as aggregate core transport networks [7-9].

The rest of the paper is organized as follows: section II of the paper describe buffering and deflection routing, section III of the paper gives proposed work, simulation results are presented in section IV of the paper, and finally section V of the paper concludes the work.

II. BUFFERING AND DEFLECTION ROUTNG

A. *Shared Buffering Scheme*

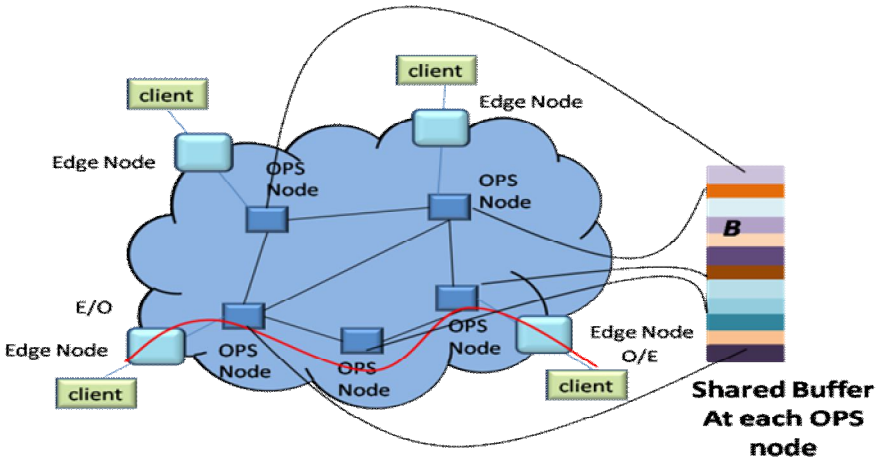


Fig. 2: Schematic of OPS Network with Shared Buffer at Each Node

As shown in Fig. 2, we will consider shared buffering scheme at each node, i.e., all the arriving packets will share a common pool of buffer of fixed capacity *B* as shown above.

B. *Shortest Path Algorithm*

In high speed network from a source to reach its destination shortest path algorithm is used. However, in case shortest path is congested other alternative route is a also followed by packets. Shortest path algorithm makes sure that packets reach their destination in the minimum possible cost. However, cost is not necessary to be economic cost; it may be factor of various network parameters like: distance, bandwidth etc.

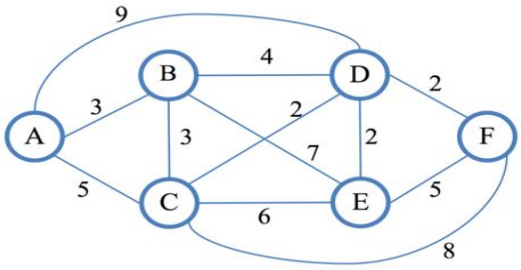


Fig. 3: Schematic of Six Node Network

C. *Limitation of Previous work*

In chitra et.al. [10], suggested a load balancing method based on the deflection of some of the packets to reduce load on a node. The limitation of chitra's work can be explained as: considering a mesh network for simplicity of *N* nodes as each one connects to another. Let again consider that at a particular load (ρ), using load balancing fraction of packets which are deflected are *g* and then

deflected load is 'ρg' which is uniformly distributed to all nodes. Therefore, additional load feel by each node is $\rho g/N$. let again out of N nodes, the number of nodes which deflect packets are n, then the effective load feel by each node will be given by

$$\rho_{eff} = \rho - \rho g + \frac{\rho g}{N} n \quad (1)$$

If only one node uses deflection routing then load is

$$\rho_{eff} = \rho - \rho g \quad (2)$$

If all the nodes use deflection routing then (N=n) load is

$$\rho_{eff} = \rho - \rho g + \rho g = \rho \quad (3)$$

Moreover due to the deflection un-necessary extra traffic is generated and lead to the congestion of networks. The illustration of above is given in Fig. 3 below. In this Fig. g is considered to be 0.5. In networks load balancing based deflection is preformed at higher loads, (0.7 - 1.0), where effective load (y-axis) is not much lesser in comparison to original load (x-axis). However, it is heavily dependent on 'n' but again at higher load we expect n to be close to N.

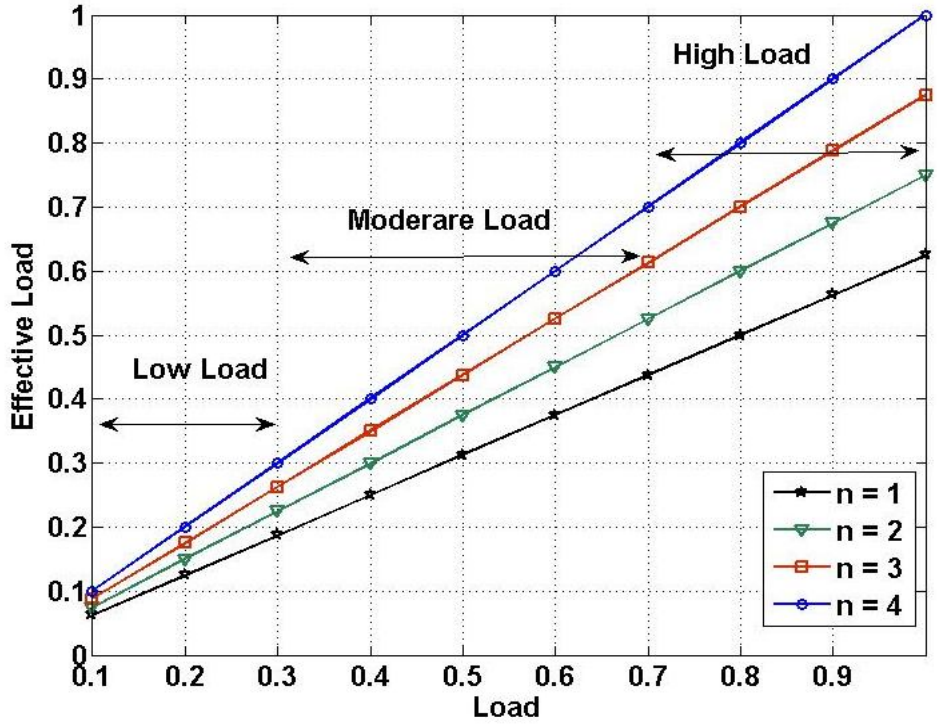


Fig. 4: Plot for load and effective load under deflection routing

III. PROPOSED WORK

We have considered 8 nodes bi-directional network for the understanding of the concepts (Fig 5). Here nodes, 1, 3, 4 and 6 have two incoming and two outgoing links. Nodes 7 and node 8 has only one incoming and one outgoing link. Node 5 have two incoming links with no outgoing links thus acts as a sink node. Thus depending on the network configuration different nodes in the network may have different number of inputs and outputs links. As the network is considered to be bi-directional there is no distinction between the input and output links. As node buffer is design for max (input links, output links).As the different number of nodes have different number of incoming and outgoing links thus buffer requirement is different for different nodes. In the network packets follow shortest path algorithm to reach its destination. Considering the case, when node 1 is the source node while node 5 is designation node, then two paths are possible 1-4-6-2-5and1-3-8-5, here in first path intermediate hops are two while in the second path intermediate hops are three. Distance in first path is 0.45+0.38+0.41+0.32=1.56 units while in the second path distance is 0.32+0.36+0.91=1.59 units. Thus first path is the shortest path. Assuming that 1unit=500Km, then shortest distance traversed would

be 780 Km. Data propagation speed in fiber as $2.07x10^8$ m/s [11]. In that case the propagation time would be $(780)/2.07x10^8$= 3.76 ms.

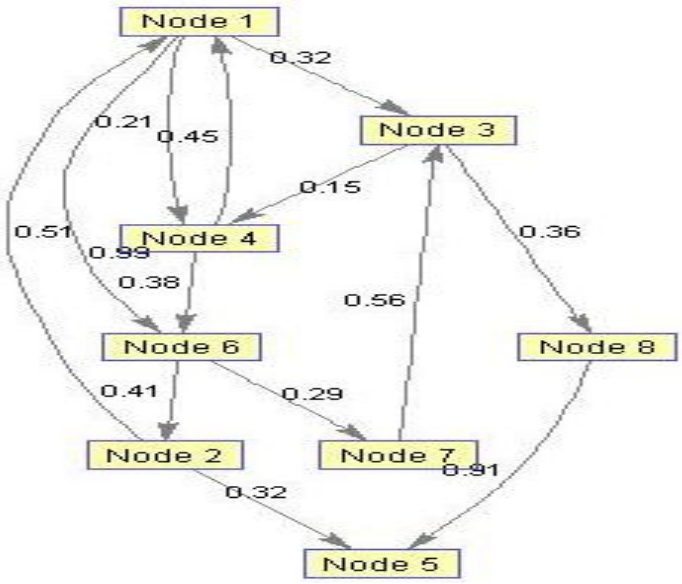


Fig. 5: Network under Consideration

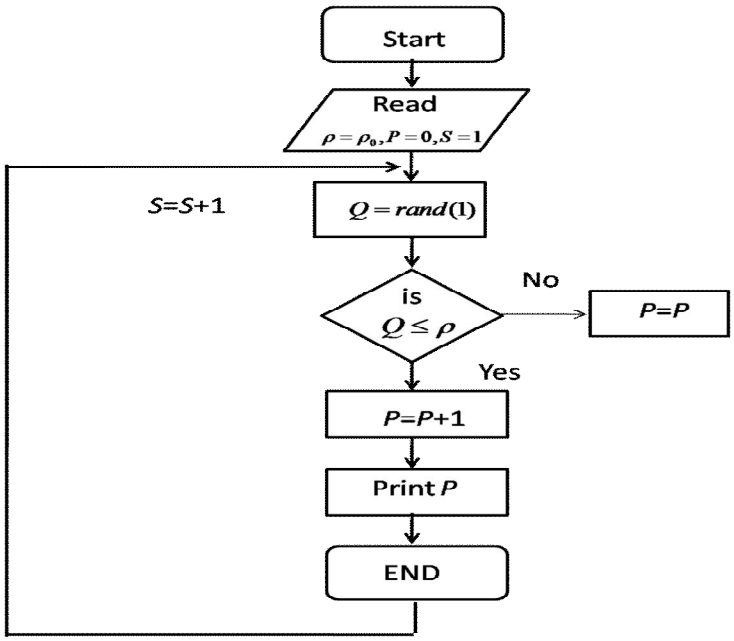
Assume that in core optical network 100000 bits packets are generated at a bit rate of 10Gbps. Therefore, slot duration is $100000/10^{10}$=10 micro second. Assuming, buffer of 16 packets; then maximum possible buffer duration is112micro second. Hence, network propagation time is much more when compared to buffering time. Therefore it can be concluded that buffering of contending packets at local contending node is better in comparison to other techniques.

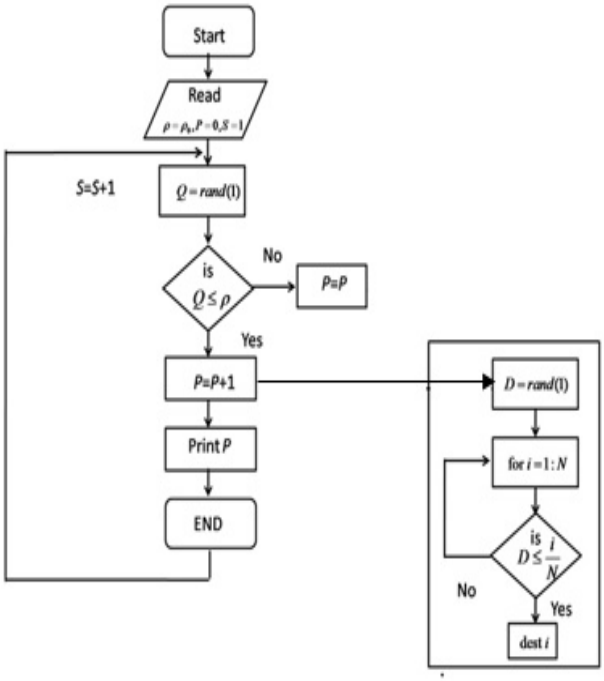
IV. SIMULATION AND RESULTS

The Monte Carlo simulation is performed in MATLAB. In the simulation, random traffic mode, i.e., information arrives randomly is considered. Here at particular load ρ, packet arrives with probability '*p*' and it can be destined to any output with probability 1/*N*.In the simulation synchronous slotted network is considered hence time is divided into equal time slots. Therefore following considerations are made in the simulation. Flow chart for packet generation and destination assignment is given in Fig. 6. In Fig. 7, process of buffer assignment is detailed. The different parameters used in the paper are detailed in Table 1; values are given whenever they are applicable.

Fig. 6: Packet generation and destination assignment process (Flow chart)

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue III, March 2018- Available at www.ijraset.com





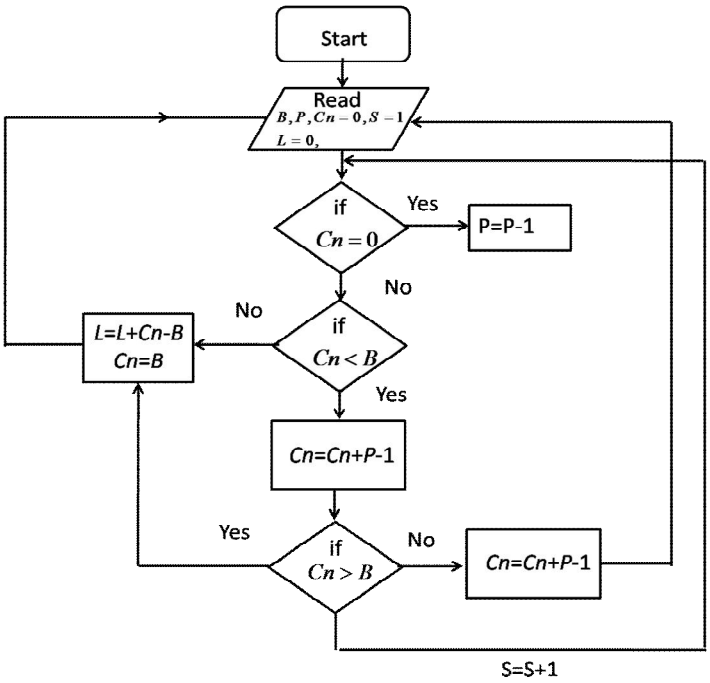


Fig. 7: Packet generation and destination assignment process (Flow chart)

Table 1: Parameters details

Parameter Description		
Description	Symbol	Value
Input and Output to switch	N	2-4
Number of generated packets	P	simulated
Load	ρ	0.1-1.0
Slot for simulation	S	10^6
Size of buffer	B	0 – 8
Counter of packets in the buffer	Cn	0 – B
Total loss of packets	L	simulated
Random Number	Q	0 - 1
Delay of packets	D	simulated

Assuming, a core node with 4 inputs and outputs lines without any buffer (Fig .8), here at higher loads huge loss is observed.

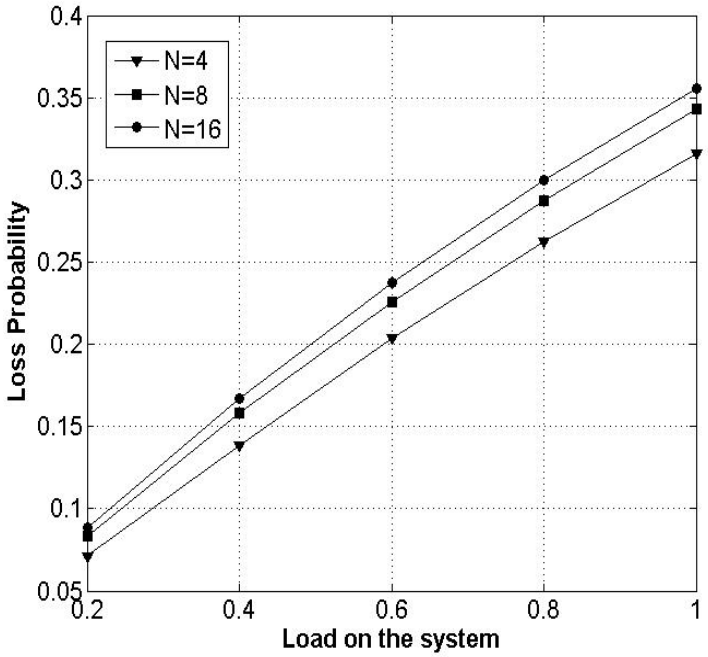


Fig. 8 Four Inputs and Outputs Node without any Buffer

Let us consider the network in Fig.8, suppose from node 1 and node 4 two packets reach for node 6, then one processed and other one will be deflected. Let us assume that processed packet is arrived from node 4 then packet arrived from node 1 will be send back to node1 from where it will send back to node 4 and a looping of 160 Km takes place. Hence, it can be concluded that in high speed networks, deflection routing is not a smart idea.

The contending packets buffering is made in either dedicated buffering scheme or in shared manner. This work concentrate on the shared buffering scheme as it provides good loss performance with lesser amount of hardware as compared to shared buffer.

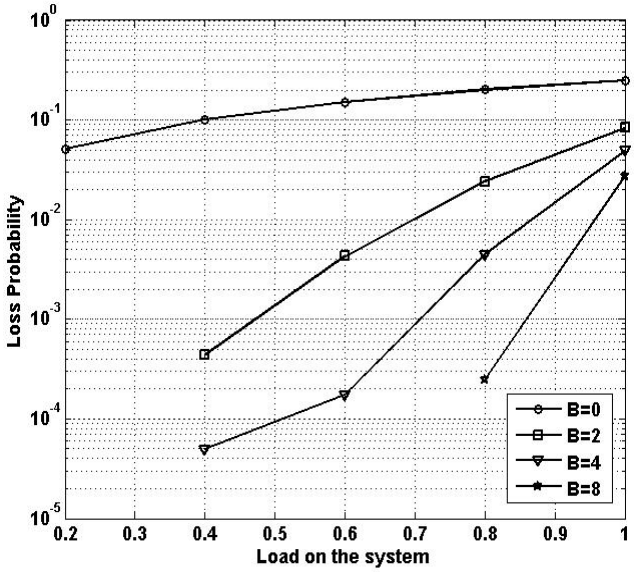


Fig. 9 Loss Probability Vs. Load with 2 Inputs/Outputs Node

In Fig. 9, loss performance is shown for 2 inputs and outputs link node (1, 3, 4 and 8). It is clear from the Fig. as the load increases, packet loss probability also increases. However, packet loss decreases as the buffer increases. Suppose at the load of 0.6, required

packet loss probability is better than $10^{-3,}$ then the needed buffer would be of 4. Similarly at the same load for packet loss probability of around $10^{-4,}$ then the needed buffer would be of 8. Thus as per the requirement different buffer space can be chosen at different nodes.

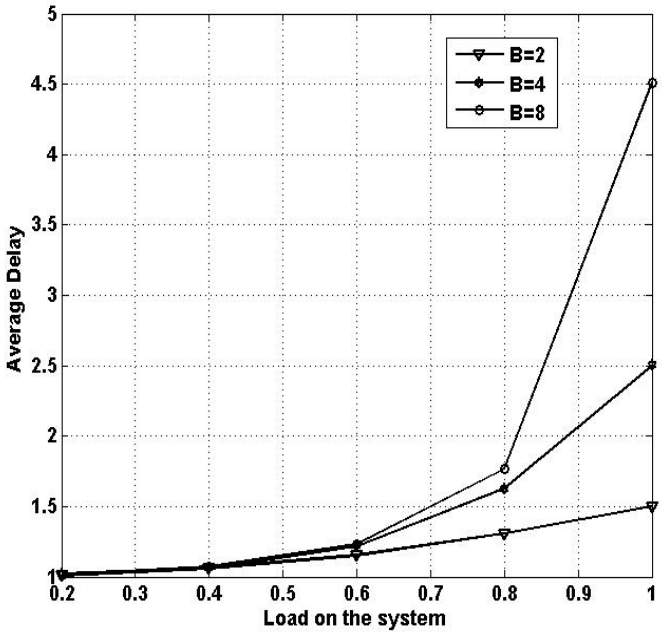


Fig. 10: Average delay Vs. Load with 2 Inputs/Outputs Node

In Fig. 10, average delay performance is shown for 2 inputs and outputs link node (3, 4 and 8). Here, average delay decreases as the buffer increases. It is clear from the Fig.s that till load of 0.6 average delay is nearly same and is around 1.3 slots. Thereafter average delay increases and at the load of 0.8, for *B*=8, average delay is nearly 1.8 slots, which rises to 9 slots at the load of 1.0.

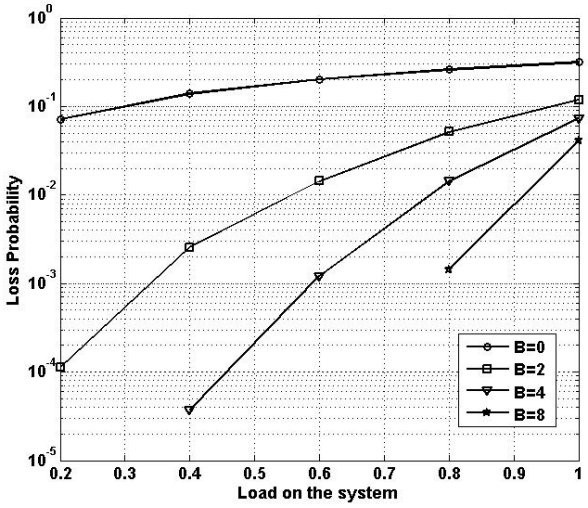


Fig. 11: Loss Probability Vs. Load with 4 Inputs/Outputs Node

In Fig. 11, loss performance is shown for 4 inputs and outputs link node, as it may possible in any other network. Suppose at the load of 0.6, required packet loss probability is better than $10^{-3,}$ then the needed buffer would be of 8. Similarly at the same load for packet loss probability of around $10^{-4,}$ then the needed buffer would be of 8. However, at the load of 0.8 the packet loss probability is around 10^{-3} for the buffer capacity of more than 8 packets will be required. Finally comparing the Fig.s 8, 4.6 and 10 it can be

concluded that as the number of inputs and outputs links increases the packet loss performance degrades and to have better packet loss probability more buffer space would be needed.

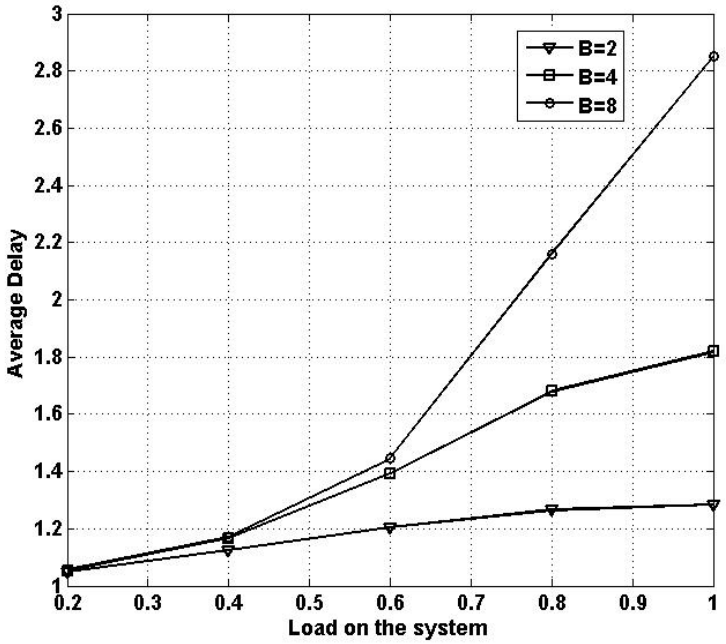


Fig. 12 : Average delay Vs. Load with 4 Inputs/Outputs Node

In Fig. 12, average delay performance is shown for 4 inputs and outputs link. It is clear from the Fig.s that till load of 0.4 average delay is nearly same and is around 1.2 slots. Thereafter average delay increases and at the load of 0.8, for *B*=8, average delay is nearly 2.2 slots, which rises to 2.85 slots at the load of 1.0. Moreover at the load of 0.8 a significant difference in the delay can be observed for *B*=2, 4 and 8.

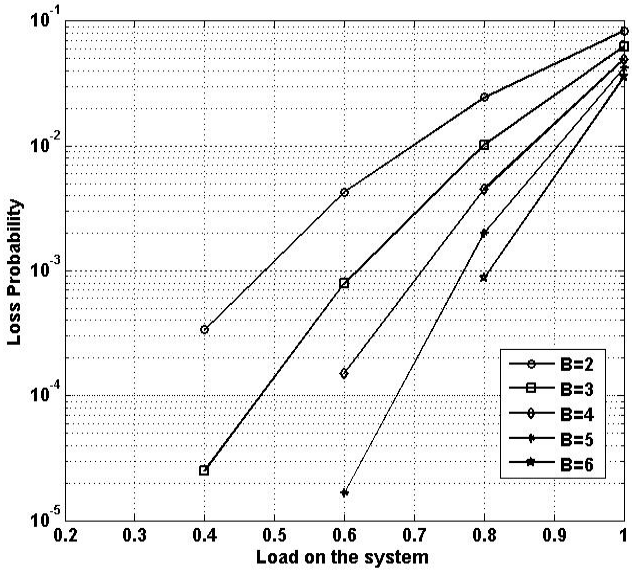


Fig. 13 : Loss Probability Vs. Load with 2 Inputs/Outputs Node

In Fig. 13, loss performance is shown for 2 inputs and outputs link node, while various buffering capacity of 2-6 packets is assumed. It is clear from the Fig. that as the buffer size increases loss probability decreases. At the load of 0.6, for B=2, 3, 4 and 5 the loss probability is $4x10^{-3}$, $8x10^{-4}$, $1.5x10^{-4}$ and $2x10^{-5}$ respectively. Thus as per the requirement, different buffer size can be set at different nodes.

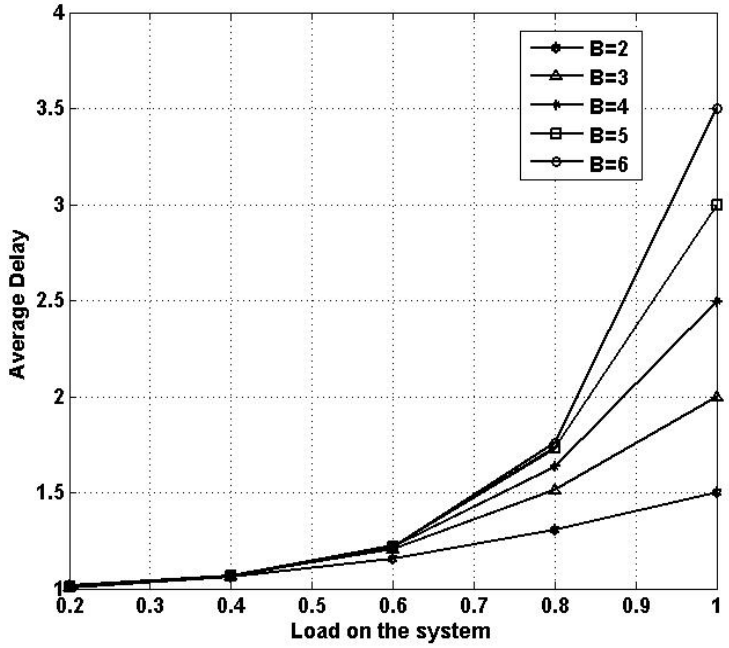


Fig. 14 : Average delay Vs. Load with 2 Inputs/Outputs Node

In Fig. 14, average delay performance is shown for 2 inputs and outputs link. It is clear from the Fig. as the load increases, average delay also increases. However, average delay decreases as the buffer increases. It is clear from the Fig.s that till load of 0.6 average delay is nearly same and is around 1.3 slots. Thereafter average delay increases and at the load of 0.8, for *B*=6, average delay is nearly 1.75 slots, which rises to 3.5 slots at the load of 1.0. It is also notable form various graph as the number of inputs increases while keeping buffer constant, the overall packet loss probability increases, while average delay decreases.

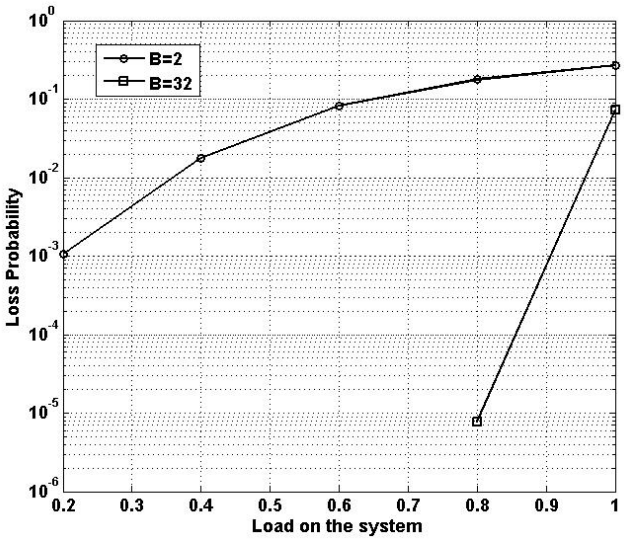


Fig. 15: Loss Probability vs. Load with 2 Inputs/Outputs Node With Variable Buffer B=2 and 32

In Fig. 14, loss performance is shown for 2 inputs and outputs link node, while various buffering capacity of 2 and 32 packets is assumed. This large variation in buffer is considered to observe the effect of buffer on packet loss probability. It is clear from the Fig. that as the buffer size increases loss probability improves tremendously. At the load of 0.8, for B=2 and 32 the loss probability is $1x10^{-1}$ and $8x10^{-6}$ respectively.

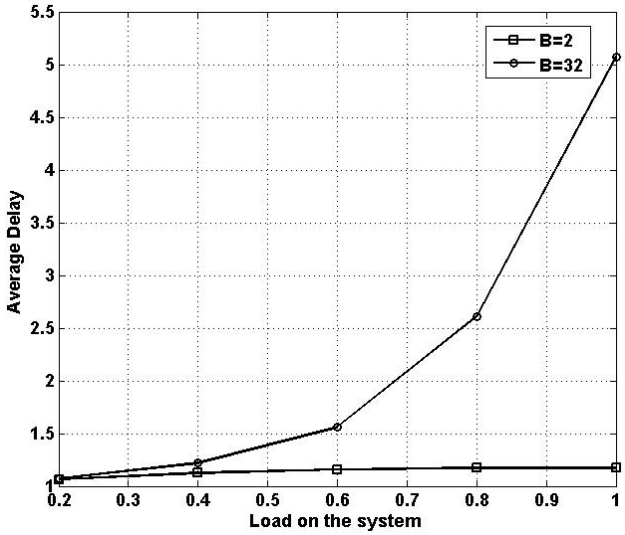
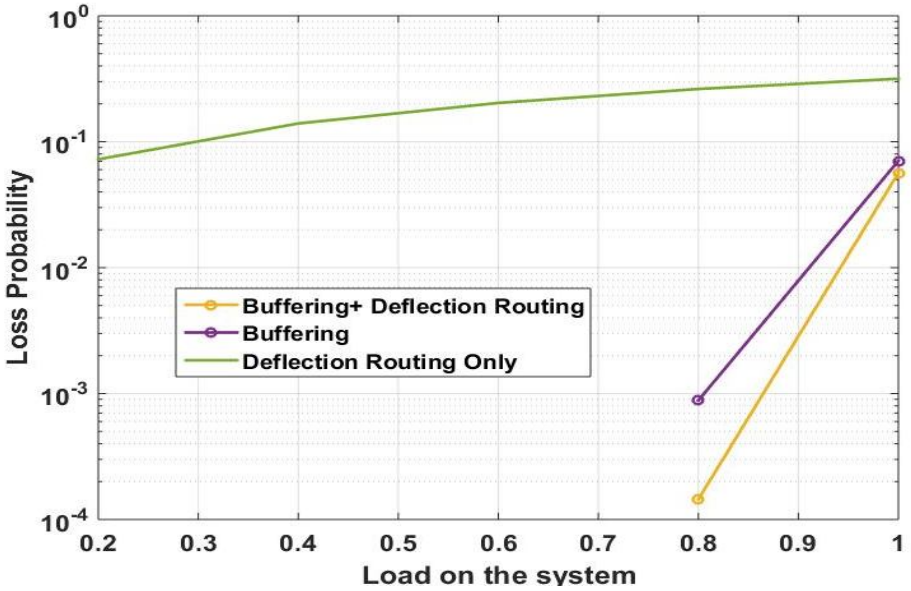


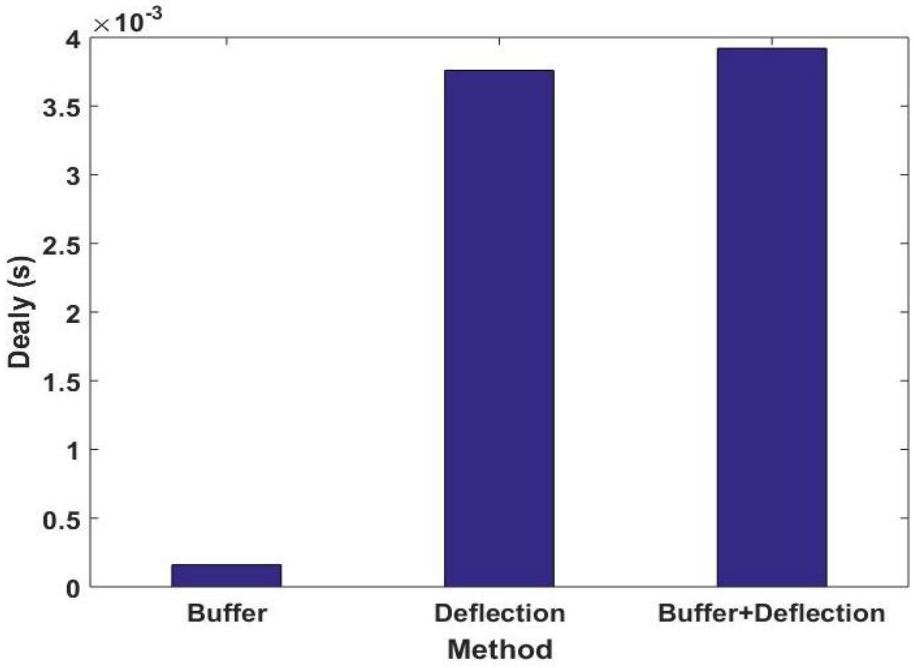
Fig. 16 : Average delay Vs. Load with 2 Inputs/Outputs Node

In Fig. 16, average delay performance is shown for 2 inputs and outputs link. It is obvious form the Fig. that as the buffer increases, the average delay increases. The delay increases and at the load of 0.8, for *B*=2, average delay is nearly 1.2 slots, which is 2.6 slots for B=32. But it is also observable that the rise in average delay is not that much higher and the load of 1.0 it is 5.2 slots.

V. COMPARISON OF RESULTS

In figure packet loss probability vs. load is plotted, under three conditions, of buffering, buffering and deflection routing and deflection routing only. It is clear from the figure that packet loss performance under deflection routing is very poor and not acceptable. While with buffering packet loss performance is much improved, therefore buffering is found to be better option in comparison to deflection routing. The best packet loss performance is observed when both buffering and deflection routing is used in conjunction.





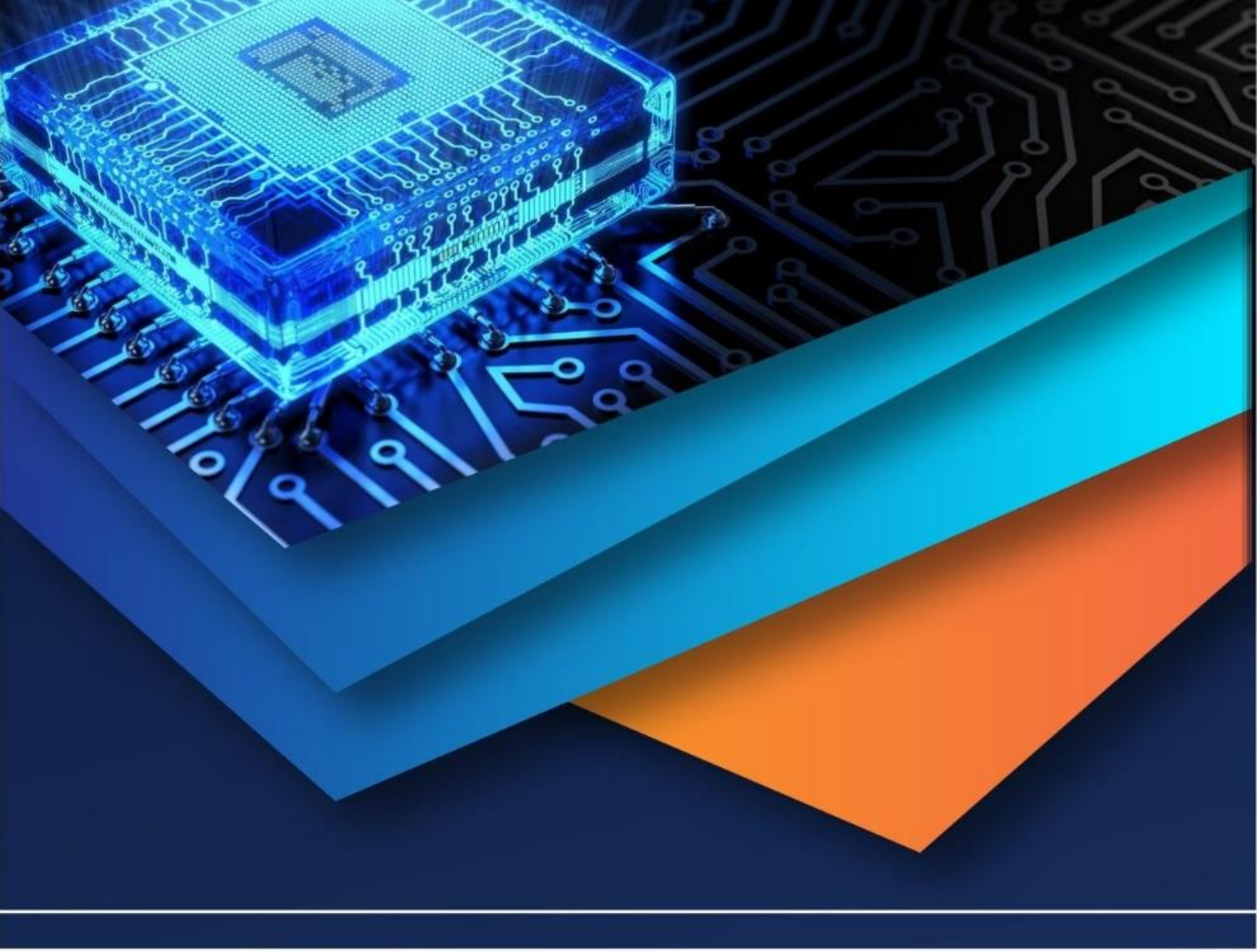
In figure delay vs. load is plotted, under three conditions, of buffering, buffering and deflection routing and deflection routing only. It is clear from the figure that delay under buffering condition is minimal. Under, deflection routing is delay is comparatively high. Poorest delay performance is observed when both buffering and deflection routing is used in conjunction. Therefore finally it can be concluded that buffering of contending packets is best possible option.

VI. CONCLUSIONS

Optical packet switching is an integral part of optical networks. For contending packets in networks both buffering and deflection routing are considered as viable option. In this work, both the methods are discussed, and it has been found that, deflection of packets is not a very good option as it increases delay and load is not reduced as desired. Using buffering mechanism at the contending nodes packet loss probability can be reduced significantly with reasonable amount of packet delay which is much lesser in comparison to network traversing delay.

REFERENCES

[1] R. S. Tucker and W.D. Zhong., "Photonic packet switching: an overview," IEICE Trans. Commun., vol. E82 B, pp. 254-264, Feb. 1999.
[2] R. Srivastava, R. K. Singh and Y. N. Singh, "Optical loop memory for photonic switching application," OSA J. of Optical Networking, vol. 6 pp. 341-348, Apr 2007.
[3] N. Verma, R. Srivastava and Y. N. Singh, "Novel design modification proposal for all optical fiber loop buffer switch," in 2002 Proc. Photonics Conf., p. 181.
[4] Y. N. Singh, A. Kushwaha and S. K. Bose, "Exact and approximate modeling of an FLBM-based all optical packet switch," IEEE J. of Lightw. Technol., vol. 21, pp. 719-726, Mar. 2003.
[5] F.S.Choa, et.al., "An optical packet switch based on WDM technologies," IEEE J. of Lightw. Technol., vol. 23, pp. 994-1013, Mar. 2005.
[6] H. Nakazima, "Photonic ATM switch based on a multi wavelength fiber loop buffer," CSELT tech. Rep. Vol. 23**,** pp. 331-335, 1995.
[7] R. Srivastava, R. K. Singh and Y. N. Singh, "Regenerator based optical loop memory," in Proc. IEEE TENCON -07 (accepted).
[8] R. Takabashi, et.al., "Photonic random access memory for 40- Gbps 16-b burst optical packets," IEEE Photon Technol. Lett. Vol.16, No. 4, pp. 1185-1187, Apr. 2004.
[9] R. K. Singh, R. Srivastava and Y. N. Singh, "Wavelength division multiplexed loop buffer memory based optical packet switch," Optical and Quantum Electronics, vol. 39, No. 1 pp. 15-34, Jan. 2007.
[10] Chitra Sharma, and Akhilesh Kumar Yadav. "Buffering Strategies in Optical Packet Switching." International Journal of Computer Network and Information Security, Vol. No. 3, pp.19-26, 2016



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY