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Design and Analysis of CMOS Cell Structures using Adiabatic Logic

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***Abstract:** This paper deals with two types of inverter structure design using CMOS and adiabatic technique. Power consumption is one of the basic parameters of any kind of integrated circuit (IC). Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost. Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and which recycle the energy from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. All simulation result performs on 180nmTMCS technology and to analysis the power consumption of both CMOS and adiabatic logic.*
***Keywords:** VLSI, Dynamic Power, Static Power, Adiabatic logic. PFAL, 2PASCL*

I. INTRODUCTION

New generations of processing technology are being developed while present generation devices are at very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1 MHz. Then comes the Pentium in 2001, with 42 million transistors, dissipating around 65 watts of power and clocked at 2.40 GHz [13].

If this exponential rise in the power density were to increase continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electro migration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance. Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable systems. Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field.

Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power. A study by American Council for an Energy-Efficient Economy estimated that office equipment account for 5% for the total US commercial energy usage in 1997 and could rise to 10% by the year 2004 if no actions are taken to prevent the trend [14].

Power consumption is one of the basic parameters of any kind of integrated circuit (IC). Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost.

II. POWER AND ENERGY DEFINITION

The power consumed by a device is, by definition, the energy consumed per unit time. In other words, the energy (E) required for a given operation is the integral of the power (P) consumed over the operation time (T), hence,

$$E=\int_0^T P(t)dt \qquad (1)$$

Here, the power of digital CMOS circuit is given by

$$P = C\ VDD\ VS\ f \qquad (2)$$

Where, C is the capacitance being recharged during a transition. VDD is the supply voltage, Vs is the voltage swing of the signal, and f is the clock frequency. If it is assumed that an operation requires n clock cycles, T can be expressed as n / f. Hence, Equation (1) can be rewritten as

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$$E = n\ C\ VDD\ VS \qquad (3)$$

It is important to note that the energy per operation is independent of the clock frequency.

It is more convenient to talk about power consumption of digital circuits at this point. Although power depends greatly on the circuit style, it can be divided, in general, into static and dynamic power. In all of the logic families except for the push-pull types such as CMOS, the static power tends to dominate. That is the reason why CMOS is the most suitable circuit style for very large scale integration (VLSI). The power consumed when the CMOS circuit is in use can be decomposed into two basic classes: static and dynamic.

A. Static Power

The static or steady state power dissipation of a circuit is expressed by the following relation [13]

$$P\ stat = I\ stat\ VDD \qquad (4)$$

Where, Istat is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static (DC) power since in the steady state there is no direct path from VDD to ground as PMOS and NMOS transistors are never on simultaneously. Thus, there will always be leakage currents and substrate injection currents, which will give to a static component of CMOS power dissipation. Another form of static power dissipation occurs for the so-called Ratioed logic. Pseudo-NMOS is an example of a Ratioed CMOS logic family. In this, the PMOS pull-up is always on and acts as a load device for the NMOS pull-down network. Therefore, when the gate output is in low-state, there is a direct path from VDD to ground and the static currents flow. In this state, the exact value of the output voltage depends on the ratio of the strength of PMOS and NMOS networks – hence the name. The static power consumed by these logic families can be considerable.

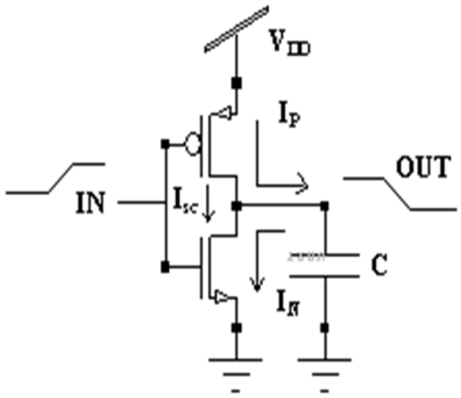

Fig.1: CMOS Inverter for power analysis

B. Dynamic Power

The dynamic component of power dissipation arises from the transient switching behavior of the CMOS device. At some point during the switching transient, both the NMOS and PMOS devices will be turned on. This occurs for gate voltages between Vtn and VDD - Vtp. During this time, a short circuit exists between VDD and ground and the currents are allowed to flow. Although short circuit dissipation cannot always be completely ignored, it is certainly not the dominant component of power dissipation in well-designed CMOS circuits. Instead, dynamic dissipation due to capacitance charging consumes most of the power. This component of dynamic power dissipation is the result of charging and discharging of the parasitic capacitances in the circuit.

The situation is modeled in Figure one, where the parasitic capacitances are lumped at the output in the capacitor C. Consider the behavior of the circuit over one full cycle of operation with the input voltage going from VDD to ground and back to VDD again. As the input switches from high to low, the NMOS pull-down network is cut-off and PMOS pull-up network is activated charging load capacitance C up to VDD. This charging process draws energy equal to CVDD2 from the power supply. Half of this is dissipated immediately in the PMOS transistors, while the other half is stored on the load capacitance. Then, when the input returns to VDD, the process is reversed and the capacitance is discharged, its energy being in the NMOS network. In summary, every time a capacitive node switches from ground to VDD (and back to ground), energy of CVDD2 is consumed.

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This leads to the conclusion that CMOS power consumption depends on the switching activity of the signals involved. We can define activity, α as the expected number of zero to one transition per data cycle. If this is coupled with the average data rate, f, which may be the clock frequency in a synchronous system, then the effective frequency of nodal charging is given the product of the activity and the data rate: αf. This leads to the following formulation for the average CMOS power consumption:

$$P_{dyn} = \alpha C V_{DD}^2 f \quad (5)$$

III. ADIABATIC LOGIC CIRCUITS

Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and which recycle the energy from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. As such every time a charge-discharge cycle occurs, an amount of energy equal to CVdd2 is dissipated. Unlike the conventional CMOS circuits, in adiabatic circuits energy is recycled.

A. Principle of Adiabatic Switching

Adiabatic switching is commonly used to minimize energy loss during the charge/discharge cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time varying voltage source instead of a fixed voltage supply. Here, the load capacitance (CL) is charged by a constant current source (I). In conventional CMOS logic we use constant voltage source to charge the load capacitance [2]. Here, R is the on-resistance of PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume the capacitor voltage zero initially.

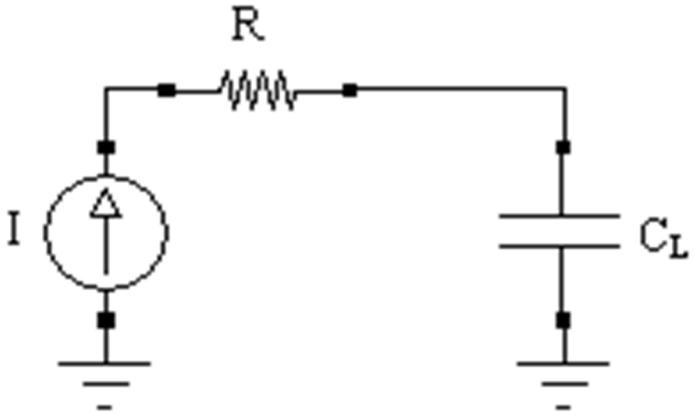

Fig.2: Adiabatic logic circuit

Theoretically, when driving voltage (Va) switching time (T) from 0 V to Vdd is long, the energy dissipation is nearly zero. When Va changes from HIGH to LOW in the pull- down network, discharging via the NMOS transistor occurs. From equation, it is observed that when energy dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the load capacitor during the current subsequent computational steps. Systems based on above-mentioned technique for charge recovery is not necessarily reversible [8].

B. A Simple Adiabatic Logic Gate

In the following, we will examine simple circuit configurations which can be used for adiabatic switching. Figure 3 shows a general circuit topology for the conventional CMOS gates and adiabatic counterparts. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up and the pull-down networks must be replaced with complementary transmission-gate (T-gate) networks. The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pull-down function drives the complementary output node. Note that all the inputs should also be available in complementary form [11].

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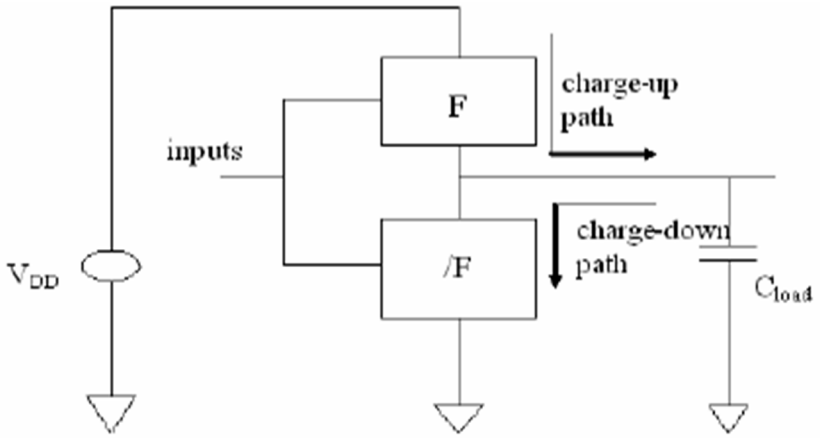

Fig.3: The general circuit topology of a conventional CMOS logic gate

Both the networks in the adiabatic logic circuit are used to charge-up as well as charge-down the output capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a pulsed-power supply with the ramped voltage output.

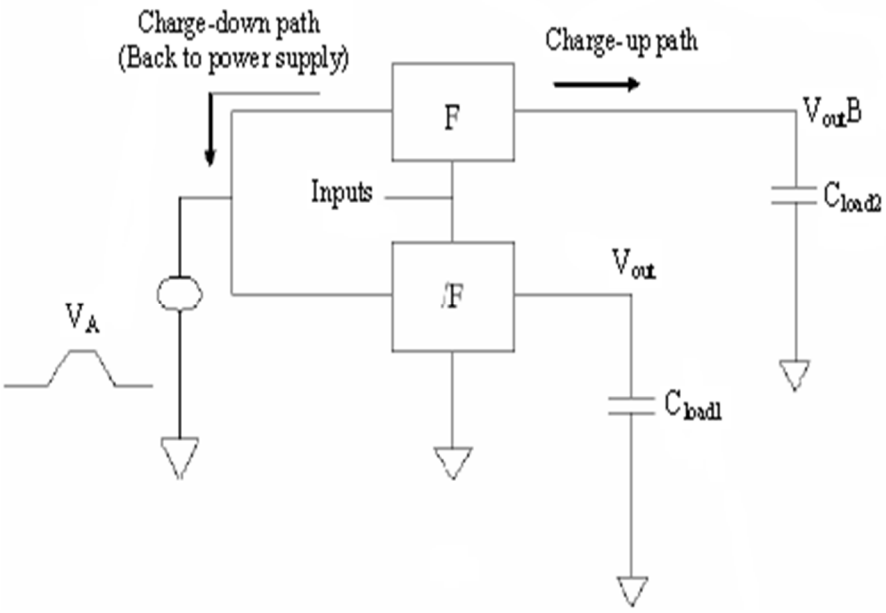

Fig.4: The topology of an adiabatic logic gate
implementing the same function

Note the circuit modifications which are necessary to convert a conventional CMOS logic circuit into an adiabatic logic circuit increase the device count by a factor of two or even more.

IV. IMPLEMENTATION AND RESULT

Power dissipation in conventional CMOS circuits primarily occurs during the device switching. When the logic level in the system is "1," there is a sudden flow of current through R. Q = CLVdd is the charge supplied by the positive power supply rail for charging CL to the level of Vdd. Hence, the energy drawn from the power supply is Q·Vdd = CLVdd2 [4].

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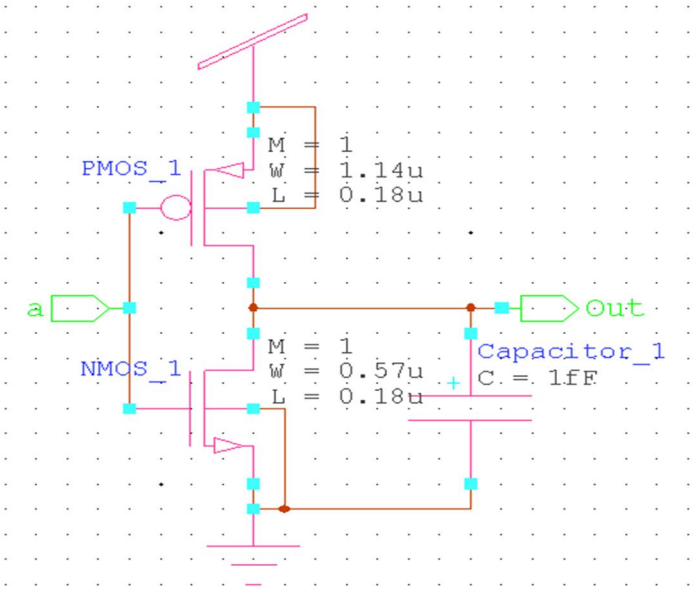

Fig.5: CMOS inverter circuit

By assuming that the energy drawn from the power supply is equal to that supplied to CL, the energy stored in CL is said to be one-half the supplied energy, i.e., Estored = (1/2)CLVdd2.

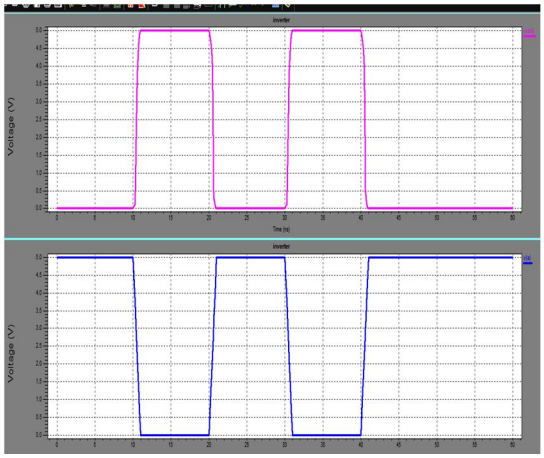

Fig.6. Waveforms of input and output voltage

A. Proposed Adiabatic Logic Inverter

Adiabatic switching is commonly used to minimize energy loss during the charge/discharge cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time varying voltage source instead of a fixed voltage supply. This is accomplished by using AC power supplies to charge the circuit during the specific adiabatic phases and subsequently discharge the circuit to recover the supplied charge. The peak current in adiabatic circuits can be significantly reduced by ensuring uniform charge transfer over the entire time available. Hence, if I is considered as the average of the current flowing to CL, the overall energy dissipated during the transition phase can be reduced in proportion to

$$I2RTp = (CLVdd/ Tp)2 RTp = (RCL/Tp) CLV2 dd \quad (10)$$

Theoretically, during adiabatic charging, when Tp, the time for the driving voltage Va to change from 0 V to Vdd is long, energy dissipation is nearly zero. When VaB changes from HIGH to LOW in the pull-down network, discharging via the NMOS transistor occurs. From Eq. (10), it is apparent that when energy dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the capacitors during a given computation step and uses it during subsequent

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computations. Systems based on the above-mentioned theory of charge recovery are not necessarily reversible. The basic inverter circuit is shown in

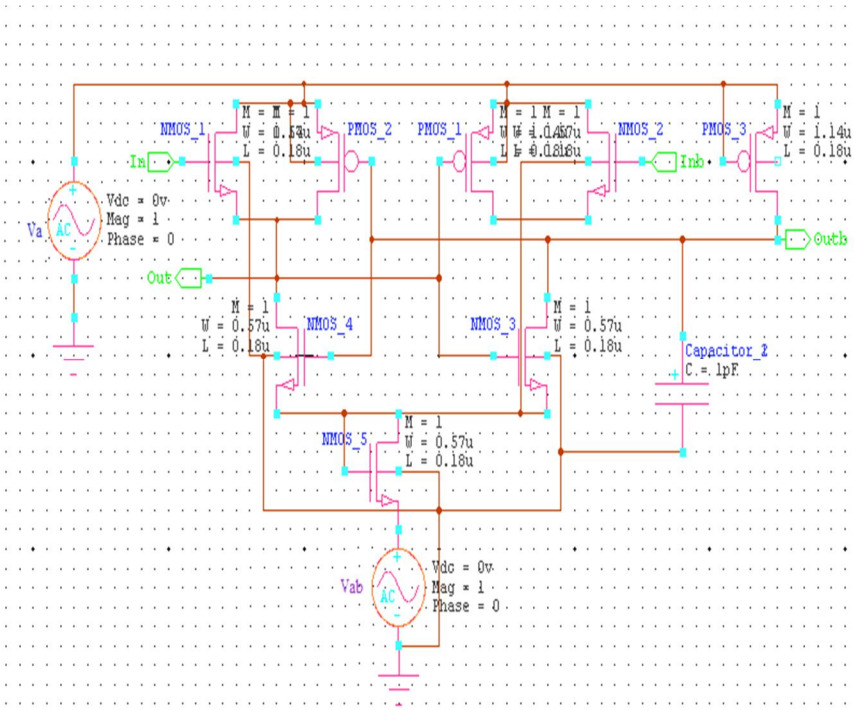

Fig.7: Proposed adiabatic logic inverter circuit

above figure of this circuit is an adiabatic amplifier, a latch made by the two PMOS M1 and M2 and two NMOS M5 and M6, that avoids the logic level degradation at Out and Outb, the logic circuit M3 and M4 are in parallel with M1 and M2 and forms transmission gate [1]. This circuit uses two-phase split level sinusoidal power supplies which are denoted as Va and VaB, where Va & VaB can vary from 1.3 to 1.6V & 0.3 to 0V respectively.

The circuit operates in two phases, evaluation and hold, in evaluation phase, Va swings up and VaB swings down, and in hold phase, VaB swings up and Va swings down. Let us assume, during evaluation phase the input (In) is high and input (InB) goes low accordingly, consequently M3 is conducting and output (OutB) follows the power supply Va, and at the same time M1 gets turned ON by output (Out) and thus reduces the charging resistance. Being in parallel with M3 and during hold phase, charge stored on the load capacitance CL flows back to power supply through M1. So that power dissipation is reduced. The proposed circuit uses two MOS diodes, one is connected to Out and Va and other diode is connected between common source of M5-M6 and other power supply VaB, Both the MOS diodes are used to increase the discharging rate of internal nodes.

Table I Power Consumption comparison of proposed inverter vs CMOS

V_{DD} (Volts)	Power Consumption (Watts)	
	CMOS	Proposed
1.2	5.054443E-008	2.450000E-013
1.4	6.595536E-008	2.780000E-012
1.6	8.316927E-008	3.480000E-010
1.8	9.878095E-008	4.980000E-010

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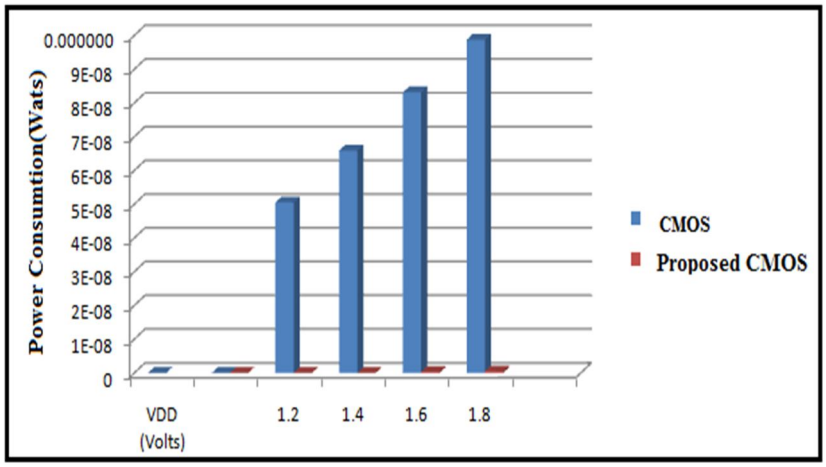

Fig.8. Power Consumption comparison of proposed inverter vs CMOS at power supply

B. PFAL

The structure of PFAL logic [16] is shown in figure 9. Two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The two major differences with respect to ECRL are that the latch is made by two pMOSFETs and two nMOSFETs, rather than by only two pMOSFETs as in ECRL, and that the functional blocks are in parallel with the transmission pMOSFETs.

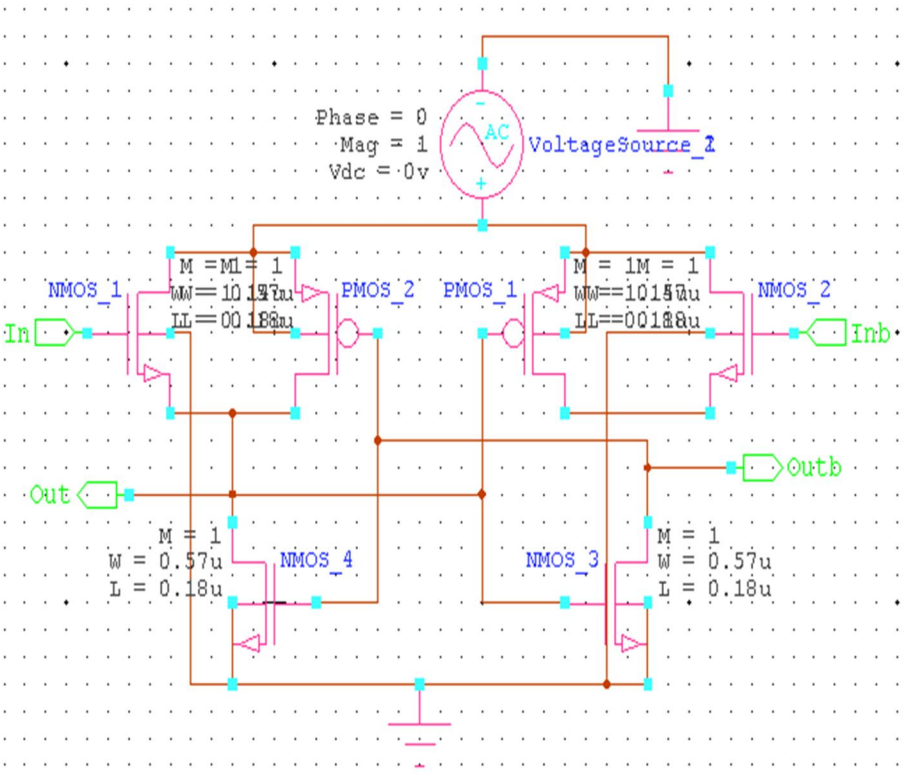

Fig.9: PFAL Logic Circuit

Thus the equivalent resistance is smaller when the capacitance needs to be charged. The ratio between the energy needed in a cycle and the dissipated one can be seen in figure 4. During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied energy decreases.

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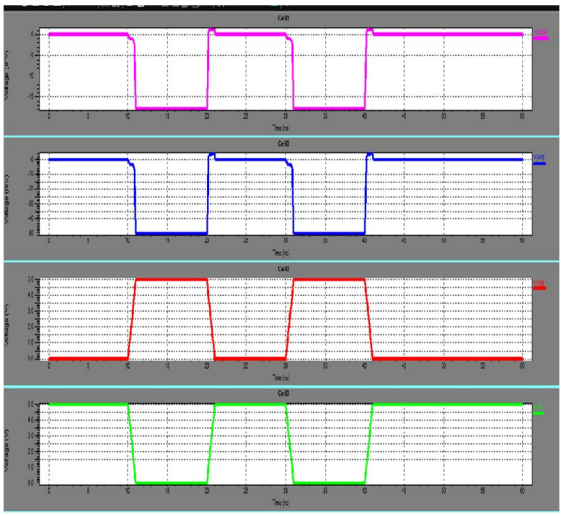

Fig.10. input and output Waveforms of PFAL Circuit

C. 2PASCL

Figure11 shows a circuit diagram of Two-Phase Adiabatic Static Clocked Logic (2PASCL) inverter. A double diode circuit is used, where one diode is placed between the output node and power lock, and another diode is adjacent to the NMOS logic circuit and connected to the other power source. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous if the signal nodes are preceded by a long chain of switches. The circuit operation is divided into two phases: evaluation and hold. In the evaluation phase, Va swing up and VaB swings down [18]. On the other hand, in the hold phase,VaB swings up and Va swings down. Let us consider the inverter's logical circuit demonstrated in

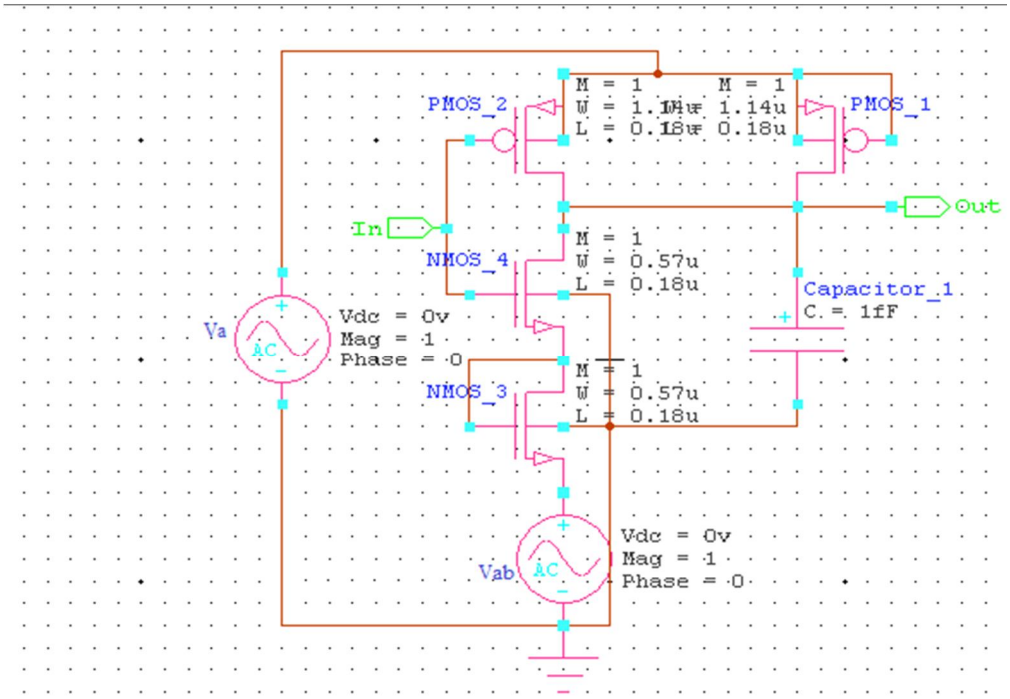

Fig.11 2PASCL inverter

The operation of the 2PASCL inverter is in two stage:1) Evaluation phase 2) Hold phase

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Table II Power Consumption comparison of proposed inverter vs CMOS

V_{DD} (Volts)	Power Consumption (Watts)			
	CMOS	PFAL	2PASCL	Proposed
1.2	5.054443E-008	1.270000E-010	3.870000E-012	2.450000E-013
1.4	6.595536E-008	2.430000E-010	2.900000E-011	2.780000E-012
1.6	8.316927E-008	4.560000E-009	2.980000E-010	3.480000E-010
1.8	9.878095E-008	3.240000E-009	4.400000E-009	4.980000E-010

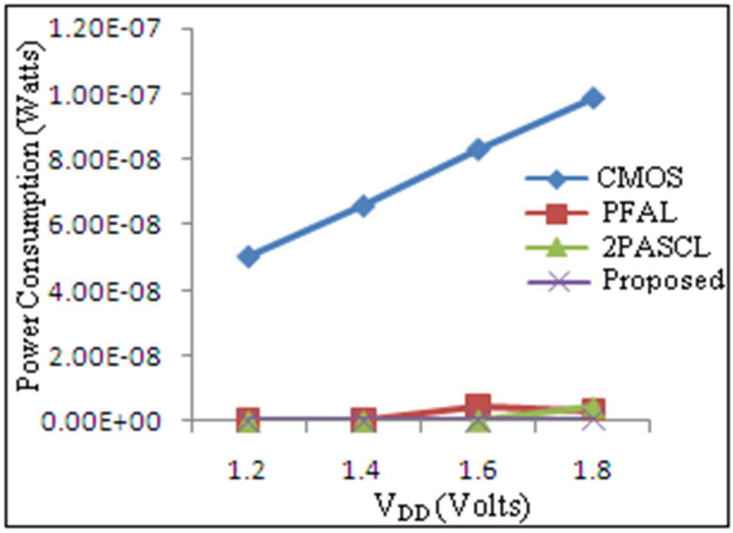

Fig.12 Power Consumption comparison of proposed inverter vs CMOS at power supply

Table III Power Consumption comparison of proposed inverter vs CMOS at frequency

Freq. (MHz)	Power Consumption (Watts)			
	CMOS	PFAL	2PASCL	Proposed
50	2.572938E-007	2.270000E-010	3.870000E-011	2.280000E-012
100	5.069244E-007	3.480000E-008	2.900000E-010	2.370000E-011
150	7.844564E-007	8.760000E-008	9.980000E-008	3.480000E-009
200	2.205502e-006	3.240000E-007	4.400000E-007	4.980000E-009

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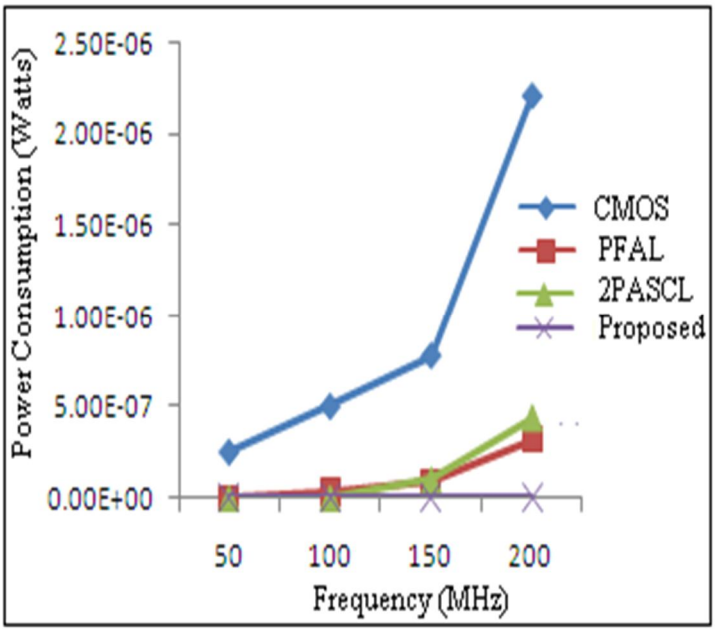

Fig.13 Power Consumption comparison of proposed inverter vs CMOS at frequency

Table IV Power Consumption comparison of proposed inverter vs CMOS at Capacitance

Capacitor (fF)	Power Consumption (Watts)			
	CMOS	PFAL	2PASCL	Proposed
20	165.198	0.265	0.037	0.0002
30	194.966	3.570	0.185	0.002
40	224.761	9.860	1.870	0.034
50	358.843	58.700	25.600	1.010
60	422.752	67.500	32.700	4.220

1) Design and Simulation for a two-input CMOS NAND gate based 2PASCL

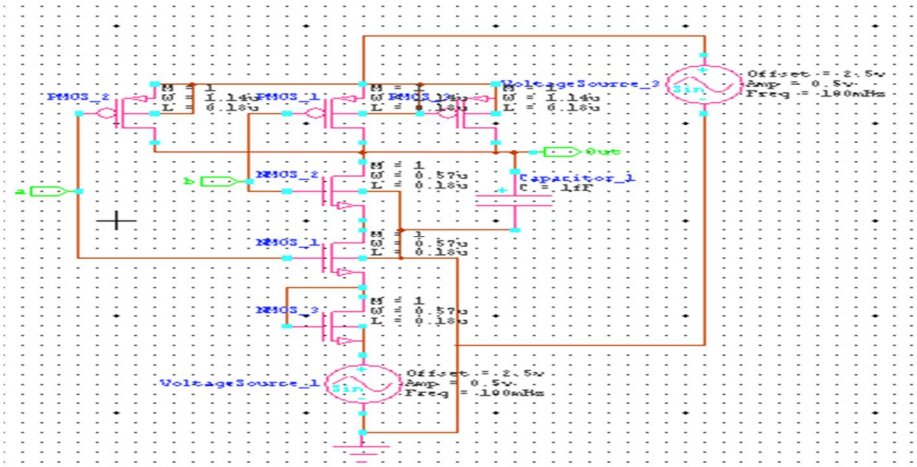

Fig.14. 2PASCL NAND Gate

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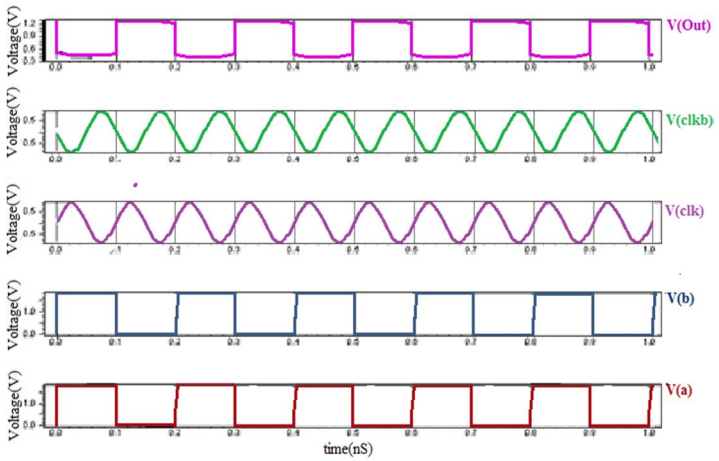

Fig.15. Input and Output waveforms for 2PASCL NAND gate

D. Proposed Adiabatic NAND gate

In this circuit we use two diodes at PMOS and NMOS logic which shown in below fig14 and are used to increase the discharging rate of internal nodes. The circuit operates in two phases, evaluation and hold, in evaluation phase, Va swings up and VaB swings down, and in hold phase, VaB swings up and Va swings down. Let us assume, during evaluation phase the input (In) is high and input (InB) goes low accordingly, consequently PMOS transistor at input a is conducting and output (OutB) follows the power supply Va, and at the same time PMOS transistor at input b gets turned ON by output (Out) and thus reduces the charging resistance. Being in parallel with M3 and during hold phase, charge stored on the load capacitance C_L flows back to power supply through transistor PMOS at input a. So that power dissipation is reduced. The proposed circuit uses two MOS diodes, one is connected to Out and Va and other diode is connected between common source of inverter (two NMOS logic which attach in midpoint of circuit and connect to the diode at NMOS logic) and other power supply VaB, Both the Mos diodes are used to increase the discharging rate of internal nodes.

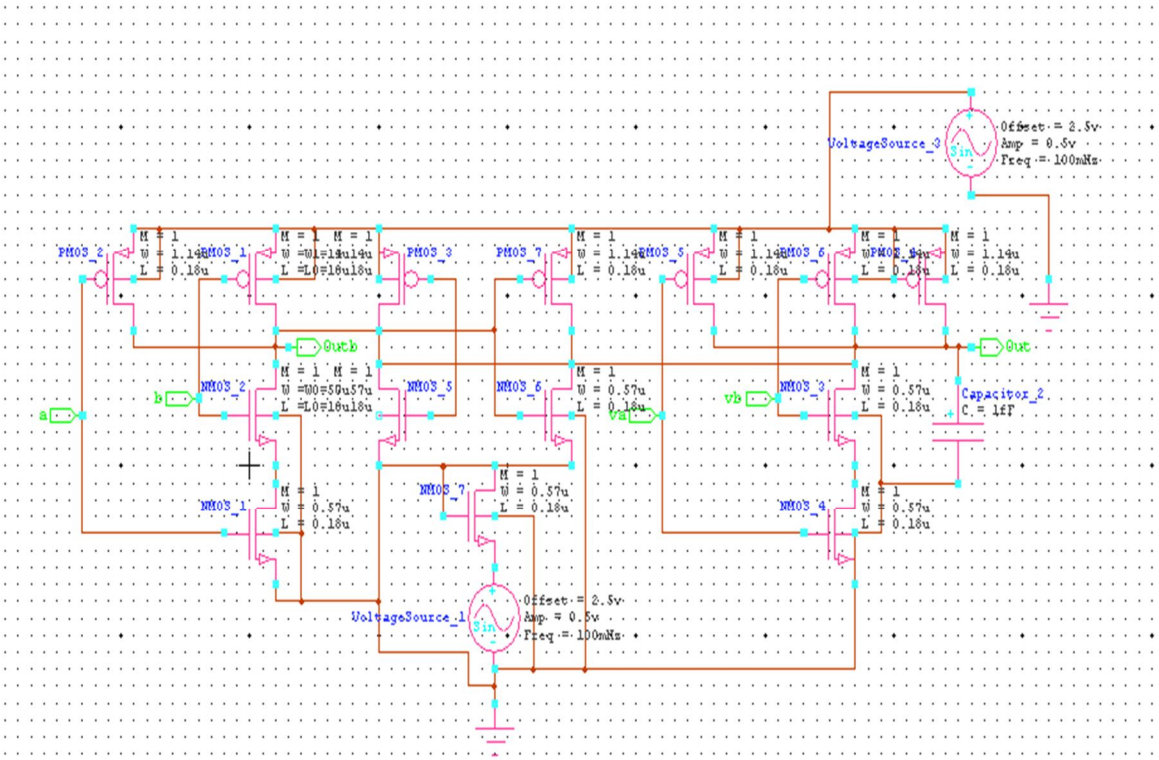

Fig.16. Proposed NAND gate

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Table V Power Consumption comparison of proposed NAND vs NAND at Power supply

V_{DD} (Volts)	Power Consumption (nWatts)		
	NAND	2PASCL	Proposed
1.2	6.149	0.014	0.002
1.4	10.755	0.196	0.015
1.6	18.131	2.560	0.243
1.8	29.943	11.401	3.285

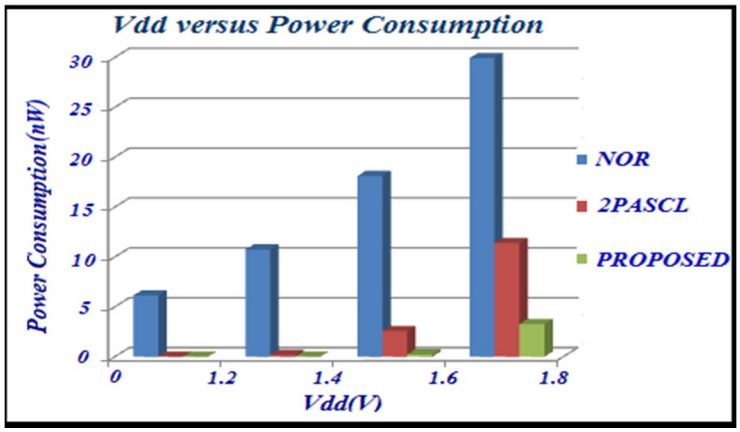

Fig.17. Power Consumption comparison of proposed NAND vs NAND at power supply

Table VI Power Consumption comparison of proposed NAND vs NAND at frequency

Frequency (MHz)	Power Consumption (uWatts)		
	NAND	2PASCL	Proposed
50	0.269	0.051	0.0056
100	0.660	0.162	0.023
150	1.758	1.579	0.487
200	5.317	3.987	1.540

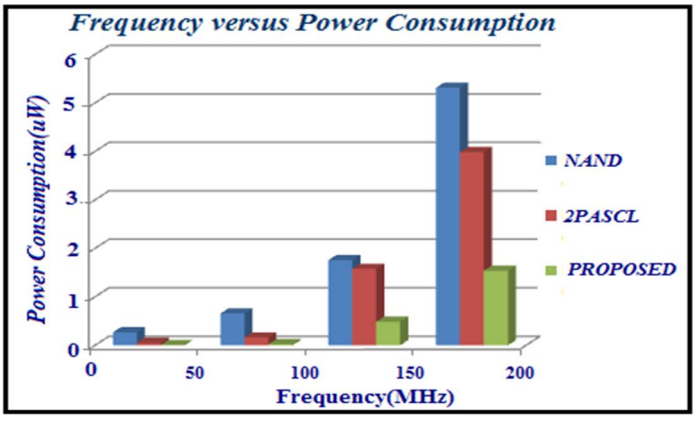

Fig.18. Power Consumption comparison of proposed NAND vs NAND at frequency

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Table VII Power Consumption comparison of proposed NAND vs NAND at capacitance

Capacitor (fF)	Power Consumption (nWatts)		
	NAND	2PASCL	Proposed
20	1.952	0.015	0.001
30	2.546	0.560	0.023
40	3.168	1.170	0.141
50	4.812	2.437	0.839
60	5.275	3.567	1.241

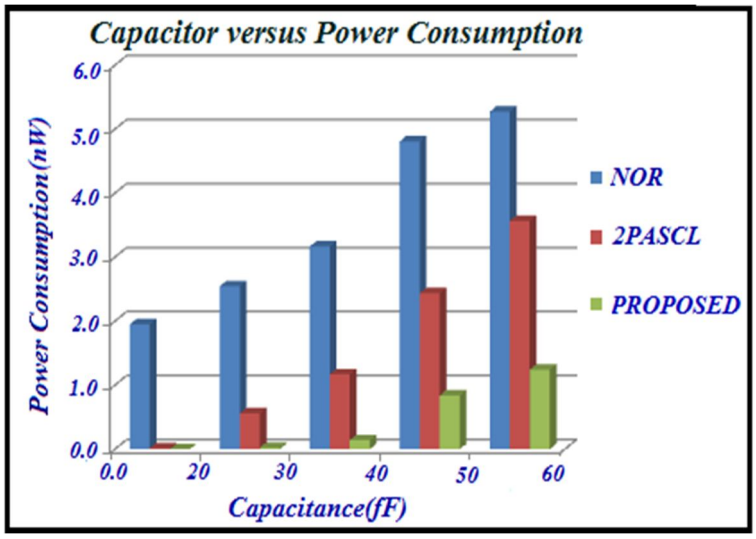

Fig.19. Power Consumption comparison of proposed NAND vs NAND at capacitance

1) Design and Simulation for a two-input CMOS NOR gate

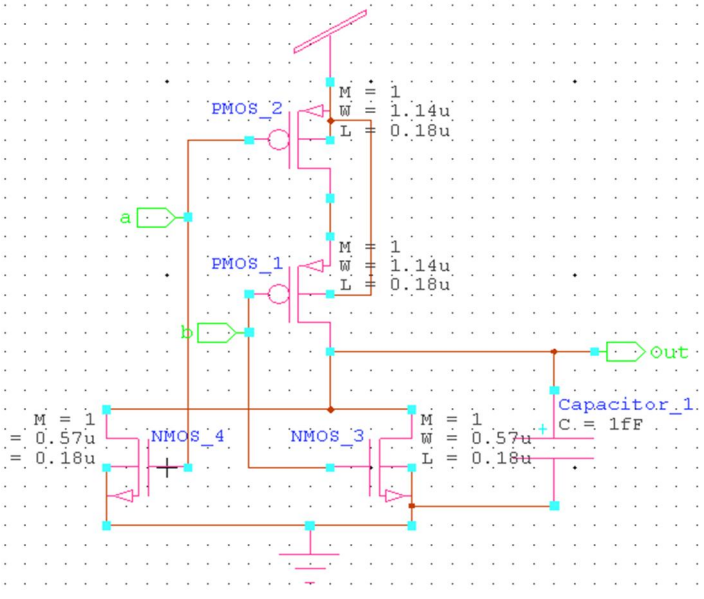

Fig.20. Two input NOR gate

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2) Design and Simulation for a 2PASCL NOR gate

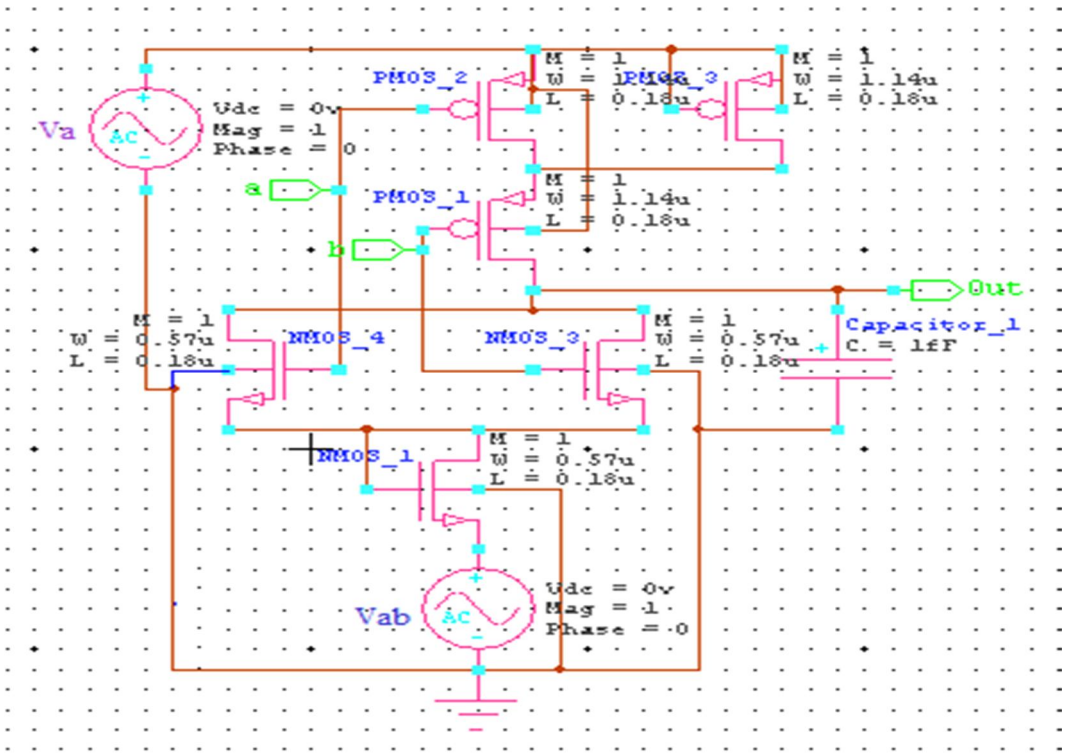

Fig.21. 2PASCL NOR gate

Table VIII Power Consumption comparison of proposed NOR vs NOR at Power supply in 180nm technology

V_{DD}(Volts)	Power Consumption(nWatts)	
	NOR	2PASCL
1.2	0.820	0.004
1.4	1.239	0.019
1.6	7.613	0.256
1.8	19.015	3.240

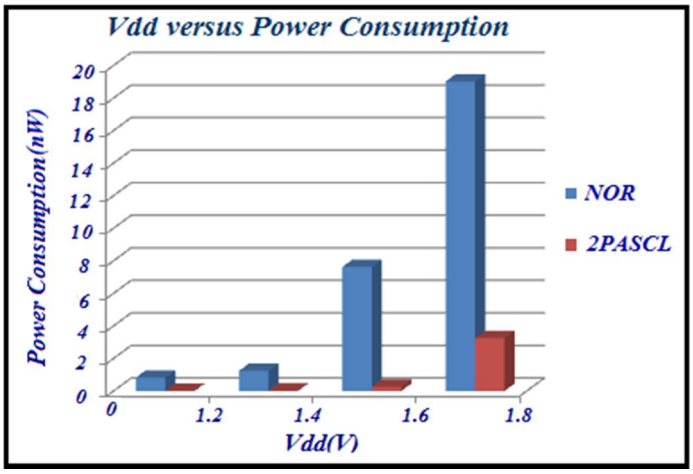

Fig22.Power Consumption comparison of proposed NOR vs NOR at Power supply in 180nm technology

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Table IX Power Consumption comparison of proposed NOR vs NOR at frequency in 180nm technology

Frequency(MHz)	Power Consumption(nWatts)	
	NOR	2PASCL
50	0.035	0.004
100	0.764	0.029
150	1.423	0.976
200	9.699	3.290

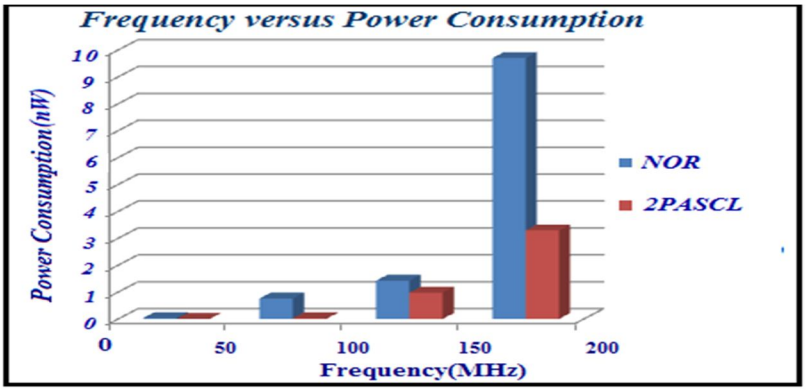

Fig23. Power Consumption comparison of proposed NOR vs NOR at frequency in 180nm technology

Table X Power Consumption comparison of proposed NOR vs NOR at capacitance in 180nm technology

Capacitor(fF)	Power Consumption(nWatts)	
	NOR	2PASCL
20	0.137	0.004
30	0.249	0.027
40	1.235	0.196
50	2.050	0.987
60	3.721	1.440

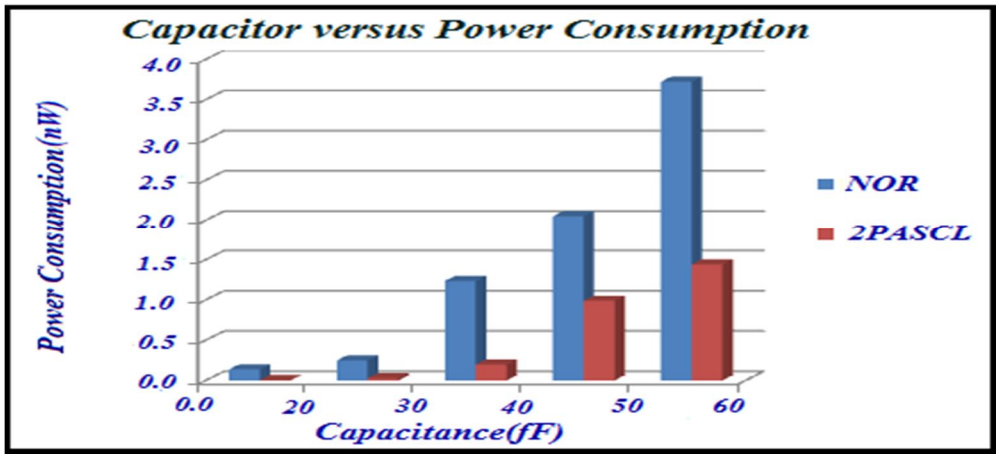

Fig24. Power Consumption comparison of proposed NOR vs NOR at capacitance in 180nm technology

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Table XI Power Consumption comparison of proposed NOR vs NOR at Power supply in 90nm technology

V_{DD}(Volts)	Power Consumption(nWatts)	
	NOR	2PASCL
1.2	0.082	0.007
1.4	0.123	0.016
1.6	1.613	0.276
1.8	2.015	1.240

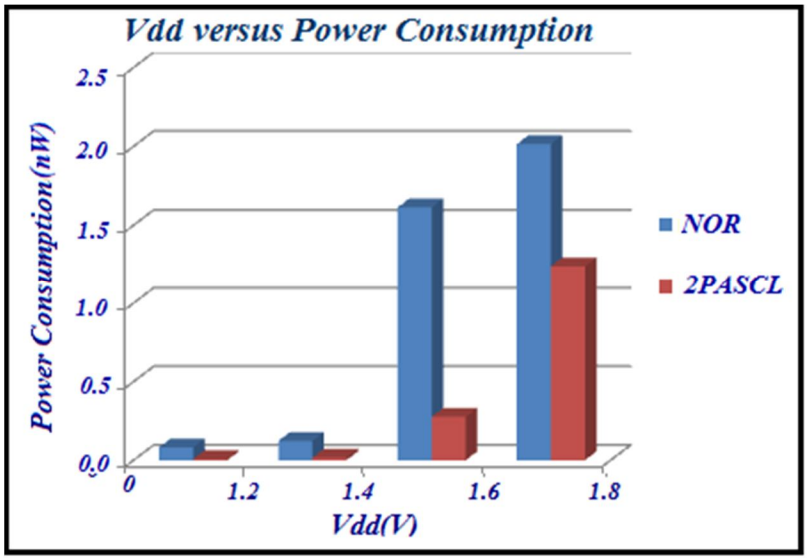

Fig25. Power Consumption comparison of proposed NOR vs NOR at Power supply in 90nm technology

V.CONCLUSION

Simulation results obtained from the proposed inverter and NAND/NOR gate has wide acceptance in low power VLSI regime at low frequency. The comparison of the proposed circuit with other traditional methodologies has proved that power consumption with the proposed logic is far less as compared to CMOS, PFAL and 2PASCL based technique. The simulation result show that power consumption of proposed NAND/NOR is less compare.

VI. ACKNOWLEDEMENT

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REFERENCES

[1] N. Waste and K. Eshraghian, Principle of CMOS VLSI Design: A System Prospective, 2nd ed. New York: Addison – Wesley, 1993
[2] W. C. Athas, L. J. Svensson, J. G. Koller, et al., "Low-power digital systems based on adiabatic switching principles," IEEE Trans. On VLSI systems, 2(4), Dec. 1994, pp: 398-4
[3] S. Samanta "Adiabatic Computing: A Contemporary Review," International conference on computers and devices for communication, Dec. 2009, pp. 1-
[4] J. Marjonen, and M. Aberg, "A single clocked adiabatic static logic – a proposal for digital low-power applications," J. VLSI signal processing, vol.27, no.27, Feb.2001, pp.253-26
[5] M. Pedram, "Power minimization in IC design: principles of applications," ACM Transactions on Design automation of Electronic System, 1(1) Jan 1996, pp 53-5
[6] A. Vetuli, S. Di Pascoli, and L.M. Reyneri, "Positive feedback in adiabatic logic, Electron.Lett"vol.32, Sept. 1996, pp.1867- 1869.
[7] A. Blotti, M. Castellucci, and R. Saletti, "Designing carry lookahead adders with an adiabatic logic," standard-cell library," in proc. 12th Int. Workshop PATMOS, Seville, Spain, Sept. 2002, pp. 118-127
[8] E. Amirante, A. Bargagli-Stoffi, J. Fisher, G. Iannaccone, and D.Schmitt-Landsiedel, "Variations of the power dissipation in adiabatic logic gates." Inproc. 11th Int. Workshop PATMOS, Yverdon-Les_Bains, Switzerland, Sept. 2001, pp. 7 – 10

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[9] Y. Takahashi, Y. Fukuta, T. Sekine and M. Yokoyama, "2PADCL: Two phase drive adiabatic dynamic logic CMOS logic." Proc. IEEE APCCAS, Dec. 2006, pp. 1486-1489
[10] N. Anuar, Y. Takahashi, T. Sekine, "Two phase clocked adiabatic static CMOS logic," proc. IEEE SOCC 2009, Oct. 2009, pp. 83-86.
[11] S. Kang and Y. Leblebici, "Low Power CMOS Digital Logic Circuits", 3rd ed., Tata McGraw Hill, 2003.
[12] N. Anuar, Y. Takahashi, T. Sekine, "Two-Phase clocked adiabatic static CMOS logic and its logic family" Journal of semiconductor technology and
[13] science, vol 10, no. 1, Mar. 2010, pp. 1-10. 463.A. P. CHANDRAKASAN, S. SHENG, AND R. W. BRODERSEN, "Low Power CMOS Digital Design," IEEE Journal of Solid-state Circuits, Vol. 27, No. 04, pp. 473-484, April 1999
[14] J. M. RABAEY, AND M. PEDRAM, "Low Power Design Methodologies," Kluwer Academic Publishers, 2002. Publishers, 2002.
[15] Vetuli, A., Di Pascoli, S., Reyneri, L.M.: Positive feedback in adiabatic logic. Electronics Letters, Vol. 32, No. 20, Sep. 1996, pp. 1867ff.
[16] Blotti, A., Di Pascoli, S., Saletti, R.: Sample Model for positive feedback adiabatic logic power consumption estimation. Electronics Letters, Vol. 36, No. 2, Jan. 2000, pp. 116-118.
[17] Atul Kumar Maurya, Gagnesh Kumar, "Energy efficient adiabatic logic for low power VLSI applications", 2011 International Conference on communication systems and network technologies.

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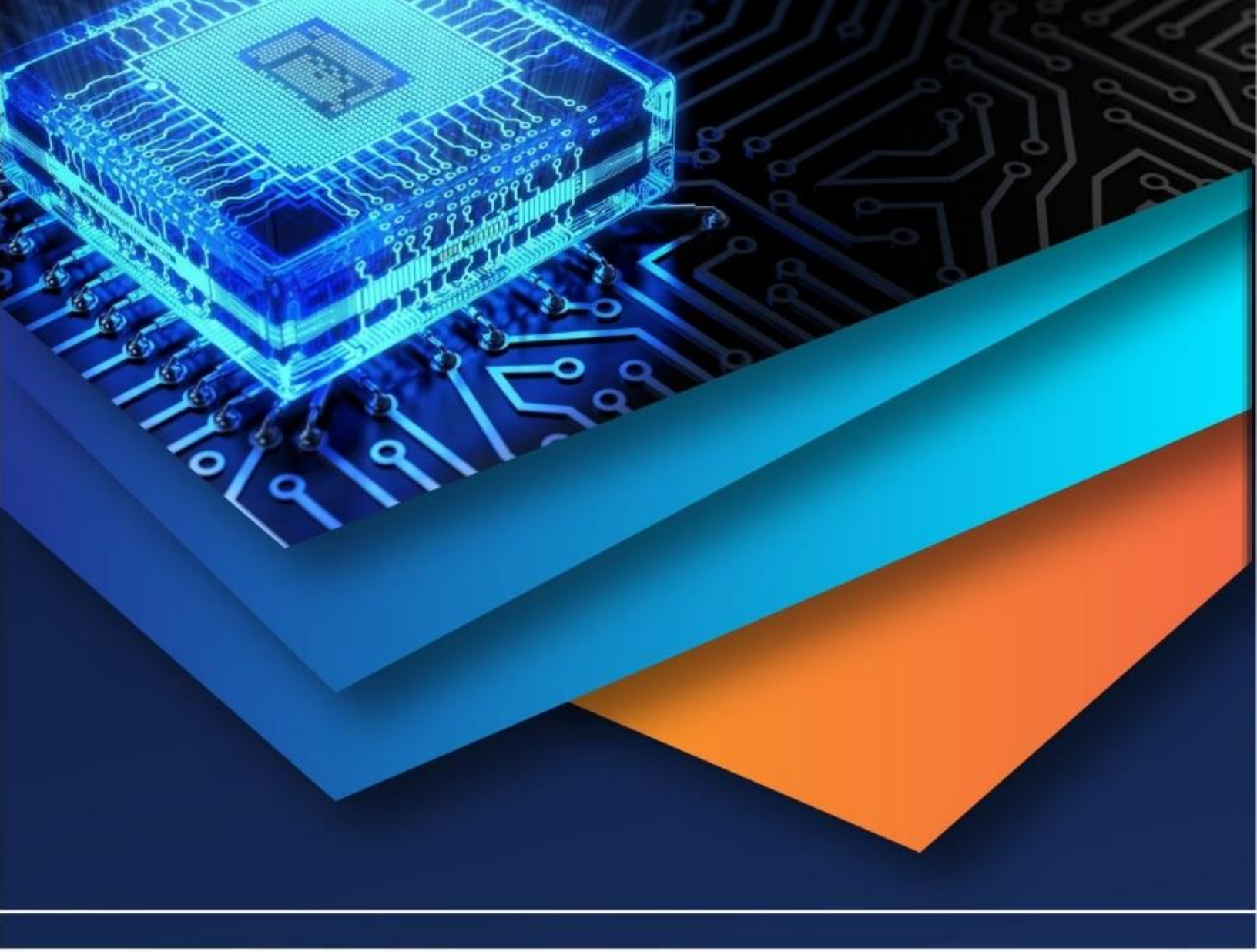

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