INTERNATIONAL JOURNAL
FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Power Efficient Carry Select Adder using 4T XNOR Gate

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Abstract: Adders are the basic elements used in complex data processing for efficient VLSI design. The Carry select adder circuit is used for the design of high speed processors. There is scope for decreasing the power consumption of the design while preserving the speed of the circuit in CMOS technology. In this paper 4transistor XNOR gate is used to design the hybrid CMOS Full Adder circuit. The CSA circuit is designed using this hybrid CMOS Full Adder circuit for 8-bit.In this paper the carry select adder is designed through 130nm CMOS process technology and implemented using Mentor Graphics tool.

Keywords: Mentor Graphics, carry select adder, CMOS, VLSI design

I. INTRODUCTION

The low power, area efficient and high speed logic data path system design is the interesting areas of research in VLSI. There are different adders which are used for different applications depending on the requirement. One of the basic adders is Ripple carry adder (RCA), but main drawback is its carry propagation delay. The designs of carry look ahead adder (CLA) adder and carry select adder(CSA) are the recommended circuit design for the reduced carry propagation delay. The conventional carry select adder uses the regular CMOS XNOR gate as the building block in designing the full adder, has more number of transistors and the power consumption. The modified carry select adder uses the 4transistor XNOR gate in designing the full adder which is of less area and power consumption. The carry-select adder generally consists of two n-bit numbers. A carry-select adder is done with two adders (therefore two ripple carry adders), in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one. After the two results are calculated, the correct sum, as well as the correct carry out is known through the multiplexer.
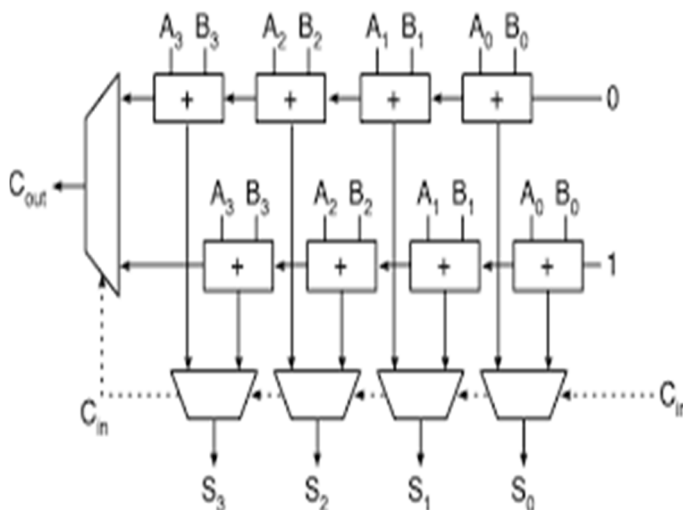

Fig.1 4bit carry select adder

Above is the basic building block of a carry-select adder, where the block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result. Further for 16bit three such ripple carry blocks with one four bit RCA block as first section. Each section's carry out

will be the carry in for the next section which will select the appropriate RCA for final out. The section will grows similarly for higher bit CSLA design.

II. EXISTING SYSTEM

Many research authors have done successful work regarding the optimization of area and power efficient FA and carry select adder with CMOS full adder block sections inside the ripple carry adder blocks. In this process complimentary pass transistor logic based, pseudo logic based, hybrid full adder using XNOR-XNOR logic gates based full adder has been proposed. Theexisting 3T XNOR gate is shown in the figure2

The Existing circuit has low power and is area efficient but the main drawback is threshold voltage drop
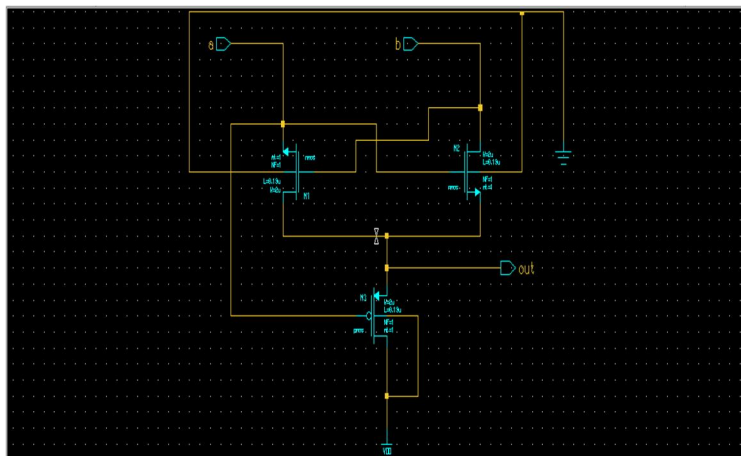

Fig.2 3T XNOR circuit

across the NMOS transistor. Because of this, full voltage swing is not possible at the output for the two combination input. The size of the PMOS transistor increased to get the full voltage swing at the output. The W/L of PMOS is increased to 2uM/700nM so that the switching frequency of PMOS is reduced that of NMOS which will gives the full swing voltage at the output.

III. PROPOSED SYSTEM

The modified carry select adder consists of 4transistor XNOR gate as building block for the full adder circuit based on the pass transistor logic. A Hybrid CMOS full adder is designed using the 4transistor XNOR circuit. Fig. 3 shows the 4transistor XNOR circuit. Based on the pass transistor logic the 4transistor XNOR circuit is designed. For the design of full adder the XNOR operation is performed twice. To improve the performance of the any design the key factor is to reduce the number of p transistors than the n transistors.
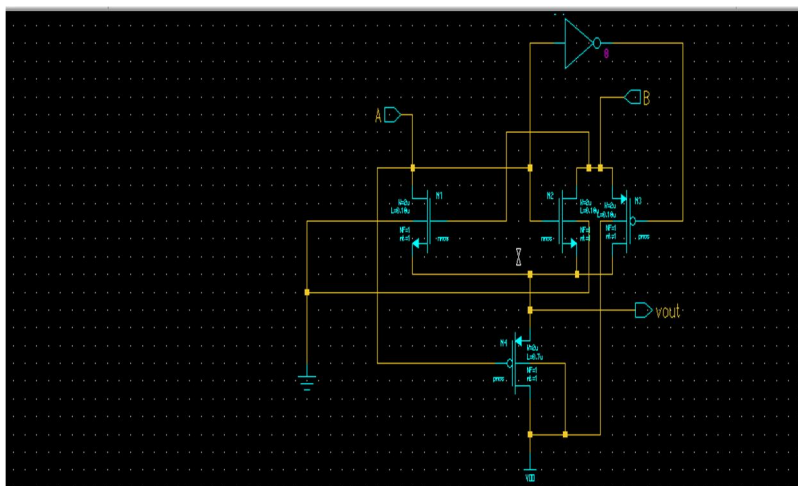

Fig.3 4T XNOR circuit

This full adder design is used in ripple carry adder block for the carry select adder. Boolean expressions for the sum and carry are:

$$\text{Sum} = ((A\ \text{XNOR}\ B)'\text{XNOR}\ C)'\ ;\ \text{Carry} = AH'+CH$$
$$\text{where} = (A\ \text{XOR}\ B)'\ \text{Fig.5 shows the construction of full adder using 4T}$$

This full adder design is used in ripple carry adder block for the 8-, 16- and 32-bit carry select adder. Fig. 3 shows the full adder circuit. The Boolean expression for the sum and carry are
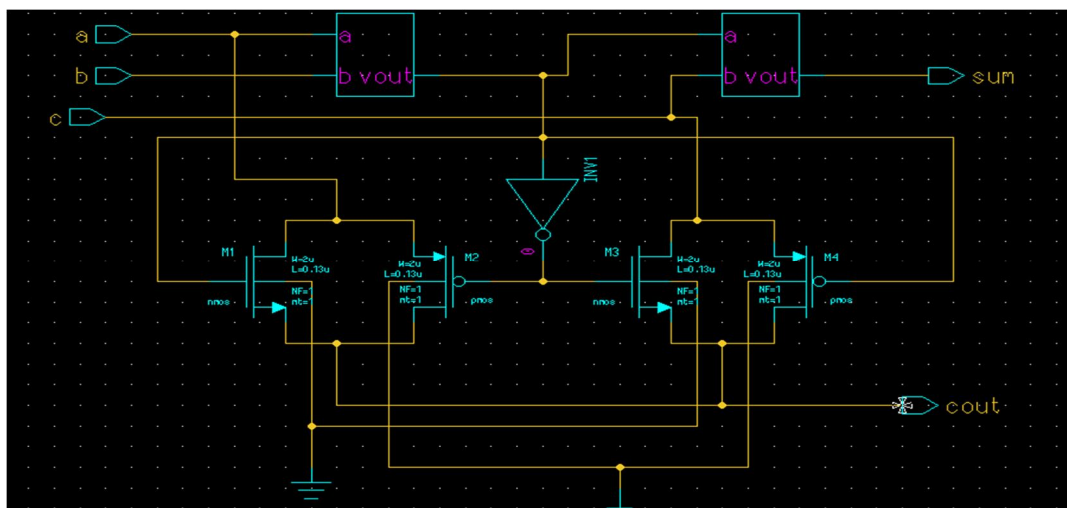

Fig.4 full adder using 4T XNOR gate

Carry select adder The modified carry select adder circuit is as shown in Fig. 5 The proposed design contains two ripple carry adder blocks with carry in as C =0 and C =1. The proposed carry select adder using full adder contains 4blocks: The block named RIPPLE18061is a Ripple Carry Adder designed using full adder circuit which produces S1, S2……..S8 with C=0 as carry in and carry bits generated are fed to the next blocks of FA circuits in the RCA block. Carry out is fed to the Multiplier circuit for the selection of final sum. The block named RIPPLE18062 a Ripple Carry Adder same as the previous RCA block which produces S1, S2….S8 with C=1 as carry in and carry out is fed to Multiplier circuit for the selection of final sum. The block named B4M11 a 16 to 8 Multiplier block with inputs as carry bits of both RCA blocks, which is used to select the carry out depending on the select line The remaining block is a 2to1 multiplier block that select one of the carry outputs of the two ripple carry adders
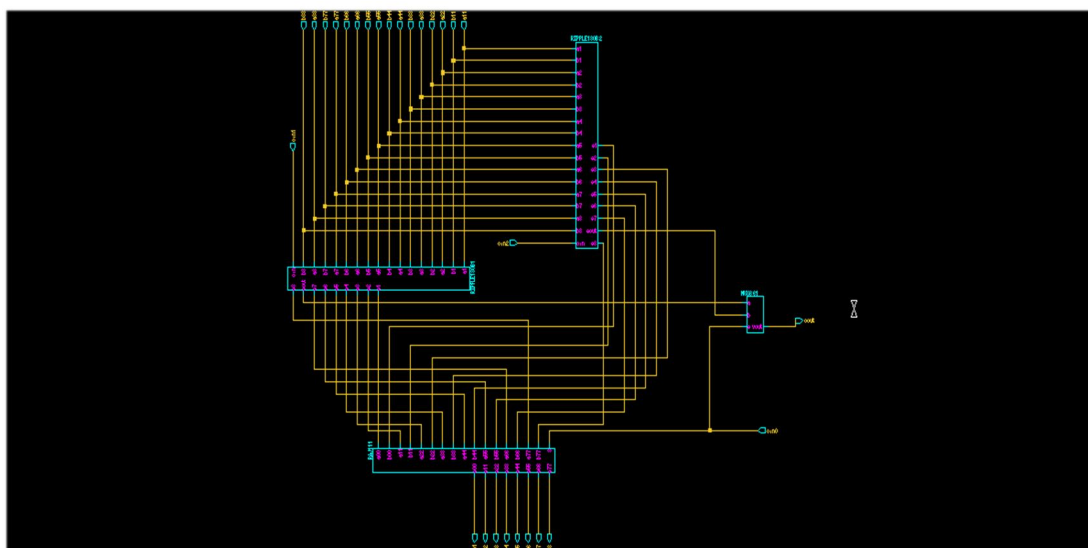

Fig.5 8-bit carry select adder

IV.   SIMULATION RESULTS

The proposed work is simulated using Mentor Graphics 130nm CMOS process technological library. The modified CSLA is made to compare with that of the regular CSLA and with the previous CSLA design 3T XNOR circuit. The existing circuit has the voltage degradation, one PMOS is used to form transmission gate this will give the full swing voltage at the output. The modified XNOR circuit is having full voltage swing at the output with increased W/L of the PMOS. Here the width of the PMOS is increased to 700nm to get the full voltage swing at the output

The following table compares the performance of both 3T and 4T XNOR gates

A(volts)	B(volts)	Expected output(volts)	3TXNOR output(volts)	Modified XNOR output(volts)
0	0	5	5	5
0	5	0	1.5	0
5	0	0	0	0.25
5	5	1	4.5	5

Table1.Performance table of 3T XXNOR and 4T XNOR circuits

The existing 3T XNOR has less area and power consumption compared to regular XNOR circuit but the disadvantage is degraded output. The proposed 4T XNOR circuit has less area and power consumption compared to regular XNOR but slight increase in area of the circuit due to one PMOS compared to 3T XNOR with full voltage swing at the output and with less power consumption. It is of power efficient circuit used to design the efficient full adder circuit and 8-, 16-, 32-bit CSLA circuit
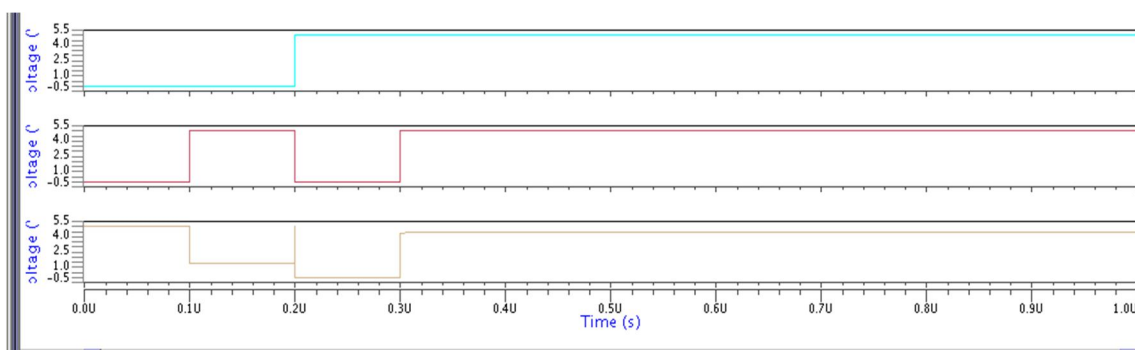

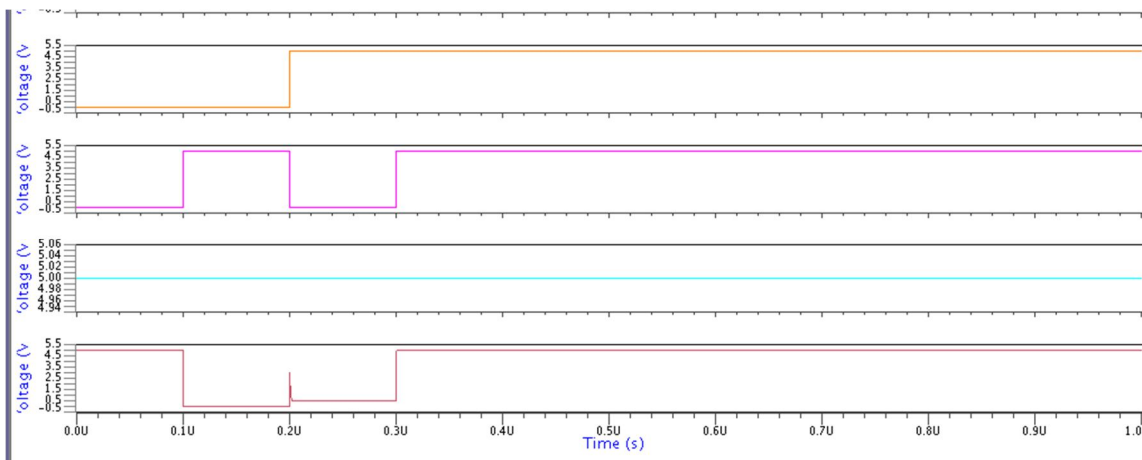Fig.6 3T XNOR output waveforms

Fig.7 4T XNOR output waveforms

The following table shows the power dissipation values for 3T XNOR based full adder and 4T XNOR based full adder as well as for 3T XNOR gate and 4T XNOR gates respectively

Name of the circuit	Power dissipation(nW)
3T XNOR gate	152.5591
4T XNOR gate	50.6971
Full adder using 3T XNOR gate	252.1290
Full adder using 4T XNOR gate	73.295

The following figure shows the output waveforms for the addition of two 8-bit numbers11110000 and 10101010
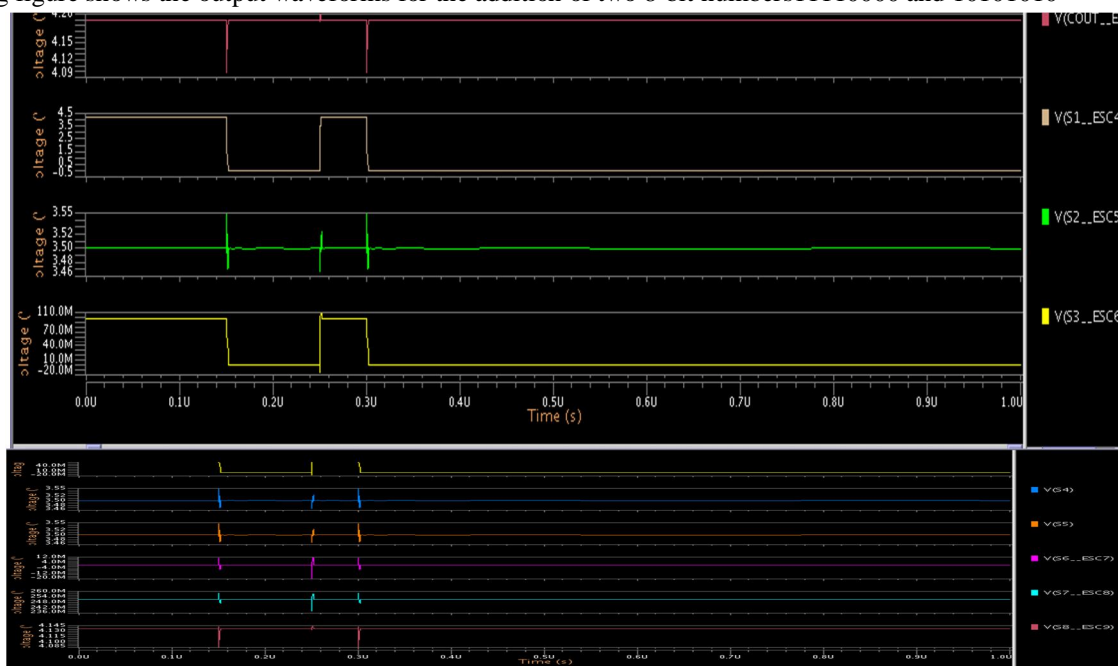

Fig.8 output waveforms for 8-bit CSA

V. CONCLUSION

In this proposed work, 8bit regular carry select adder and the existing 3T XNOR based CSA and modified CSA are analyzed for the parameters like area and power consumption. The proposed work can be further implemented for the higher bits depending on the application. The proposed work is having slight increase in the area but is of power efficient adder circuit with full voltage swing at the output. The adder can be further implemented for 16-bit, 32- bit,64-bit,128-bit and even for 256-bit CSA by using the optimization method to reduce the power area and delay of the circuit.

VI. FUTURE SCOPE

The work is done for the implementing 8-bit word size and is of power and area efficient circuit compared to the regular Carry select adder. This work can be extended further for high bit word size and also different optimization techniques can be applied to reduce the area power and delay of the circuit.

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