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Design of a Low Power and High Speed Comparator using Mux based Full Adder Cell for Mobile Communications

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Abstract: ***The implementation of a comparator (1-bit) circuit using a MUX-6T based full adder cell is designed with a combination of multiplexing control input and Boolean identities. The proposed comparator design features a higher computing speed and lower energy consumption due to the efficient MUX-6T adder cell. The design adopts multiplexing technique with control input to alleviate the threshold voltage loss problem which is commonly encountered in Pass Transistor Logic (PTL) design. The design proposed successfully embeds the buffering circuit in the full adder design which helps the cell to operate at lower supply voltage compared with the other related existing designs. It also enhances the speed of the cascaded operation significantly while maintaining the performance edge in energy consumption. In this design the transistor count is minimized. For performance comparison, the proposed MUX-6T comparator is compared with existing full adder based comparator using cadence tool. The simulations are performed for 45nm and 90nm technologies; indicate that the proposed design has the lowest energy consumption along with the performance edge on both speed and energy.***
Keywords: MUX, comparator, full adder, pass transiator logic, cadence.

I. INTRODUCTION

Comparators are widely used in electronic circuits after operational amplifiers. They are also mostly popular as 1-bit analog-to digital converters. Analog to digital conversion efficiency mainly depends on the input sampling process. Comparator determines the digital equivalence of the analog signal with the help of its sampled input. In today's world, portable battery operating devices are growing rapidly due to the low power methodologies predominance in high speed applications. Power minimization can be attained by inching towards feature size reduction techniques (Etienne and Sonia, 2007a). The Short Circuit Channel (SCE) effect due to feature size reduction introduces various non-idealities and other process variations that affect the entire performance of the device. In analog-to-digital converters low noise margin, low power dissipation, low hysteresis, less offset voltage and high speed is essential for portable and mobile communication devices. The design of comparators with low power consumption, low offset along with the high speed forms the major interest in research today to achieve overall higher performance of ADCs. In the past, pipeline and flash based ADC architectures implement comparator based pre-amplifier designs. Offset voltage becomes a major constraint in pre-amplifier based comparators. Dynamic comparators are an alternative to overcome this problem to make a comparison during every clock cycle and need much low offset voltage. However, the power consumption is very high in dynamic comparators in comparison with the pre-amplifier based comparators. The major drawback of these dynamic comparators is the fluctuating output signal from the latch stage during clock transitions. This is due to the noise occurrence at the input terminals. The proposed converter design using multiplexer based full adder cell topology eliminates the noise at the input and reduces the power consumption and delay. Comparator is the fundamental and performs a predominant role in the arithmetic unit of digital systems and there are numerous topologies available in the design of CMOS comparators with different operating speed, noise margin, complexity and its power dissipation. In this study comparator design implementation is done by full adder which is the basic functional blocks of the digital VLSI circuits. Several enhancements in approaches have been rendered related to its structure since its invention even one can implement the comparator by flattening the logic function directly too. The main concern of such refinements is to reduce the transistors count which intern increase the speed of operation and minimize the power consumption. One of the major advantages in reducing the transistor count is to increase the fabrication density of a single chip thereby reducing the total chip area. In digital system arithmetic, magnitude comparators are used for comparison. Magnitude comparator is a

combinational circuit which compares two binary numbers for e.g., A and B and then their relative magnitude is determined and outcome is specified by three states which indicate whether A<B, A=B and A>B shown in Fig. 1. This research work focuses on designing a high speed and low power magnitude comparator (1-bit) using MUX based full adder cell. The magnitude comparator with two inputs namely A and B consist of full adder, inverters at one of the input and AND gates at the output. The threes outputs are for various combinations of its inputs and its truth table as shown in Table 1.

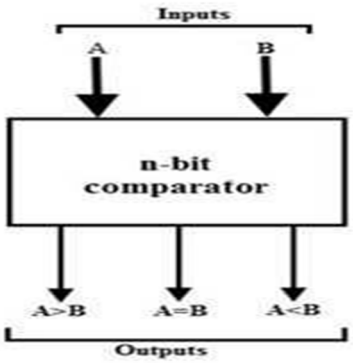

Fig.1. Block diagram of a comparator

INPUTS		OUTPUTS		
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

II. REVIEW FOR COMPARATOR DESIGN

Many researchers in the recent past aim to focus on numerous approaches towards CMOS comparator design implementations using various logic styles that were incorporated in formulating a uniform method of design. In CMOS comparator design power consumption, speed and circuit area become the major criteria of concern. However, the design methodology constraint in CMOS forms a major bottleneck scenario in the circuit design of comparators. To overcome this each individual parameter performance criteria are analysed, estimated, along with their behavior to build-up both qualitative and quantitative apprehension of numerous designs were presented in the literature. Different comparator (1-bit) designs have been introduced by researchers using conventional CMOS, PTL, GDI, TG and hybrid logic styles. Comparator (1-bit) design using conventional CMOS consisted of 42 transistors, PTL comparator design consisted of 18 transistors, GDI comparator design consisted of 16 transistors, TG comparator design consisted of 36 transistors and hybrid comparator design consisted of 17 transistors. Comparator forms a fundamental functional unit of an Arithmetic and Logic Unit (ALU) in ASIC's and Digital Signal Processors (DSPs) used in mobile communication applications. Various concepts in CMOS comparator design with the help of numerous design logic methods were presented by researchers in the literature. Power consumption, speed and chip area are the three major estimates in predicting the overall performance of a CMOS comparator design (Etienne and Sonia, 2007b). However, these estimates conflict with one another i.e., each individual estimate can't be optimised independently (Anjali ET AL., 2013). Hybrid comparator (1-bit) design consisting of 17T by using GDI and PTL logics was introduced. The design of comparator (1-bit) consisted of 8 PMOS and 9 NMOS. The hybrid comparator (1-bit) design was based on 9T full adder cell. PTL and GDI logic was implemented in the design of the full adder module. Full adder cell was used as the basic building block in the design. The hybrid logic used in the design of full adder

suffers from switching delay and thereby causing additional propagation delay along with switching penalty. The design performance was evaluated by simulating BSIM-3 and BSIM-4 models. Hybrid PTL and GDI logic used in the design introduced additional complexity in the circuit there by degrading the overall performance. Considering three different approaches in the design of CMOS comparator (1-bit), The focus was on auto-generated, semi-custom and full-custom based layout designs. Auto generated approach is easy to design but takes more area and consumes less power than semi-custom design approach. Semi-custom design takes less area but consumes much more power than auto generated design. Finally, full-custom design takes less area and consumes less power than both auto generated and semicustom design. Full-custom design is more efficient in terms of chip area and power consumption when compared with auto generated design and semi-custom design. The work didn't highlight on comparator's performance as the approach was mainly restricted to different types of layout generation. Comparator (1-bit) design using four 10T GDI full adder cells was implemented by Anjali and Pranshu (2014). GDI full adder cell, XOR-XNOR cell included 6 transistors. GDI XOR-XNOR output is used to generate the carry and sum of the full adder cell. The comparator (4-bit) consisted of 28 NMOS and 28 PMOS which is less when compared with the other comparator (4-bit) designs using CMOS, PTL and TG logic. The comparator (4-bit) consisted of four full adder cells designed by using GDI logic. Two hexadecimal inputs were used to generate two 4-bit binary outputs. In cascade four AND gates were used to generate A=B output of the comparator (4-bit). Output sum of first full adder acted as one of the input to the first AND gate. Output carry of first GDI Full adder acted as a C_{IN} input of the succeeding full adder. Output carry of last full adder acted as B>A output of the comparator (4-bit). The GDI logic introduces power overhead due to more number of PMOS transistors used in the design and need restoration logic to improve the performance in cascade. Comparator (2-bit) design was introduced by Rachana ET AL. (2016) using hybrid full adder module. The design included 16 transistors. The design was validated by comparing it with the conventional CCMOS, CPL, TGA and TFA based adder modules by using Tanner EDA Tools 13.0. TG and CMOS combination was used in the hybrid logic design of full adder. Sum and carry signals were generated using XNOR modules. The XNOR module consumed more power in the adder design. In order to compare two numbers in digital systems, magnitude comparators were used. The hybrid logic used in the full adder design introduces additional propagation delay along with need of higher switching activity. Agarwal and Kaur (2015) introduced magnitude comparator (2-bit) design by using CMOS, PTL and GDI logic. CMOS based comparator (2-bit) consisted of 88 transistors to provide three outputs i.e., A>b, A>B, A=B. PTL logic consisted of 28 transistors which are relatively less in numbers compared to the conventional CMOS. The GDI based design used three inputs: G i.e., gate which is common to NMOS and PMOS, P i.e., input to the source/drain of PMOS and N i.e., input to the source/drain of NMOS. The GDI cell consisted of only two transistors. GDI based comparator consisted of 30 transistors. Four XOR gates, two MUX and two AND gates were used in the design of full adder. The inverter at the input of XOR produces XNOR by using 3 transistors. The inverter used to produce XNOR consumes more area and high power consumption thereby degrading the design performance.

III. COMPARATOR DESIGN FOR MUX 6T

Proposed comparator (1-bit) is implemented using MUX-6T based full adder introduced by Ramana Murthy ET AL. (2012) consumes lower power than other logic styles described in the literature. The architecture of the proposed comparator is shown in figure. It consists of 6 transistors. Most of the existing adder design techniques have been considered along with its pros and cons in all the previous studies conducted (Ramana Murthy ET AL., 2014). The proposed adder is based on simplified Boolean identities along with multiplexing control technique with less number of transistors. The Boolean expressions for sum and carry of adder (1-bit) with 3-inputs A, B and C are given by expressions shown in Equations 1 and 2 respectively:

SUM = A'B'C + ABC + A'BC' + A'B'C' (1)

CARRY = AB + AC + BC (2)

IV. SCHEMATIC DIAGRAM

To obtain the three comparative outputs inverted input at the B input terminal is given to the full adder design and C input is connected to the ground. Carry output directly act as A>B output of the comparator (1-bit). For the A=B and B>A, different input combinations of AND gate has been used. For generation of B>A input combination for the AND gate is B and A1 and for the generation of A=B input combinations for AND gate is SUM and V_{DD} as shown in Fig. 13.

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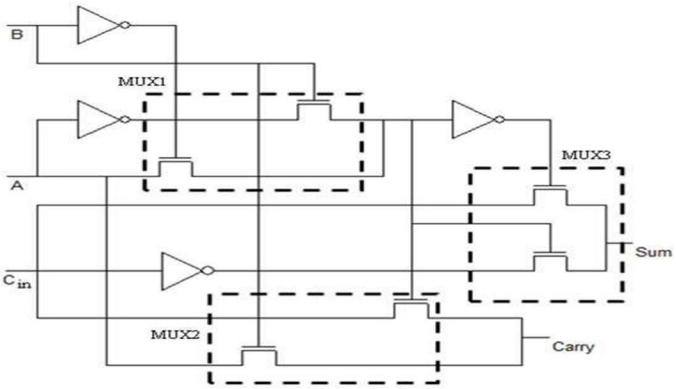


Fig.1. MUX 6T full adder

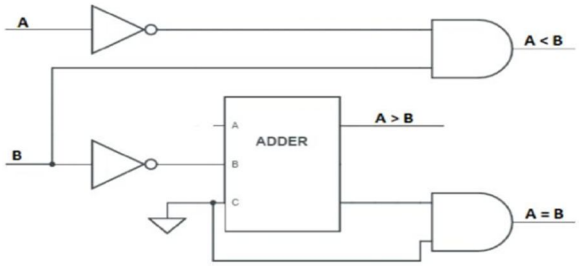
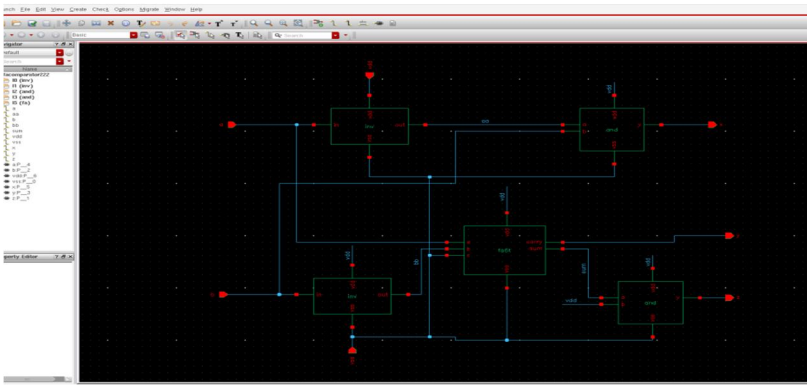
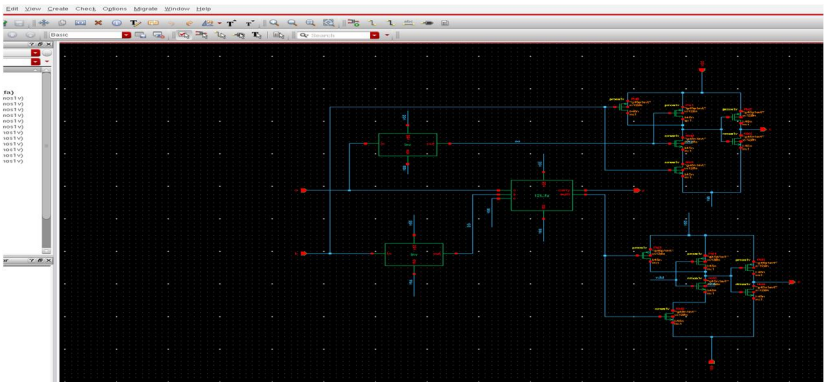


Fig.2. Full adder based comparator block diagram



comparator with MUX-6t based full adder in cadence schematic view



comparator with MUX-12t based full adder in cadence schematic view

V. SIMULATIONS

A. Layout Diagrams of Mux 6t

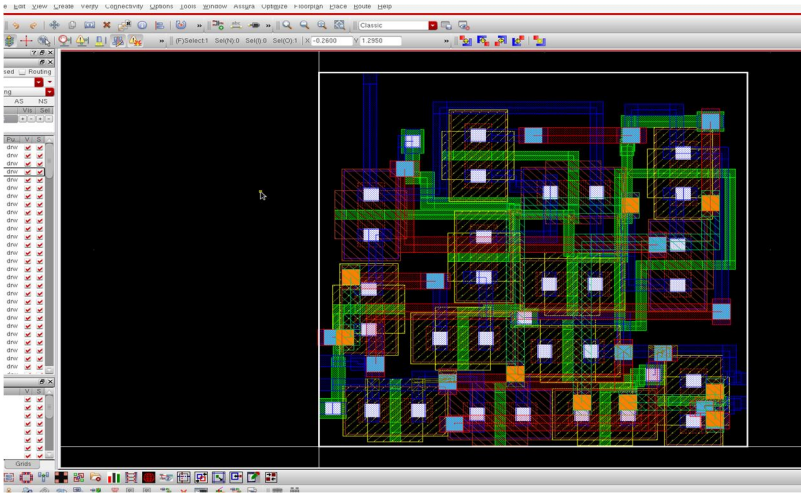


Fig.21. Layout design for 45nm MUX 6T full adder

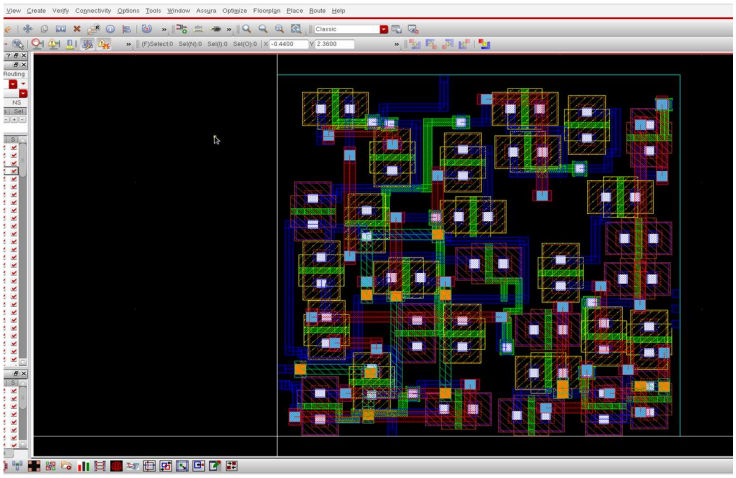


Fig.22. Layout design for 45nm MUX 6T comparator

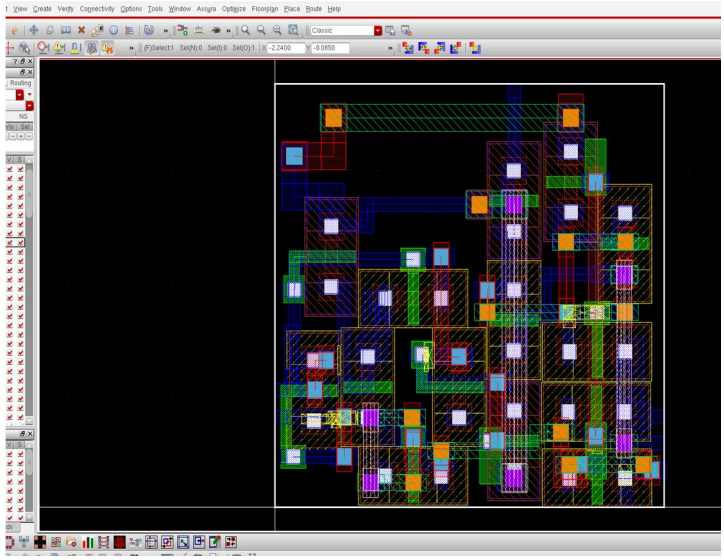


Fig.23. Layout design for 90nm MUX 6T full adder

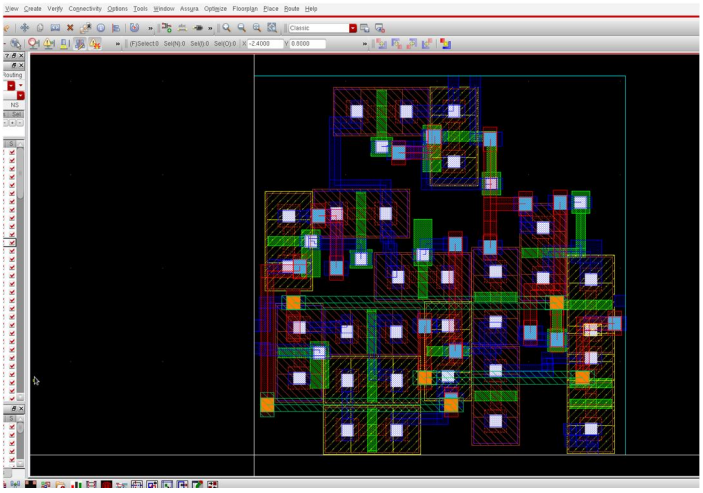


Fig.24. Layout design for 90nm MUX 6T comparator

1) Layout Diagrams of Mux 12t

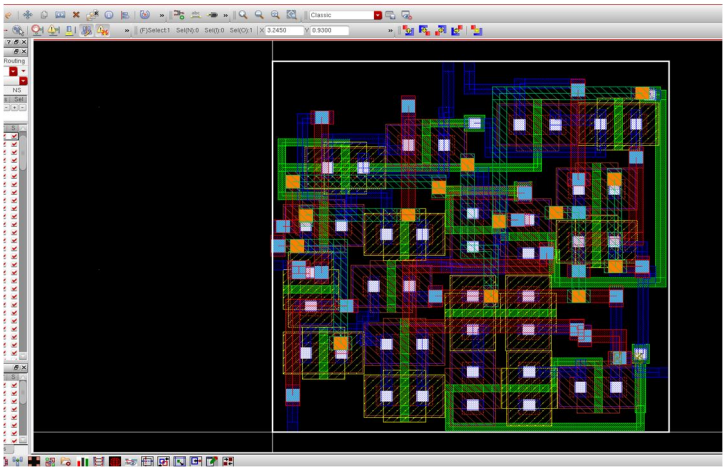


Fig.25. Layout design for 45nm MUX 12T full adder

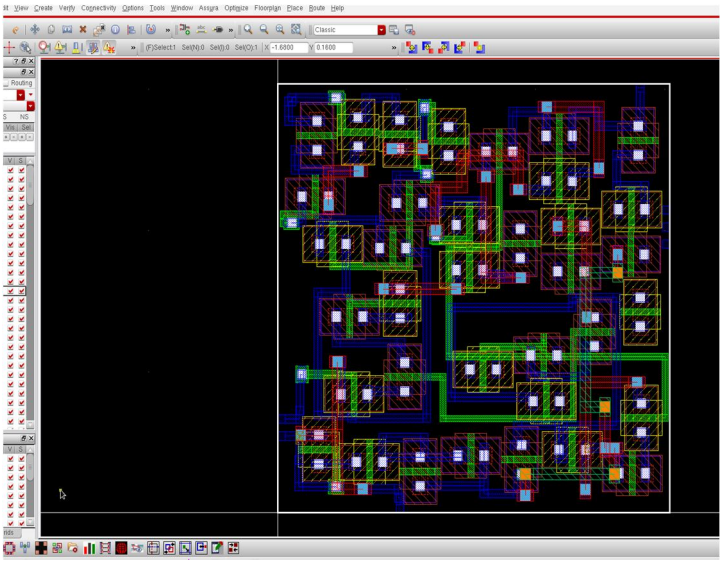


Fig.26. Layout design for 45nm MUX 12T comparator

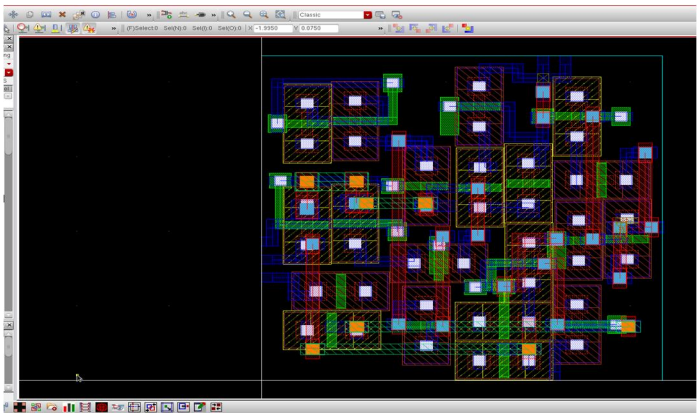


Fig.27. Layout design for 90nm MUX 12T full adder

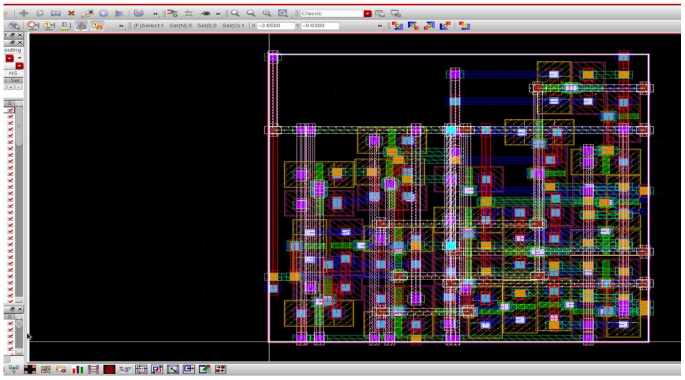


Fig.28. Layout design for 90nm MUX 12T comparator

B. Waveforms

1) Waveforms of Mux 6T

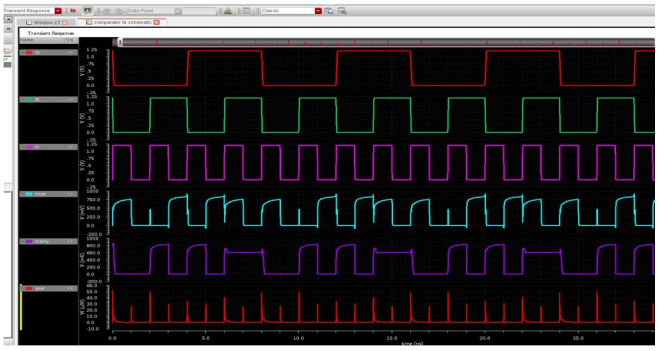


Fig.29. Output waveform for 45nm MUX 6T full adder

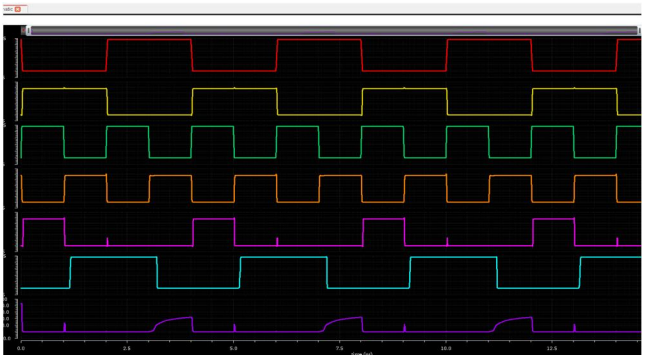


Fig.30. Output waveform for 45nm MUX 6T comparator

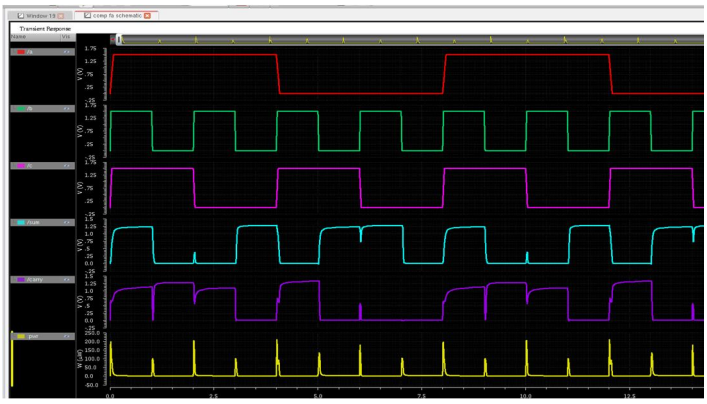


Fig.31. Output waveform for 90nm MUX 6T full adder

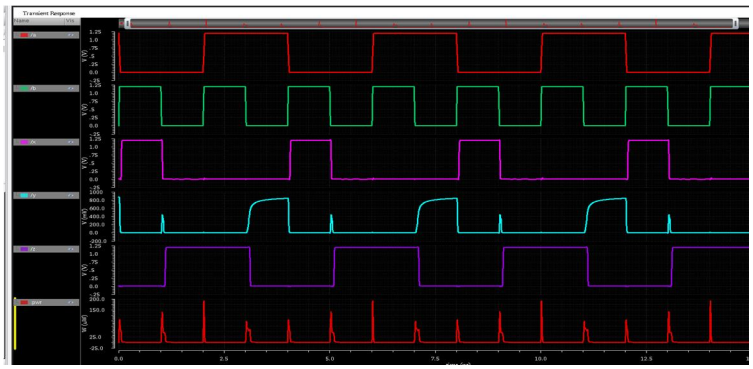


Fig.32. Output waveform for 90nm MUX 6T comparator

2) Waveforms of MUX 12T

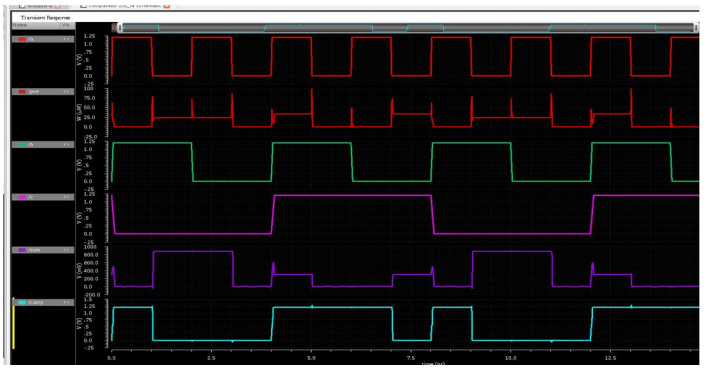


Fig.33. Output waveform for 45nm MUX 12T full adder

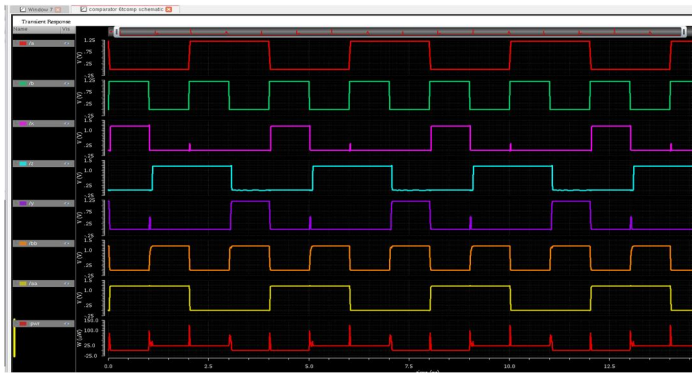


Fig.34. Output waveform for 45nm MUX 12T comparator

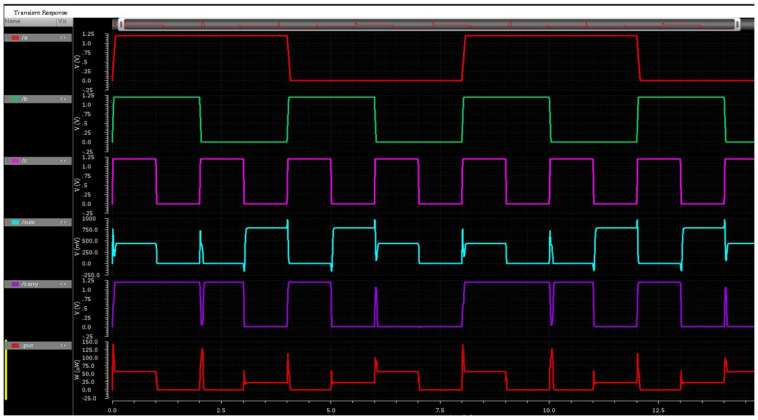


Fig.35. Output waveform for 90nm MUX 12T full adder

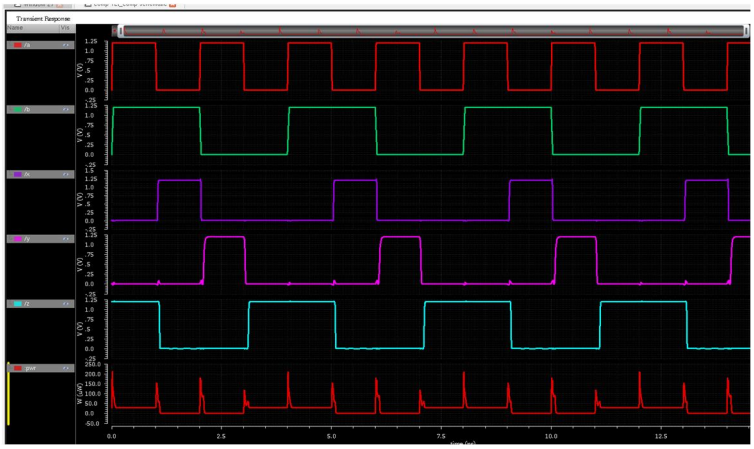


Fig.36. Output waveform for 90nm MUX 12T comparator

VI. RESULTS

The below results are observed when the comparative analysis of a 1-bit comparator using MUX based full adder cell with 6-tranisisors and 12-transistors and the comparator using mux-6t based full adder is more efficient in terms of area , power dissipation and delay.

TECHNOLOGIES USED		AREA	DELAY	POWER DISSIPATION
MUX-6T	45nm	3.61	29.86 ps	2.384 µW
	90nm	16.48	43.74 ps	6.282 µW
MUX-12t	45nm	9.241	2.020 ns	14.70 µW
	90nm	33.64	2.025 ns	21.52 µW

VII. CONCLUSION

In this study, a MUX-6T adder cell based comparator (1-bit) has been proposed. The MUX-6T comparator (1-bit) along with four other existing adder cell based comparators is designed by using Cadence tool. The MUX 6-T comparator (1-bit) is compared with the previous researcher's designs at 90 and 45nm feature sizes. The MUX-6T comparator (1-bit) shows better performance in terms of area, power and PDP. The transient simulation of the MUX-6T comparator (1-bit) is performed to validate the design. Furthermore, the MUX-6T comparator (1-bit) is compared to the MUX-12T existing full adder based comparator simulated values for power, propagation delay, PDP and area. The simulation results show better performance than the other MUX-12T existing full adder based comparator circuits. This shows that the MUX-6T comparator (1-bit) may be suitable to use at low power and high speed mobile communication applications.

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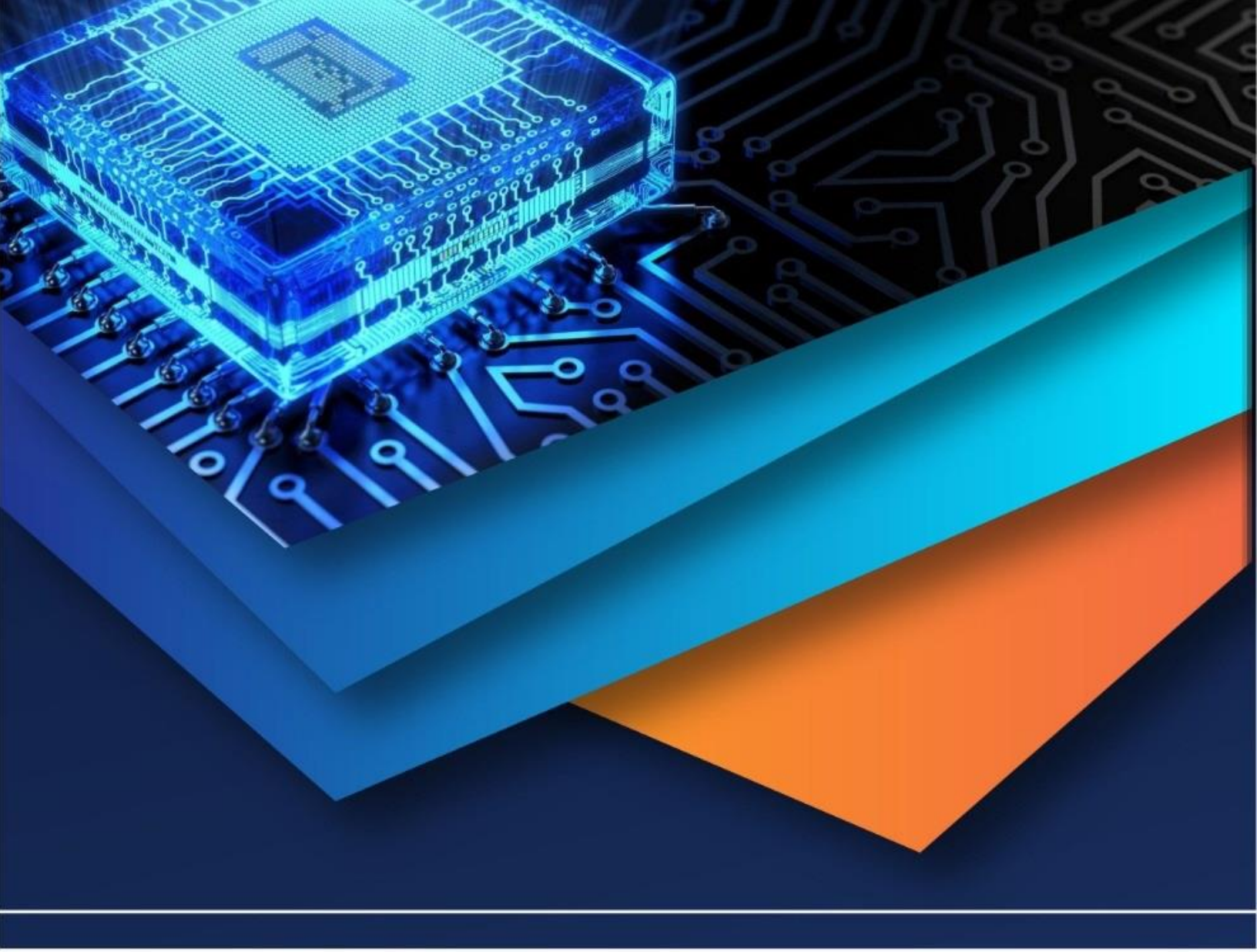

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