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Hybrid Model of 64- Bit Adders and Subtractors

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***Abstract*: The increasing demand of large memory devices and electronics circuit with small area and high speed of processing increase the popularity of these device . For large memory devices there will be higher bit addition subtraction like 64-bit addition\subtraction and 128 –bit addition subtraction. This paper include the designed model of 64- bit adder , subtractor, hybrid adder and the compression of their different parameters by using Xillinx 8.2 software. CMOS logic, transmission gate logic and pass transistor logic are used**

Keywords: Ripple Carry Adder (RCA),Carry Look ahead Adder (CLA), Ripple Borrow Adder (RBA), Input Output Bounded (IOB), Select Line (SL).

I. INTRODUCTION

Adder and subtractor are the basic building block of memory device and electronics devices. There are different type of adder and subtractor like:-

A. Carry Look Ahead (CLA)

It is the fastest method of adding numbers. This method is simple because it does not require the carry signal to propagate stage by stage. This type of adder reduces the time to calculate carry and make the process fast. A additional logic term will be used in design, so more hardware will be required. It is drive from the ripple carry adder. But there is a large delay problem in ripple carry adder. This problem is solved out by CLA.

B. Ripple Carry Adder (RCA)

A ripple carry adder is a logic circuit in which the carry outputs of each full adder become input of next full adder. It is called a ripple carry adder because each carry bit rippled the every next stage of full adders.

C. Ripple Borrow Subtractor (RBS)

Ripple borrow subtractor is a circuit which is used to perform subtraction of three input bits, it has three inputs a, b and borrow and two outputs d (difference) and borrow out (borrow) in this case each borrow is rippled into the every next stage of full adder.

D. Hybrid Adder (HA)

A Hybrid model can be designed By combining two adder circuit or by combining adder and subtractor circuit. This type of model is designed to reduce delay and area size. In this type of adder one circuit work as multi-function circuit.

II. PROPOSED MODEL

Different type of 64-bit adder and subtractor has been simulated. Like carry look ahead adder, ripple carry adder, ripple borrow subtractor and their hybrid model like hybrid model of carry look ahead and ripple carry adder, and hybrid model of adder and subtractor has also designed . on the base of which, different RTL design and their waveforms are generated, that is shown below. After studying their performance it will be decided that which model is better. Xillinx software just design a RTL view of model as the input given. It just show the structure of model which input, output and signal are programmed. In result it create a waveform which describe the whole working of model. It generates a log table also in which it summarised the various parameters. On the base of which it will be decided that it is costly or not, or it is complex or simple, or it is large in size or small in size.

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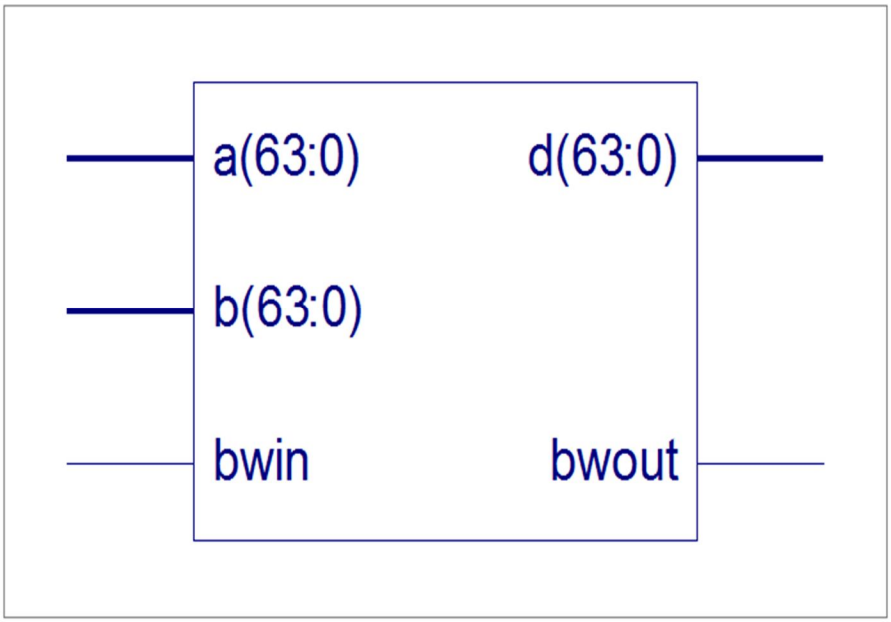

Figure 1. Ripple Borrow Subtractor.

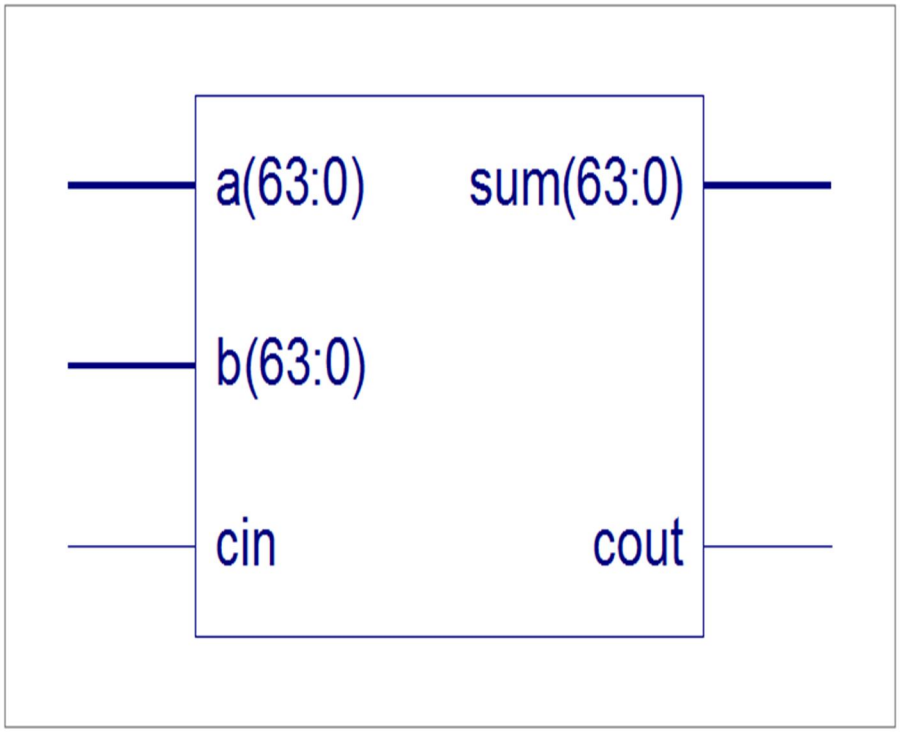

Figure 2. Carry Look Ahead Adder.

Here: a(63:0), b(63:0), cin – 64 bit inputs of carry look ahead adder.
Cout- Carry output of carry look ahead adder.
Sum (63:0) – 64 bit output after adding inputs.
This is RTL model of Carry Look Ahead Adder. RTL model of ripple carry adder and carry look ahead adder are same that's why we just mention here RTL of carry look ahead adder. But the output waveforms are different because of different inputs.

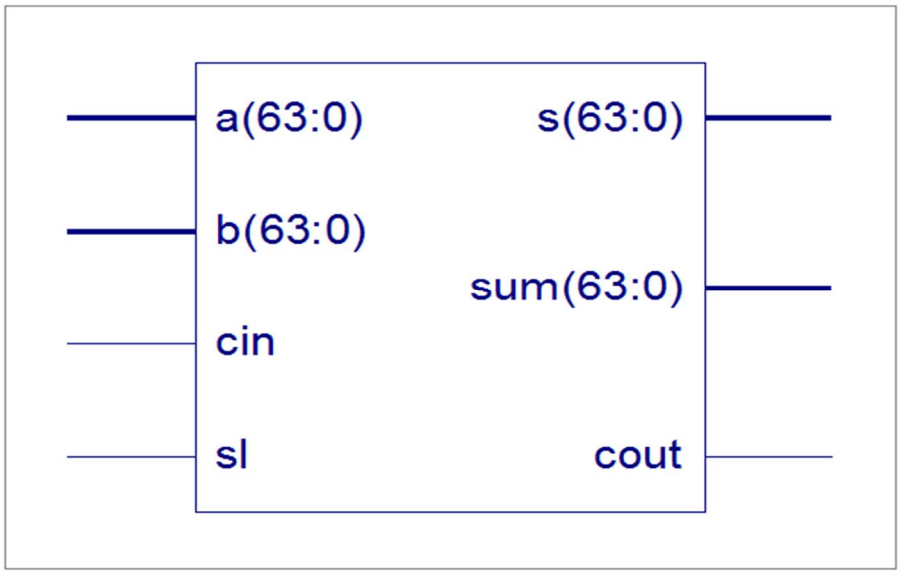

Figure 3. Hybrid Adder.

a(63:0), b(63:0), cin – are inputs of hybrid adder.
Sl- is select line of hybrid adder.
S(63:0) – is summing output of ripple carry adder.
Sum(63:0) – is summing output of carry look ahead adder.
Cout – carry output of hybrid adder.
To make hybrid adder we add two type of adder that is ripple carry adder and carry look ahead adder. According to output it will work for both type of output result.

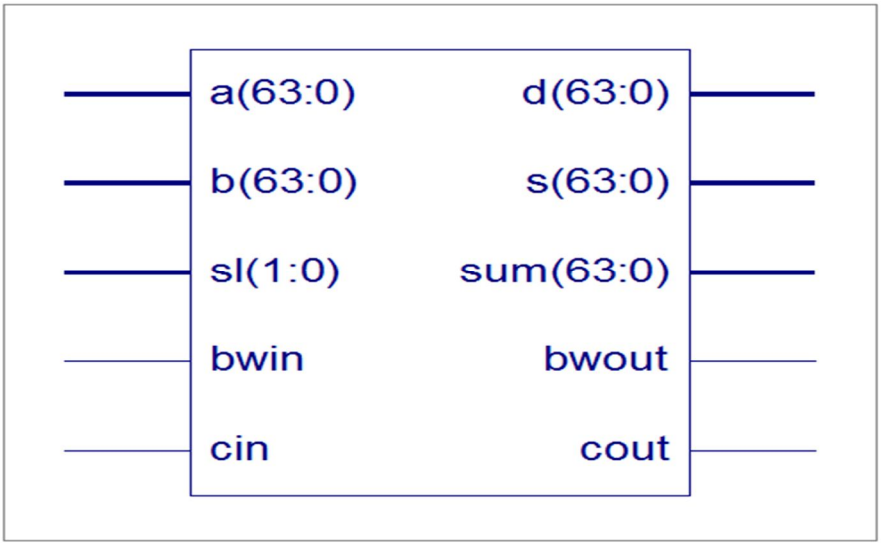

Figure 4. Hybrid Adder and Subtractor.

A hybrid adder and subtractor is made by combining to circuit of ripple carry adder, carry look ahead adder and ripple carry subtractor.
a(63:0), b(63:0), bwin, cin :-are inputs of hybrid adder and subtractor.
d(63:0) :- calculated 64 –bit difference of ripple borrow subtractor.
s(63:0), sum(63:0) :- calculated 64 bit sum of different adder.
Bwout, cout :- are for borrow output and carry output . Sl(1:0) :- select line , 1 for high value , 0 for low value.

III. RESULTS

After designing model we have to provide input that may in binary, decimal or hexadecimal. Here we providing 64 bit inputs and inputs are in decimal number. As we can see in figure of generated waveform. As we know every model do the same process of adding and subtraction but the diffence will only depends on inputs.

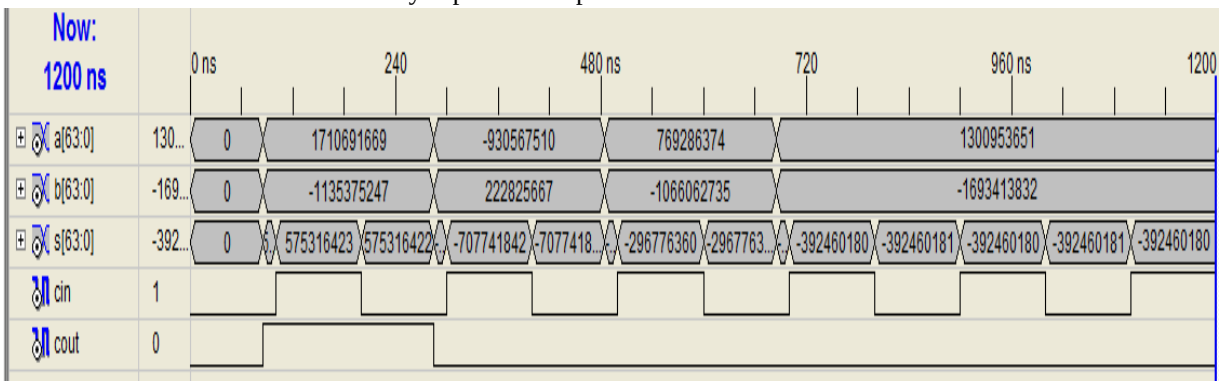

Figure 5. Ripple Carry Adder Waveform

In figure-5 a[63.0], b[63.0], and cin are the inputs of ripple carry adder and s[63.0], and cout are outputs of the ripple carry adder. As shown in diagram.

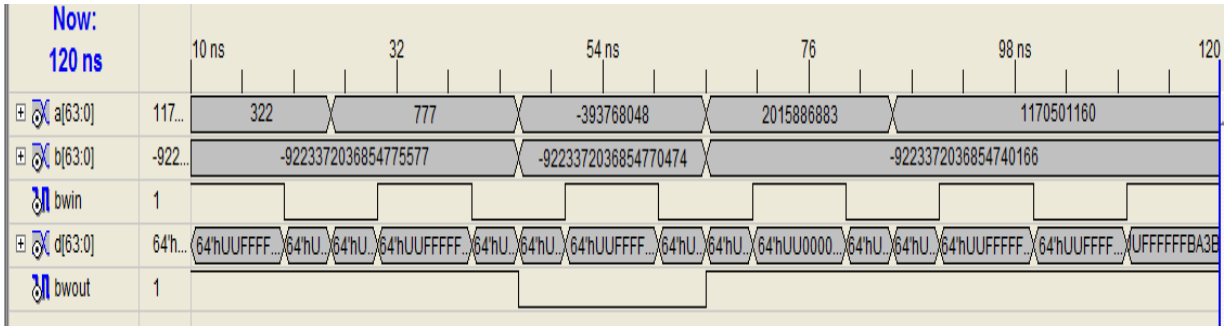

Figure 6. Ripple Borrow Subtractor Waveform.

In figure-6 a[63.0], b[63.0], and bwin are the inputs of ripple carry adder and d[63.0], and bwout are outputs of the ripple carry adder. As shown in diagram.

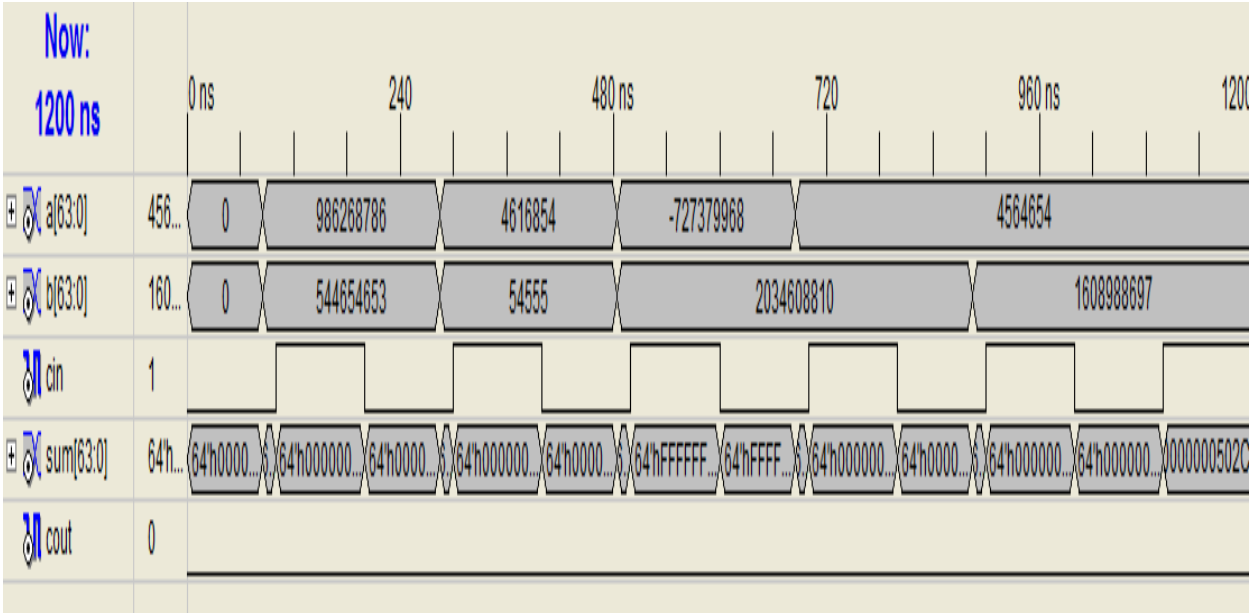

Figure 7. Carry Look ahead Adder Waveform.

In figure-7, a[63.0], b[63.0], and cin are the inputs of ripple carry adder and s[63.0], and cout are outputs of the ripple carry adder. As shown in diagram.

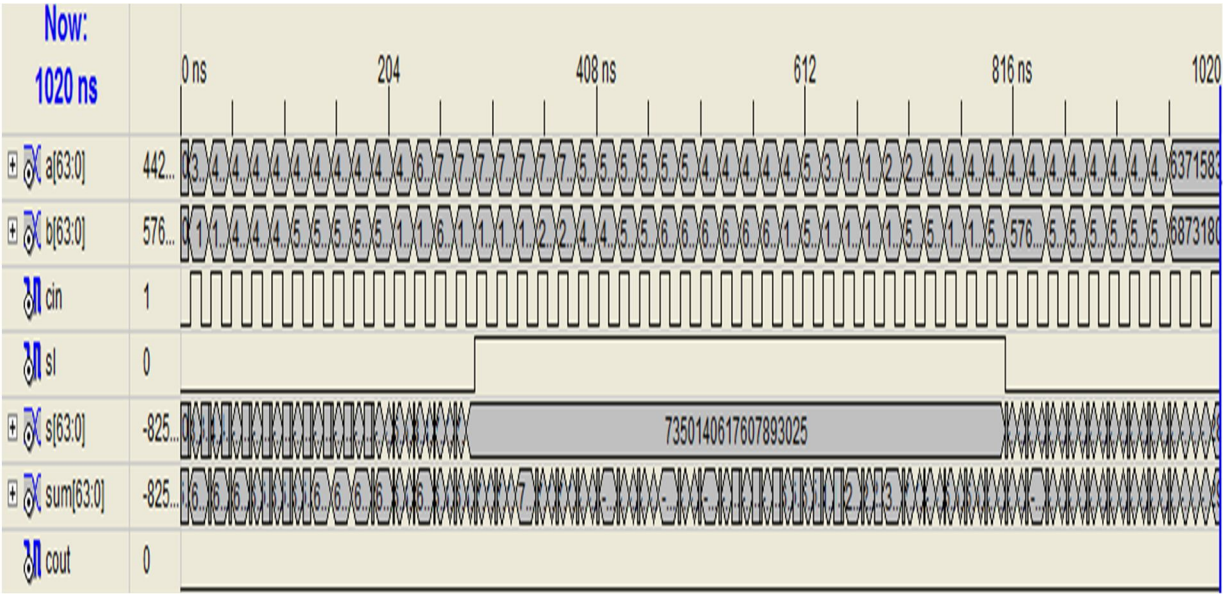

Figure 8. Hybrid Adder Waveform.

In figure-8, a[63.0], b[63.0], and cin are the inputs of ripple carry adder and s[63.0],sum[63.0] and cout are outputs of the ripple carry adder.and sl is select line. As shown in diagram.

IV. DESIGN SUMMARY

In summary we are listing different parameter of models. Like delay report of different model and no. of slices, no. of bonded IOBs, no of input/output LUTs. As shown below.

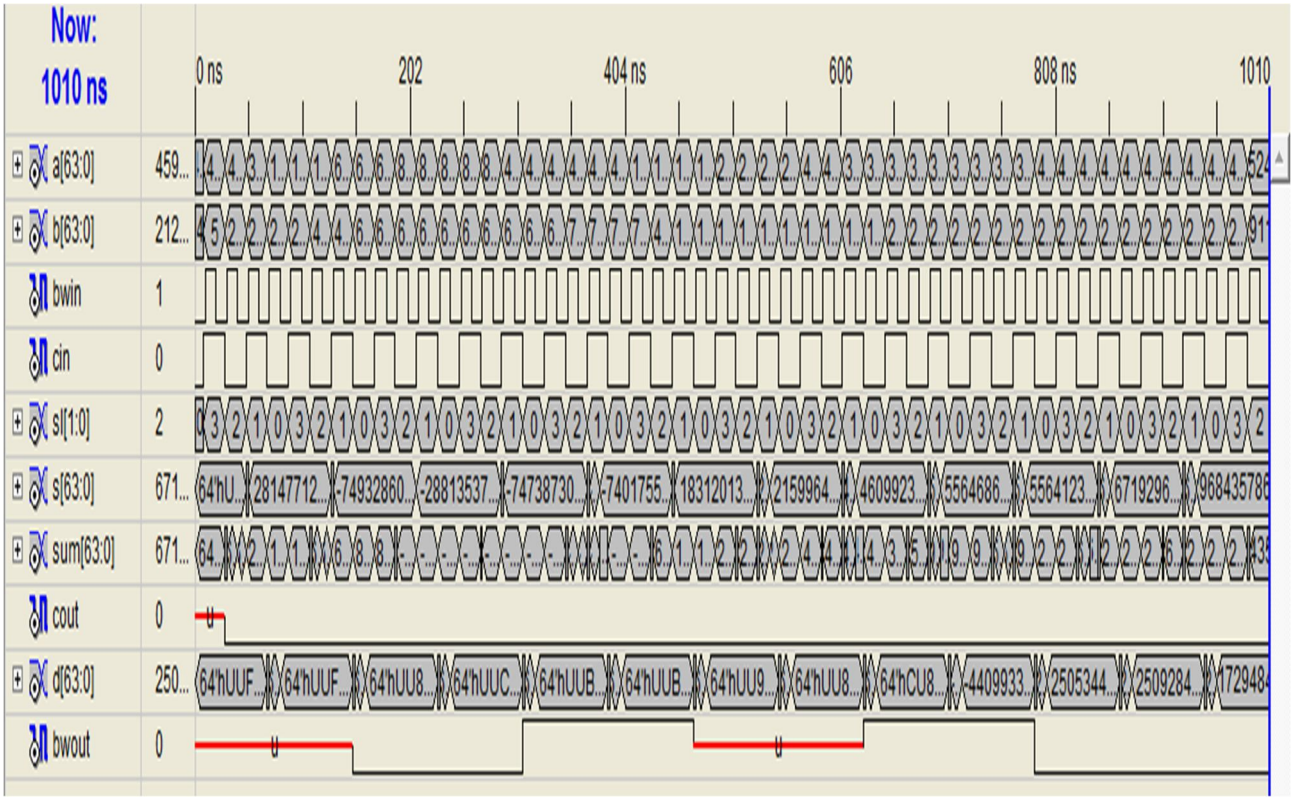

Figure 9. Hybrid Adder and Subtractor Waveform.

in hybrid model we just apply two input signal value that may be binary number like '0', '1' if signal input is '0' it means that is in off state. If it is '1' then it is in on state. Means if signal for adder is '1' and for subtractor is '0' then model will work as a adder circuit. But we have to provide input only one time. So this model will work for both operation at same time for same inputs.

V. COMPARISON OF VARIOUS PARAMETERS :-

Table 1. Comparison of various parameters of different adders.

Parameters	CLA	RCA	RBS	Hybrid adder	Hybrid of Adder and Subtractor
No of slices	74	74	74	183	249
No. of 4 i/p LUTs	129	129	129	334	449
No. of bonded IOBs	194	194	194	259	326
Delay (ns)	107.142	107.142	99.92	146.77	9.22

These are the parameters of different adder. Here five types of adders are listed as shown in table. Where delay is measured in (ns) nano second.

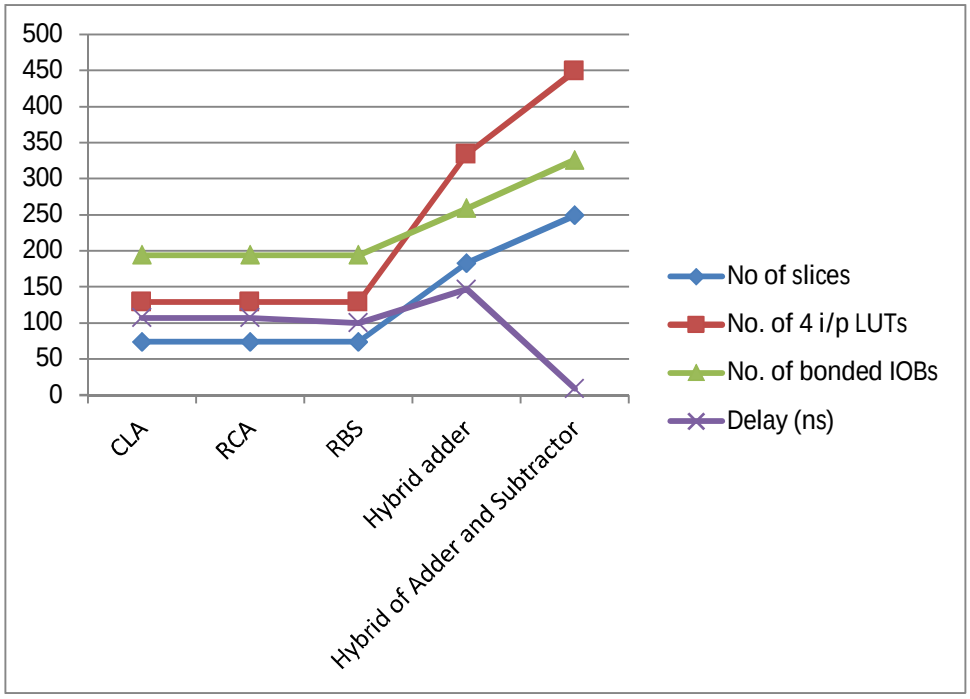

Figure 10. Comparisons of Different Parameters of Different Modelled Designs.

Table 2. Delay based performance comparison of proposed design and existing designs.

Parameter	16 bit Adder	32 bit Adder	64 bit Adder	Hybrid Adder and Subtractor
Delay	14.67 ns	18.83 ns	23.71 ns	9.22 ns

Many models are designed ever before on the base of which students improve their size and performance. There is a great progress in history time by time. Like first of all 2 bit Adder comes then 4 bit, then 8 bit. And this size increasing with time .every time there is a improvement in the performance. As table showing a increase in performance by reducing delay.

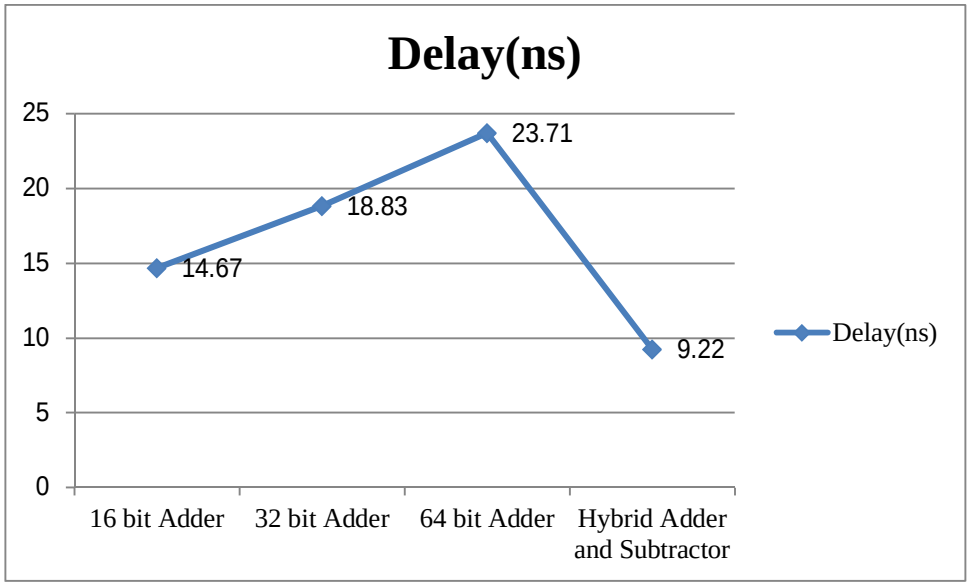

Figure 11. Comparison of different Adders Delay.

VI. CONCLUSION

After study all the parameters of different modeled adder and their simulation result. By studying different graphs value and comparing them with existing graphs value. It is concluded that delay and size of model can be reduced to such a level. The simulated design has less delay than ever before but size, area and input output results not much changed. In last, It is concluded that hybrid model of adder and subtractor is best with reduced delay performance. As we increase the number of inputs and area, Size of model will be automatically increased. Delay is the time taken to provide result by any circuit. So if simulation results decrease in the delay, performance of model will be automatically increased.

In future we may decrease the delay much further than this and can get an efficient model of adder. There is a large area of research in reducing the size of model and area of model.

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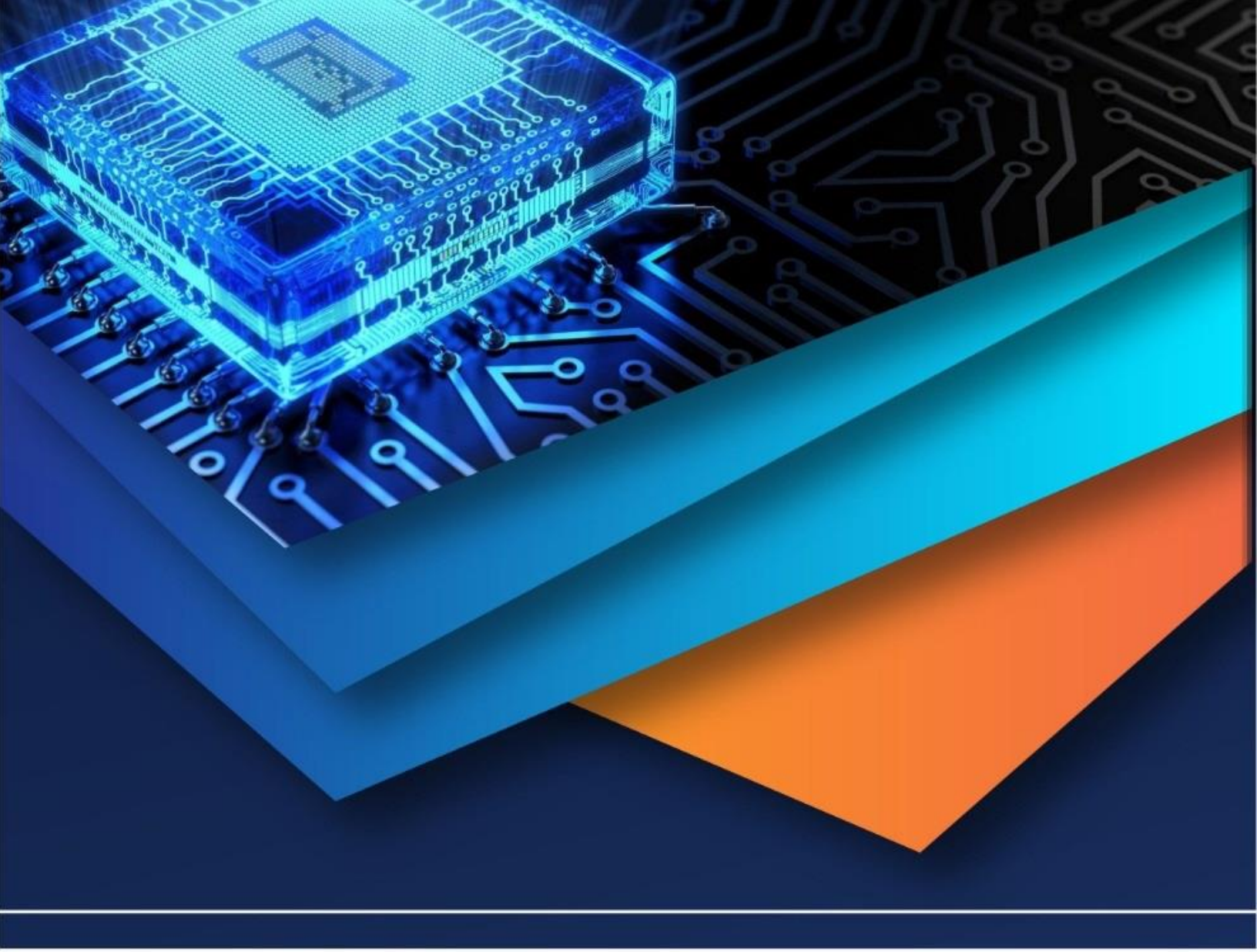

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