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Analysis of Low Power High Speed Carry Skip Adder: A Review

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Abstract: ***The Carry Skip Adder (CSKA) is identified by a better efficiency in the trade off between operating speed and power dissipation, as it has a very low power-delay product, near to that of a carry-look ahead adder (CLA). A CSKA consists of blocks of full adder combined together, whose schematic (i.e., combination of full adders per block) mainly affects the overall operating speed of carry skip adder. For skip logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates.***
Keywords: Carry Skip adder, mux, skip logic.

I. INTRODUCTION

The ever-increasing demand for mobile electronic devices requires the use of power-efficient VLSI circuits. Computations in these devices need to be performed using low-power, area-efficient circuits operating at greater speed. Addition is the most basic arithmetic operation; and adder is the most fundamental arithmetic component of the processor. Adders are key building block in arithmetic and logic units (ALUs). There are many works on the subject of optimizing the speed and power of these units, which have been reported in [1-5]. It is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage and addition to the knob of the supply voltage, one may choose between different adder structures/families for optimizing power and speed. There are many adder families with different delays, power consumptions, and area usages. Examples include ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs). The descriptions of each of these adder architectures along with their characteristics may be found in [6]. The RCA has the simplest structure with the smallest area and power consumption but with the worst critical path delay. In the CSLA, the speed, power consumption, and area usages are considerably larger than those of the RCA. The PPAs, which are also called carry look-ahead adders, exploit direct parallel prefix structures to generate the carry as fast as possible. There are different types of the parallel prefix algorithms that lead to different PPA structures with different performances. As an example, the Kogge–Stone adder (KSA) [2] is one of the fastest structures but results in large power consumption and area usage. It should be noted that the structure complexities of PPAs are more than those of other adder schemes. The CSKA, which is an efficient adder in terms of power consumption and area usage. It is designed to speed up the addition operation by adding a propagation of carry bit around a portion of entire adder [7]. The critical path delay of the CSKA is much smaller than the one in the RCA, whereas its area and power consumption are similar to those of the RCA. Carry-skip adder has the advantage of short delay and high computing efficiency so causes wide attention. In addition, due to the small number of transistors, the CSKA benefits from relatively short wiring lengths as well as a regular and simple layout [7-9]. In this paper, we have implemented a complementary multiplexer as a skip logic using TANNER EDA tool for high speed and low power application of a 4 bit carry skip adder. The growing market of portable (e.g., cellular phones, gaming consoles, etc.), batterypowered electronic systems demands microelectronic circuits design with ultralow power dissipation. As the integration, size, and complexity of the chips continue to increase, the difficulty in providing adequate cooling might either add significant cost or limit the functionality of the computing systems which make use of those integrated circuits.

II. LITERATURE REVIEW

A static CMOS CSKA structure called CI-CSKA was proposed, which exhibits a higher speed and lower energy consumption compared with those of the conventional one. The speed enhancement was achieved by modifying the structure through the

concatenation and incremenation techniques. In addition, AOI and OAI compound gates were exploited for the carry skip logics. [1]

The critical path delay of the CSKA is much smaller than the one in the RCA, whereas its area and power consumption are similar to those of the RCA. In addition, the power-delay product (PDP) of the CSKA is smaller than those of the CSLA and PPA structures[1].

The paper [2] entitled, the performance parameters of delay, average power, PDP and EDP are compared at different technology node. Worst case delay can be reduced with different techniques which has been proposed for full adders, it provides an optimization techniques that is Static CMOS technology and Pass Transistor logic used only for the case of constant block size to improve the speed performance.

In Static CMOS logic, each logic stage is controlled by input signal which contain pull up network and pull down network. In the Pass Transistor logic (PTL), it reduces the number of transistor which are used to design all the type of logic gates[2].

The comparison of average power of CMOS and PTL techniques of carry skip adder with supply voltage variation, it is observed that CMOS techniques consumes more power than the PTL technique.

The paper [3] entitled, A novel incrementer circuit in the interim stages of the CSA by calculating carry out (C0) of the block in parallel along with third bit by using a parallel chain of AND gates, whereas a series pattern of carry propagation is used in RCA structure, which reduces the delay of incrementing in CSA when compared with the conventional RCA is employed. CSA reduced propagation delay characteristics.

The paper [4] entitled, The basic idea of this work is to uses simple and area efficient gate level modification to reduce area and power of CSLA. In that the Binary to Excess-1 Converter (BEC) is used instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption. The advantages of BEC logic comes from the lesser number of logic gates than n-bit full adder structure. An n+1-bit BEC is required to replace the n-bit RCA.

The paper [5] entitled, an efficient Carry select adder by sharing the Common Boolean logic (CBL) term is used. In this paper, an efficient method used that replaces the BEC using Common Boolean Logic. After a logic simplification, only one OR gate and one inverter gate for carry and summation operation has been needed. Through the multiplexer, the correct output according to the logic states of the carry in signal has been selected.

The paper [6] entitled, the carry select (CS) operation is schedule before the calculation of final-sum, which is different from the conventional approach. Bit patterns of two anticipating carry words (corresponding to cin = 0 and 1) and fixed cin bits are used for logic optimization of CS and generation units. An efficient CSLA design is obtained using optimized logic units. Due to small carry output delay, the proposed CSLA design is good candidate for the square-root (SQRT) CSLA. [6]

III. ADDER ARCHITECTURES

Multiple-bit addition can be as simple as connecting several full adders in series or it can be more complex. How the full adders are connected or the technique that is used for adding multiple bits defines the adder architecture. Architecture is the most influential property on the computation time of an added. This property can limit the overall performance. In general the computation time is proportional to the number of bits implemented in the adder. Many different adder architectures have been proposed to reduce or eliminate this proportional dependence on the number of bits. Several adder architectures are reviewed in the following sections.

A. Ripple Carry Adder (RCA)

An n-bit ripple carry adder consists of n full adders with the carry signal that ripples from one full-adder stage to the next, from LSB to MSB. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a Cin which is the Cout of the previous adder. Addition of k-bit numbers can be completed in k clock cycles[3]. A 4-bit ripple carry adder structures is shown in figure 1.

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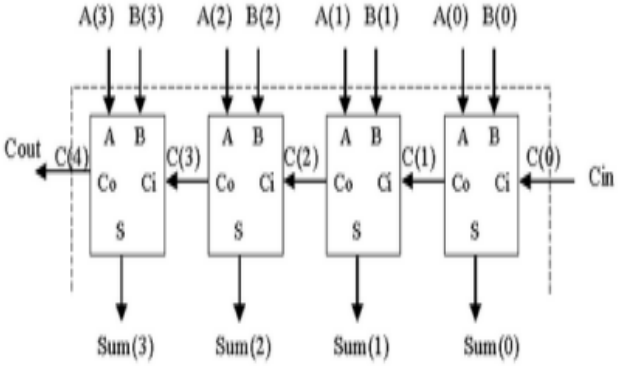

Fig 1: Structure of 4-Bit Ripple Carry Adder

The ripple-carry adder has many advantages like low power consumption, low area and simple layout. The drawback of the ripple carry adder is its slow speed because each full adder must wait for the carry bit to be calculated from the previous full adder.

B. Carry Look-Ahead Adder (Cla)

To reduce the computation time, faster ways to add two binary numbers by using carry look ahead adders. It is done by creating two signals (P and G) for each bit position, based on if a carry is propagated through from a less significant bit position (at least one input is a '1'), a carry is generated in that bit position (both inputs are '1'), or if a carry is killed in that bit position (both inputs are '0'). In most cases, P is simply the sum output of a half-adder and G is the carry output of the same adder. After P and G are generated the carries for every bit position are created.

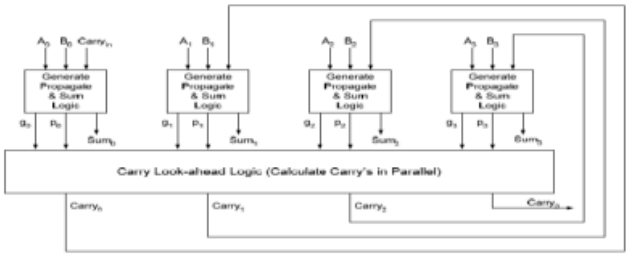

Fig 2: Structure of 4-Bit Carry Look-ahead Adder

These block based adders include the carry bypass adder which will determine P and G values for each block rather than each bit, and the carry select adder which pre-generates sum and carry values for either possible carry input to the block. On the other hand adder designs include the conditional sum adder, carry skip adder, and carry complete adder. In carry look-ahead architecture instead of rippling the carry through all stages (bits) of the adder, it calculates all carrys in parallel based on equation (1).

$Ci = gi + piCi-1$ (1)

In equation (1) the gi and pi terms are defined as carry generate and carry propagate for the ith bit. If carry generate is true then a carry is generated at the Ith bit. If carry propagate is true then the carry-in to the Ith bit is propagated to the carry-in of i+1 bit. They are defined by equations (2) and (3) where Ai and Bi are the binary inputs being added.

$gi = AiBi$ (2)

$pi = Ai + B$ (3)

C. Carry Bypass Adder (CBA)

The carry-bypass or carry-skip adder is much like the RCA only it has a carry bypass path. This architecture divides the bits of the adder into an even number of stages M. Each stage M has a carry bypass path that forwards the carry-in of the Mi stage to the first carry-in of the Mi+1 stage. If the binary inputs are such that the carry would normally ripple (or propagate) from the input of the

Mi stage to the input of the Mi+1 stage, then the carry takes the bypass path. A multiplexer is inserted between each stage M of the adder to choose from the normal ripple path or the bypass path (see Figure 3).

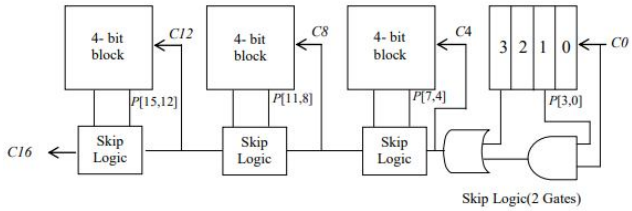

Fig 3: Structure of 4-Bit Carry Bypass Adder

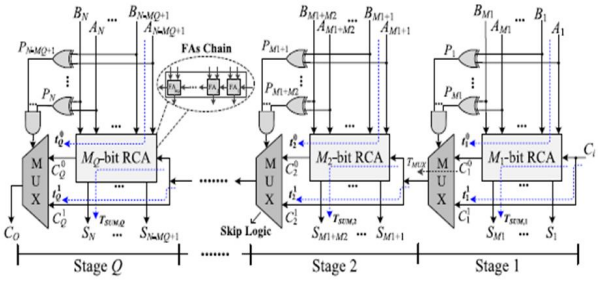

Fig 4: conventional structure of CSKA

The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1 multiplexers, which can be placed into one or more level structures. The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder [1].

A CSKA performs fast addition since adders are split in blocks of N bits. It greatly reduces the delay of the adder through its critical path, since the carry bit for each block can be bypassed (skip) over the blocks. It consists of simple RCA with a AND-OR skip logic as shown in Figure 3. It generates carry-out from each block depending on MSB full adder carry-out, LSB full adder carry-in and sum bit of each full adder. If the AND-OR skip logic output is 1, the current block will be bypassed and next block will start computation [1].

IV. CONCLUSION

This paper has reviewed the mainly latest research trends on adder and carry skip adder (CSKA).This paper analyzed the speed enhancement, achieved by applying concatenation and incrimination schemes to improve the efficiency of the conventional CSKA structure. In this paper many different methods are studied for adder,a higher speed and lower energy consumption compared with those of the conventional one. The speed enhancement was achieved by modifying the structure through the concatenation and incrimination techniques. In addition, AOI and OAI compound gates were developed for the carry skip logics.

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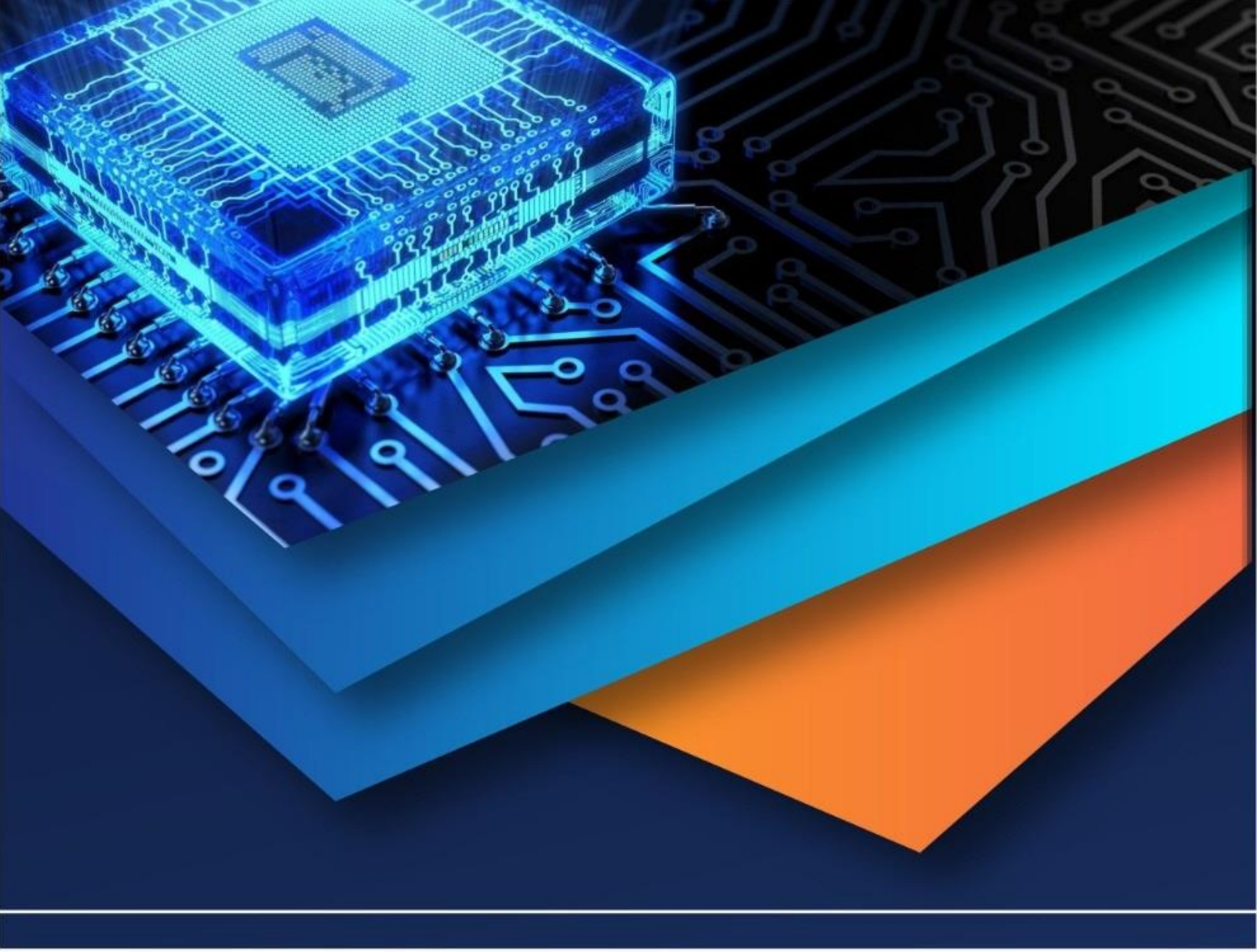

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