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FPGA Implementation of Forest Fire Detection System using Colour Models

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Abstract: Uncontrolled fire occurring in nature causes huge threats. If there is a fire in the forest, it takes lot of time for the fire fighting crews to gain control over the situation resulting in huge loss to the life of animals and various creatures. So, It becomes important to monitor and detect forest fire. There are many techniques adopted for detecting forest fire caused due to the interference of humans with nature or due to natural phenomenon's like lightning, here we are using the Colour models to detect the fire. Implementation of the system is through FPGA, a reconfigurable hardware.
Keywords: ASIC, Cb, Cr, CCD, FPGA, ICON, ILA, MATLAB, PCA, ROM, RTL, XPE.

I. INTRODUCTION

Taking India's population into consideration, the forest wealth we are having is not encouraging. So it is important that we conserve the resources that we have. According to the most recent condition of forest report of the Forest Survey of India the genuine forest area of India is 19.27% of the geographic region, relating to 63.3 million ha. Just 38 million ha of forest are all around loaded (crown thickness above 40%). This asset needs to take care of the demand of a population of 950 million individuals and around 450 million cows. Thus any nation needs to address the issues of 16% of the world's population from 1% of the world forest resources. The same forest has additionally to cook for the 19% of the world dairy cattle populace. The forest of the nation are thus, need to protect. Woods flames are a noteworthy reason for corruption of India's backwoods. Forest fires are a more dangerous in degradation of India's forests. It is evaluated that, forest fires every year ranges from 33% in a few states to more than 90% in other.

II. DESIGN AND IMPLEMENTATION OF FOREST FIRE DETECTION SYSTEM

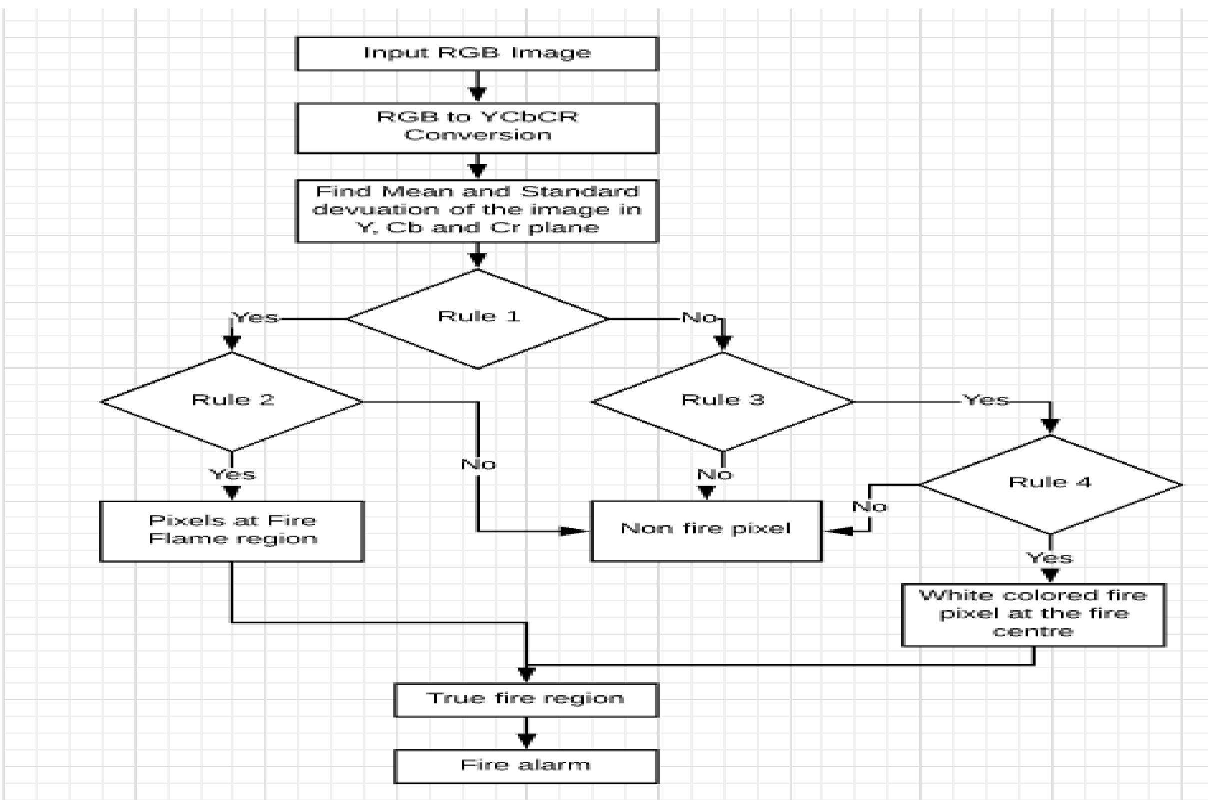

Figure 1: Flow chart for Forest Fire Detection System

A. Forest Fire Detection using YCbCr Colour Model

The best suited algorithm for forest fire detection is Image Processing Based Forest Fire Detection using YCbCr Colour Model. In software modelling of the selected forest fire algorithm has been done as shown in the Figure1.

B. RGB to YcbCr Color Conversion

In RGB colour space contains only intensity information and so it is required to separate intensity and chrominance. This information can be extracted using colour space conversion to convert from RGB to YCbCr colour space and chrominance can be used in modelling colour of the fire rather than modelling its intensity and it gives a more chance of representation for fire pixels. So there is need for transforming RGB colour space into one of the colour space.

C. Applying the Rules Defined

The rules defined in the flow chart are discussed in this section. There are four rules and in these, first 2 rules defines the fire segmentation region and other 2 rules are used for segmentation of centre fire pixels which are high temperature pixels. After applying all these, rule 2 and rule 4 are added to get true fire region.

1) The rule 1 states that the value of Y channel should be greater than Cb channel so, the intensity of Y channel should be greater than intensity of Cb channel, therefore rule 1 can be found as

$$R1(x,y) = \begin{cases} I(x,y), & if\ Y(x,y) > Cb(x,y) \\ 0, & otherwise \end{cases}$$

2) The rule 2 justifies about brightest region, here the chrominance red is one which counts in chrominant part of fire image. In fire region, the value of Y (luminant) factor at each special location is greater than mean value of the Y (Y mean) and the value of Cr channel at each special location is greater than mean value of the Cr (Cr mean)

$$R2(x,y) = \begin{cases} R1(x,y), & if\ Y(x,y) > Y_{mean}\ , Cr(x,y) > Cr_{mean} \\ 0, & otherwise \end{cases}$$

3) As the temperature increases, the center of fire region become white and in this information, chrominance blue is more than chrominance red. From several test of images, the Prem Emmy .C and Vinsely S.S detected that at the fire center region, the chrominance blue (Cb) channel is greater than luminance (Y) and chrominance red (Cr) and the rule 3 formed is as follows

$$R3(x,y) = \begin{cases} I(x,y), & if\ Cb(x,y) \geq Y(x,y) > Cr(x,y) \\ 0, & otherwise \end{cases}$$

4) This rule is formulated using texture of fire like region and non-fire like region. The texture of fire region is defined using mean, standard deviation and here the standard deviation of Cr plane is used and constant

$$R4(x,y) = \begin{cases} R3(x,y), & if\ Cr(x,y) < \tau \times Cr_{std} \\ 0, & otherwise \end{cases}$$

III. SOFTWARE IMPLEMENTATION:

After the theoretical explanation of concepts, this section deals with implementation of sub-blocks and their incorporation in software modelling.

1) *Image Acquisition:* In any computer based vision system, the first step is to read or acquire an image. Once the image is obtained, it is processed using various methods depending on the application. The images are taken from the internet database in the jpg/ png format, size of “mxn”. Where m is the number of rows and n is number of columns

2) *Colour Conversion RGB to YCbCr:* Ycbcr colour conversion which has information of luminance and chrominance hence these colour components are used in algorithm.

3) *Separation of Y, Cb, and Cr Channel:* The channels are isolated from ycbcr colour space and stored in the register separately and later mean, standard deviation is calculated and which is helpful in providing the conditions.

4) *Mean and standard deviation of y, cb, and cr channel:* Sub block for YCbCr are created and stored in registers, Mean of Y, Cb and Cr channels is calculated and standard deviation of Cr channel is calculated

5) *Algorithm implementation:* In this section, algorithm implementation has been done by using the 4 rules as explained above. Rule2 and Rule4 are added to detect the true fire region.

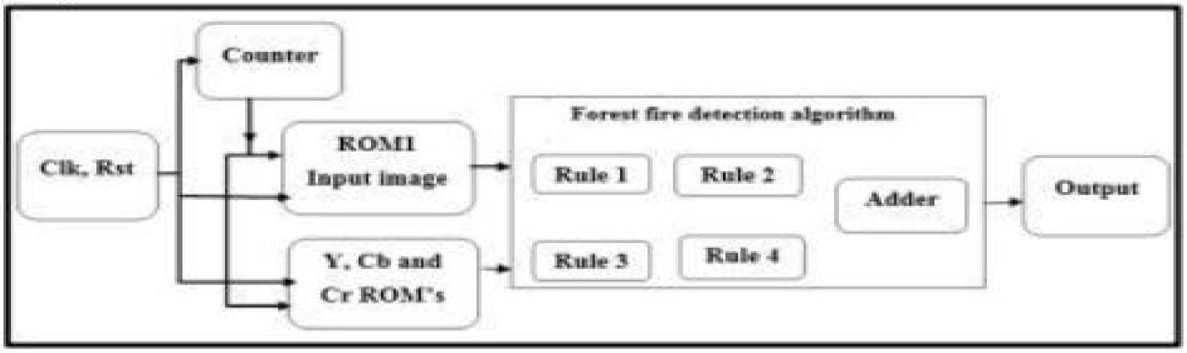

Figure 2: Block Diagram

IV. HARDWARE IMPLEMENTATION OF FOREST FIRE DETECTION

This section deals with the hardware implementation of the forest fire detection algorithm on FPGA. The developed code is compiled with Xilinx ISE 14.4 by choosing Digilent Nexys4 development board consisting Spartan 6 family, CSG324 package with speed grade -1. RTL code is developed for forest fire detection and each sub-block is simulated. The design is synthesized and implemented on FPGA. Forest fire detection algorithm is developed using Verilog HDL. The functionality of RTL code developed is verified using fire and non-fire images. Analysis of timing and power is observed. Validation of Verilog HDL is verified using Chip Scope pro. In the following section steps are carried out for hardware implementation

For image processing on FPGA, the generations of COE files are important because the image cannot directly read to FPGA. So the text files are generated for input image, Y, Cb and Cr channels in COE format. Figure 2 shows the basic building blocks of forest fire detection system. The design of forest fire detection system has been developed in MATLAB and Verilog HDL. The results for different types of images containing fire and non-fire region have been carried. Forest fire region for different still images has been detected. The implementation on FPGA has been performed and works satisfactorily. The validation and debugging of system is performed using Chip Scope pro.

V. RESULTS

The validation and functional verification of developed forest fire detection system. Matlab results are observed and Verilog HDL developed is verified for its functionality. Hardware implementation is done on Nexys4 board and its validation and debugging is done in Chip Scope-pro. Then MATLAB, Verilog HDL, Chip Scope pro outputs are compared and discussed.

The MATLAB code is developed and evaluated with different image containing fire and non-fire regions. The Figure 3 shows the input image and its colour conversion and fire detected output.

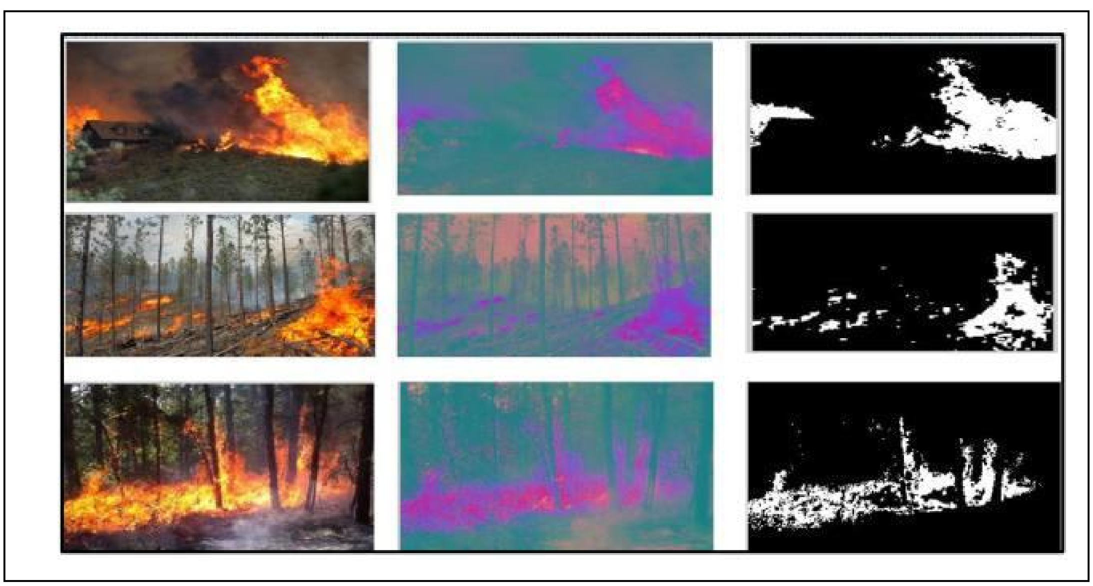

Figure 3: MATLAB Simulation Results

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Figure 4: MATLAB Simulation results for no fire images

Figure 4 depicts the results of forest fire detection system for non-fire region and it can be observed that developed algorithm recognises no fire region for the images. Verilog output is validated by the RTL code developed is synthesized. By developing the test bench, simulation is performed.

Figure 5: Simulation of Forest fire detection

Figure 5 shows the simulation results of forest fire detection system. When clock is high and reset is low, at address location 7290, fire detected has pixel intensity value of 119 with delay of 2 clock pulses. The test bench is generated for forest fire detection.

1) *Synthesis of Proposed Architecture* In the synthesis report, device utilization summary is generated. This information gives brief description of available total number of resources and use of resources in numbers and percentage. The table 5.1 shows the resource utilization by the developed design.

Logic Resources	Available	Used	Utilization
Number of Slice Registers	126800	59	1%
Number of slice LUTs	63400	132	1%
Number of fully LUT FF-pairs	164	49	28%
Number of bounded IOBs	210	81	38%

2) *Timing Analysis* The minimum period for the developed design is 5.808 ns and maximum frequency operation is 172.176 MHz
3) *Power Analysis* In present trend of low power applicant such as handheld devices, battery operated devices, etc., demands for architecture with ultra-low power requirement for long battery life. Proposed architecture is subjected to power analysis using the Xilinx Power Estimator (XPE) which is an integrated tool from Xilinx ISE package.

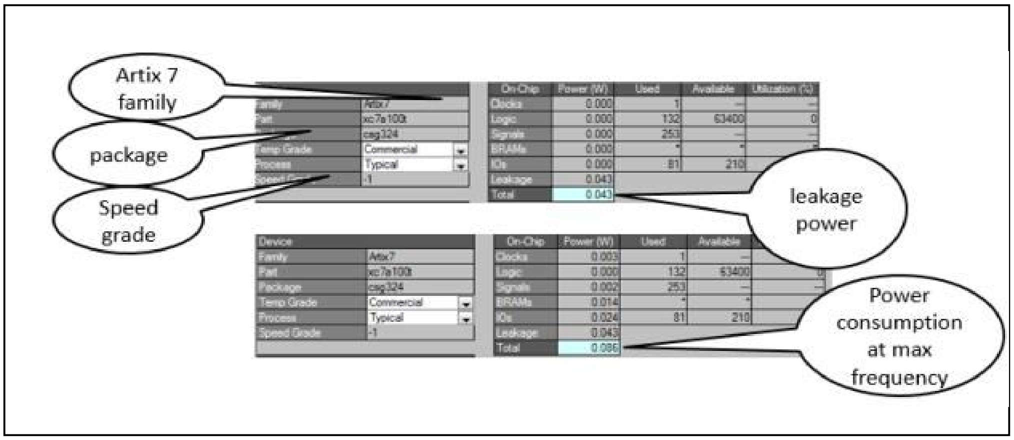

Figure 6: Leakage and Maximum Power Consumption

4) *Comparison of Results* In this section, the comparison of results of Software and hardware implementation results has been discussed. The output of prototype is displayed on monitor using VGA port.

Figure 7: Comparison of outputs detected by MATLAB and Verilog.

Figure 7 shows the output results of reconstructed image in software and Hardware implementation. Another comparison is Verilog simulation and Chip Scope pro simulation. Using the memory address location, the pixel value present in that location can be compared between Verilog output and Chip Scope pro output.
The results for the developed forest fire detection system in software and hardware implementation had discussed and functionality of both implementation has been verified and working successfully for different images.

VI. CONCLUSION

Forest fire is most commonly found threat in the forests. It occurs due to lightening, rubbing of dry trees, waste thrown by human who contains flammable things. Stern economic loss also occurs along with damage to forest. Even though forest fire monitoring or detection system exists which has disadvantages like high cost and low performance. To overcome these disadvantages new techniques have been identified to solve the problems like accuracy, low speed and resolution. The forest fire detection algorithms based on image fire detection and due to less complication and high effective ness rule based colour model is adopted. YCbCr is used to separate luminance component from chrominance compared to other colour spaces like RGB. Here two rules are used for segmenting the fire region and other two rules are used for segmenting the high temperature fire centre region. Conditions are applied for different set of images containing fire region and non-fire region.

Future Scope Since this work carried out is limited to still images, it can further extend it to real time image processing and regarding implementation, it can take it for ASIC implementation. The algorithm can be improved in terms of accuracy, using CIE L*a*b colour space by adopting K-NN classifier for fire pixels. (Burak Celen et.al 2012). The resolution was set to 100*100 pixels can be increased to get high resolution images. Processing uses colour spaces. In this thesis YCbCr colour model is used in forest.

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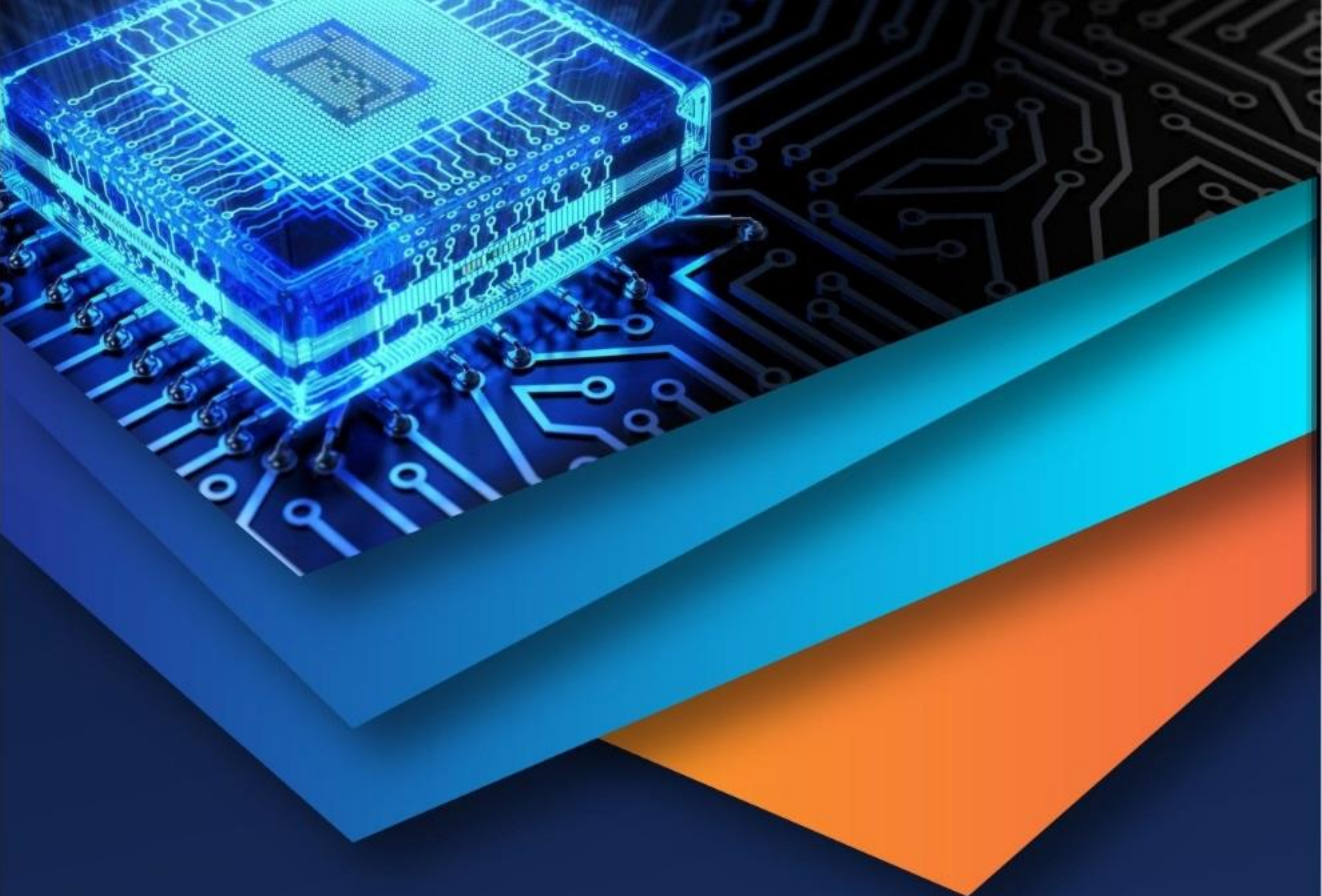

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