iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 6 **Issue:** V **Month of publication:** May 2018

DOI: http://doi.org/10.22214/ijraset.2018.5056

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue V, May 2018- Available at www.ijraset.com

High Performance Advanced P-OCI Crossbar with PaCC Codec

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Abstract: ***On-chip communications profoundly impact the overall area, performance and power consumption of modern System on Chips. Developing an efficient high performance on chip interconnects has been of paramount importance for the parallel and high performance computing technologies. Network on Chips are the most scalable interconnection paradigm that is capable of addressing various application needs and meet different performance requirements. Overloaded CDMA is a well known medium access technique deployed in wireless communication to increase the interconnect capacity. The Walsh spreading codes enables adding more number of non orthogonal spreading codes to increase the interconnect capacity. In this paper, a hybrid encoder used in the crossbar can develop both the orthogonal and nonorthogonal spreading. The orthogonal and overloaded decoders are used to decode the data. The data spreading and despreading are parallelized in the P – OCI crossbar. A parallel compare and compress (PaCC) architecture is used to reduce the excess area need to store the message data. Codec is the key component that is used in the PaCC architecture which effectively balances the area and performance. The parallel Run Length Encoding scheme observes k bits in parallel. If they all are 0 or 1, all the k bits are bypassed in one clock cycle. The value of k affects the compression speed by impacting the bypass opportunity. This helps to improve the overall area, power and performance along with increase in bandwidth. The design is simulated using Xilinx ISE Design Suite 14.5. The results show that the PaCC Codec based P-OCI attains greater bus capacity, less power consumption and efficient in area when compared with the normal P-OCI architectures.***

Keywords: System on Chip, Overloaded CDMA, on-chip interconnect, Crossbar, Network on Chip, Codec, Code Division Multiple Access.

I. INTRODUCTION

System on Chip integrates several intellectual property (IP) blocks into a single chip. All of these IPs need to communicate in the Gbps range. So the on-chip communication requirements for these systems are very demanding. The IP blocks must comprise an interconnection architecture and several interfaces to connect the peripheral devices. The interconnection architecture includes many physical interfaces and communication mechanisms. On-chip data transfer affects the area, performance and the power utilization of the System on Chips. Developing an suitable high performance on-chip interconnect architecture has been of supreme significance while considering the high speed computing technologies. Network on Chips provide a way to prevail over the restrictions inherent in regular bus based interconnection schemes and offers several benefits like high throughput, lower energy dissipation, flexible scalability and design reusability.

In the case of Network on Chips , data from the routers are considered as several packets and on - chip processing elements are examined as network nodes which are interconnected via routers and switches. A crossbar is one of the most important component of the NoC physical layer. It is a shared communication medium which helps in the exchange of packets. Time Division Multiple Access (TDMA), Space Division Multiple Access (SDMA) and Code Division Multiple Access (CDMA) are the foremost resource allocating techniques utilized by the existing network on- chip crossbars. In the case of CDMA communication each transmit – receive pairs is assigned a distinctive bipolar spreading code. In the communication channel all the data from the transmitters are added. The ordinary CDMA systems use Walsh – Hadamard codes to facilitate the sharing of medium [9]. The spreading codes that used in normal CDMA communication systems are mostly orthogonal and it allows the CDMA receiver to accurately decode the sum from the channel. Multiple Access Interference (MAI) may occur if any additional codes were added. The supreme number of users in the CDMA based communication system may limited because of the Multiple Access Interference problem. Overloaded CDMA can be used to intensify the number of users sharing the communication channel. The interconnect capacity of the on chip interconnects can be boosted with overloaded CDMA concept.

In this paper, we apply the idea of overloaded CDMA to the crossbar of Network on Chip to appreciably increase the capacity of the bus. Also, a parallel compare and compress (PaCC) architecture is used to diminish the surplus area needed to store the message data. Codec is an important component of the PaCC architecture and it effectively balances the area and performance. The Parallel Run Length Encoding scheme observes *q* bit in parallel[10].

II. LITERATURE REVIEW

The ordinary CDMA bus depend on orthogonal Walsh codes to validate the allocation of bus. Tatjana Nikolic, Mile Stojcev and Goran Djordjevic proposes a Code Division Multiple Access related bus structure in [3] for the reduction of the parallel data transfer lines to TDMA based buses. Combination of Code Division Multiple Access and Time Division Multiple Access in the CT bus communicates the data over the time domain as well as the code domain. A multilevel 2 bit Code Division Multiple Access proposed in [8] was mainly used as an input and output redesign scheme and also reduces the bus contention over Time Division Multiple Access. In [2]a comparison of based Network on Chip and a Point To Point duplex ring based Network on Chip is done. The outcome after simulation shows that the Code Division Multiple Access Network on Chips irreversible data transfer latency is equal to the best case latency of the Point To Point of the identical channel width. The irreversible data transfer latency of the Code Division Multiple Access based Network on Chip is attributed to the co-occurent allocation of the channel by the nodes of the network . In [5] , a wireless Code Division Multiple Access Network on Chip system was indicated to have notably lower energy consumption and larger bandwidth than a Time Division Multiple Access Network on Chip. Most of the associated work with the Code Division Multiple Access interconnect makes the enhancements in the architecture and the topology. Also the performance of the normal DS – Code Division Multiple Access communication scheme is evaluated. In this paper, we find a solution to reduce the area and power consumption of the P-OCI crossbar which increases the bus capacity by applying overloaded Code Division Multiple Access to the existing on chip Code Division Multiple Access bus.

III.OVERVIEW OF CONVENTIONAL CDMA CROSSBAR

Fig. 1 demonstrates the block diagram of the architecture of the normal CDMA NoC router. The classical CDMA crossbar as shown in the Fig. 2 consists of three sections. They are encoder section, channel section, and decoder section. In the encoder part, the spreading code generator module (Walsh spreading code) generates binary orthogonal code which has a chip length of C. After the XOR operation between the data and the spreading code the output is sent to the communication channel in a serial manner. It indicates that spreading of each single bit takes place in a time span of C clock cycles. Maximum number of IP core Transmit-Receive pairs that shares the channel bus is equal to B i.e., B > C. For the normal CDMA bus, which uses the Walsh spreading codes B = C.

The Serial data streams from every transmitting IP cores that shares the CDMA bus system are added together. Then the resultant sum that obtained is denoted in the binary form and it is sent to the decoding unit which is connected to the receiving IP cores. It cross correlates the serialized data (sum) from the channel with the spreading code which is assigned for every transmit- receive pair. The data despreading mainly require two operations. They are sum multiplication by and the accumulation. The data from the channel (bus) is passed to zero or one accumulator on the basis of the chip value. If the chip value is zero, then it is passed to the zero accumulator and if the value is one , then it is passed to one accumulator [2].

At the beginning of each decoding cycle the accumulators is reset to zero. Consequently, each of the accumulators adds half of the chip length of different inputs during the decoding cycle. This is possible due to the balancing nature of spreading codes. During the completion of each decoding cycle, if the content of the zero accumulator is greater than the content of one accumulator, the data bit transmitted is one otherwise it is zero.

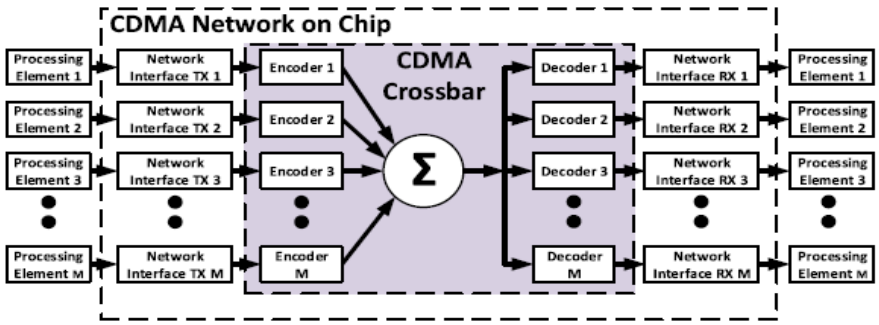

Fig.1. Architectural diagram of normal CDMA based Network on Chip Router.

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887
Volume 6 Issue V, May 2018- Available at www.ijraset.com

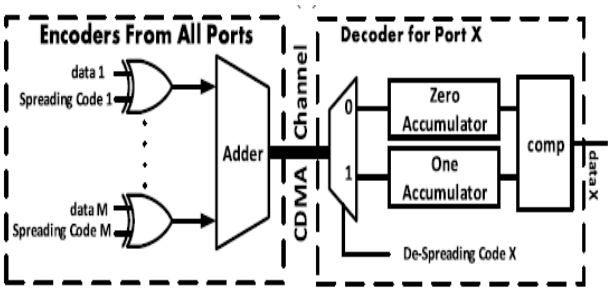

Fig.2. CDMA Crossbar.

IV. PRLE BASED P-OCI CROSSBAR

The main objective of this on-chip interconnect system is to increase the number of elements that shares the normal CDMA bus and to reduce the area and power consumption without changing the complexity. The spreading of data and it's decoding are occurred in parallelized manner. So it is known as P-OCI (Parallel Overloaded CDMA Interconnect). Fig.3 shows the PRLE based P-OCI architecture. It uses a simple encoding circuitry. But there are several changes in the accumulator based decoder. In addition to this, a PaCC codec is used to reduce the area needed to store the message data. This can be made possible by using the distinctive properties of the Walsh spreading code, which can identify several sets of non orthogonal spreading codes. One of the main feature of the Walsh spreading code is that the difference between any successive channel sums of data that spread by the orthogonal spreading codes is always even for an odd number of Transmit - Receive pairs B regardless of the spread data. The above feature of Walsh code reveals that for the C-1 pairs of transmitter and receiver which uses the Walsh orthogonal codes, user can encode an extra C-1 data bits in the successive differences between the C chip of the spreading code.

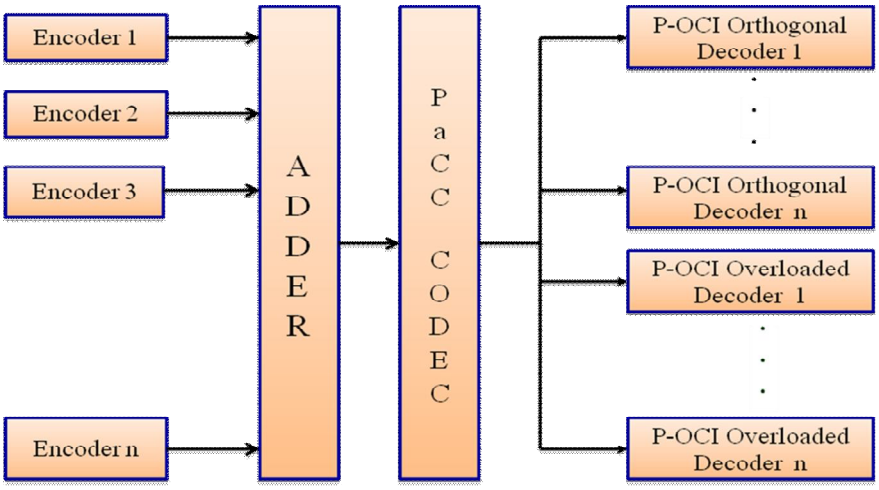

Fig.3. PaCC Codec based P-OCI Crossbar Architecture

This increase the capacity of CDMA bus. In addition to the XOR encoder in the ordinary CDMA, an AND gate is used additionally to encode data with nonorthogonal spreading codes. For each nonorthogonal encoder, a single chip summoned at specific time slot is added to the bus sum if the transmitted data is one. This causes the deviation of consecutive sum difference. Because the suggested codes are similar to TDMA signals. In the case of Parallel Overloaded CDMA Interconnect (P-OCI) crossbar, it utilizes the same Walsh and overloaded codes as the TDMAOCI crossbar . The main difference is the spreading of data and it's decoding are occurred in parallelized manner in P-OCI. In this crossbar architecture, the number of XOR gates and AND gates used for the encoding of data is C. So that the crossbar adder is also replicated into C times. Also separate P-OCI orthogonal and overloaded decoders are needed for the decoding process.

A. Encoder Module

Fig.4 shows the encoder module. The encoder has the capability to encode both the orthogonal and nonorthogonal data. So it is known as hybrid encoder. The XOR operation of the data bit and the Walsh spreading code produce the orthogonal code and AND

operation of data bit and the Walsh spreading code to produce nonorthogonal spread data. A multiplexer is used to choose between the orthogonal and nonorthogonal inputs in accordance with the code type allotted [1].

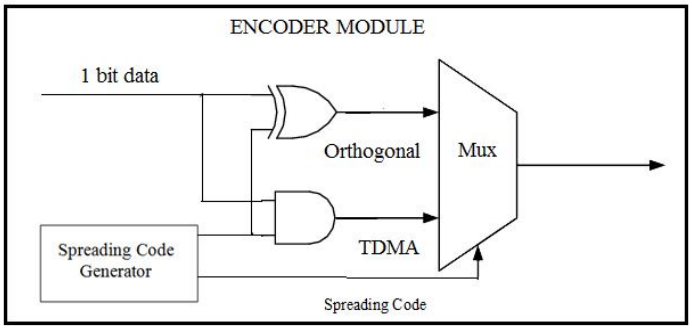

Fig.4.Encoder Module.

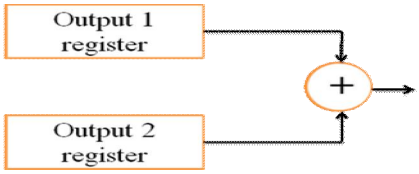

Fig..5. Crossbar Adder.

B. Crossbar Adder

The output of the encoder is stored in two registers in accordance with the spreading code. The crossbar adder structure is shown in the Fig.5. Two registers named output1 and output2 is mainly used to store the encoded data bits . The encoded data bits according to the spreading code value '0' is stored in output 1 register and the encoded data bits according to the spreading code value'1' is stored in output 2 register.

C. PaCC Codec

A Parallel Compare and Compress (PaCC) architecture is mainly used for diminishing the surplus area needed to store the message data. Codec is an important component of the PaCC architecture, which produces less area and high performance. The Parallel Run Length Encoding scheme observes the *q* bits in parallel. If they all are *zero* or *one* all the *q* bits are circumvent in single clock cycle. The value of *q* influence the speed of compression by impacting the bypass opportunity. Fig 6 shows a PaCC based encoder, which offers the Parallel Run Length Encoding mechanism. The shifting network at the input end in PaCC encoder shifts *p* bit from the register and is given to the Run Length Encoding unit. The *p* bit output which produces in the input end shifting network is the shifted value for upgrading the input end registers. Likewise , the shifting network at the output end shifts the *j* bit compression results to the output end registers. The all *zero or one* detector unit helps to perform *q* bit parallel monitoring and generates a bypass signal. The signal is fed to the RLE encoder unit and to the length controller[10].

The function of the length controller is to provide the length of shifting to the shifting network at the input end in accordance to the bypass signal as well as Observation Window Width (OWW) *q*. The Run Length Encoder unit compresses the *q* bit input serially .This will perform only when the bypass signal is in disabled condition, otherwise bypasses the *q* bit input.

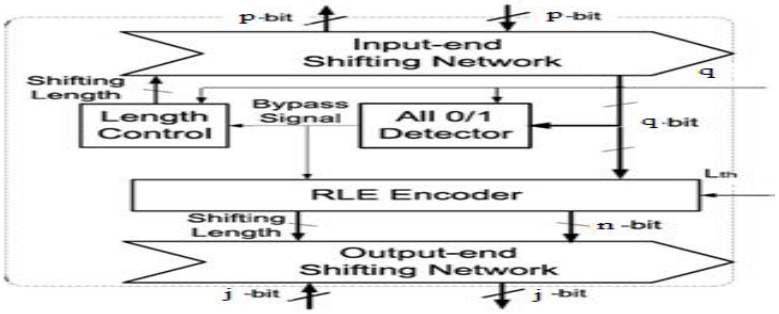

Fig.6. PaCC Encoder.

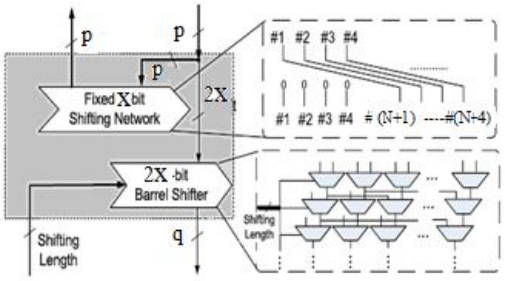

Fig.7. Shifting Network Architecture.

Once the Run Length Encoder unit completes the compression, it sends a compressed segment having length *n* to the shifting network at the output end. The PaCC decoder is almost identical to the encoder. The PaCC decoder can reutilize the shifting networks at the two ends, since encoding and decoding are reverse operations. The input end and output end parts are interchanged and the direction of data flow is in reverse direction. The main dissimilarity in the PaCC decoder is that it comprises an Run Length decoding unit instead of the Run Length encoding unit. Because of the change in the shifting length , there are some challenges occurs while designing the shifting networks. Most commonly the barrel shifter is used for the shifting purposes, but it may consume much area. So that a novel area efficient shifting structure is used for the shifting network at the input and output end. The shifting process can be classified into two stages. The first stage shifting network is a coarse grained, which has a shifting length of X. Here the input is shifted by X. This is an area efficient shifter. In the second stage a barrel shifter of 2X bit is used. It takes the first 2X bits from the p bit input data and use as it's input. The detailed structure of the shifting network is shown in Fig.7

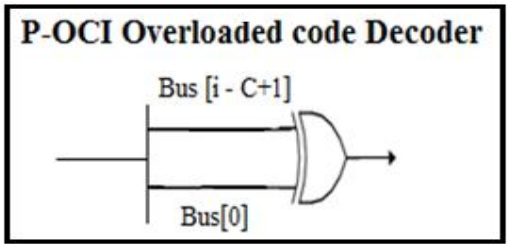

Fig.8. P–OCI Overloaded Decoder.

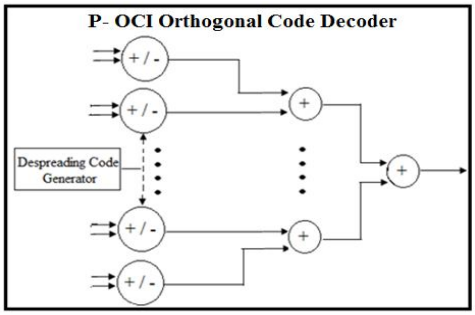

Fig. 9 P- OCI Orthogonal Decoder

D. Decoder

The P-OCI orthogonal decoder shown in Fig. 9 receives the adder sum values concurrently not sequentially; therefore, the accumulator loop is unrolled into a parallel adder. The P-OCI overloaded code decoder consists of only one XOR gate which is shown in the Fig.9.

V. RESULTS AND CONCLUSIONS

In this portion , a comparative analysis between conventional/ normal Code Division Multiple Access, P-OCI crossbar and PRLE based Parallel overloaded on Code Division Multiple Access Interconnect crossbar is done. All the architectures are simulated using Xilinx ISE design Suite 14.5. The various simulation results of the crossbar are shown below. Fig.10.a represents the encoder section of the P-OCI crossbar and Fig.10.b represents the PaCC encoder section of the P-OCI crossbar. Fig 10.c and Fig.10.d shows

the PaCC decoder section and decoder section of the P-OCI crossbar and .The crossbar architectures are evaluated for spreading code length C=8 and is shown in Table.1. The evaluation results includes the resource utilization, area and power consumption. The below results show that the Parallel Run Length Encoding based P-OCI crossbar consumes less area and reduced usage of power when compared with the normal CDMA bus and normal P-OCI crossbar.

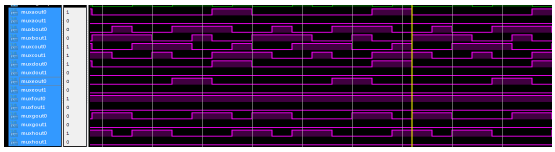

Fig. 10.a P- OCI encoder section

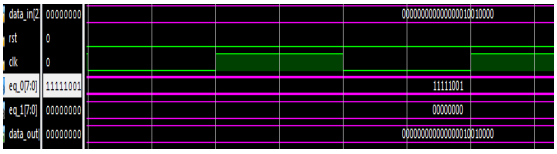

Fig. 10.b PaCC encoder

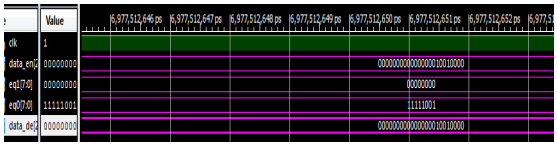

Fig. 10.c PaCC Decoder

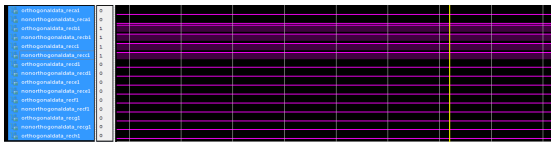

Fig. 10.d P- OCI Orthogonal Decoder

TABLE I.RESULT ANALYSIS

Crossbar / Parameter	P-OCI Crossbar	PaCC Based P-OCI Crossbar
Power	0.040W	0.034W
Clock Period	1.894ns	1.668ns
No of LUT	994	819

VI. ACKNOWLEDGMENT

The authors thank the faculties at T.K.M Institute of Technology for technical discussion and simulation support.

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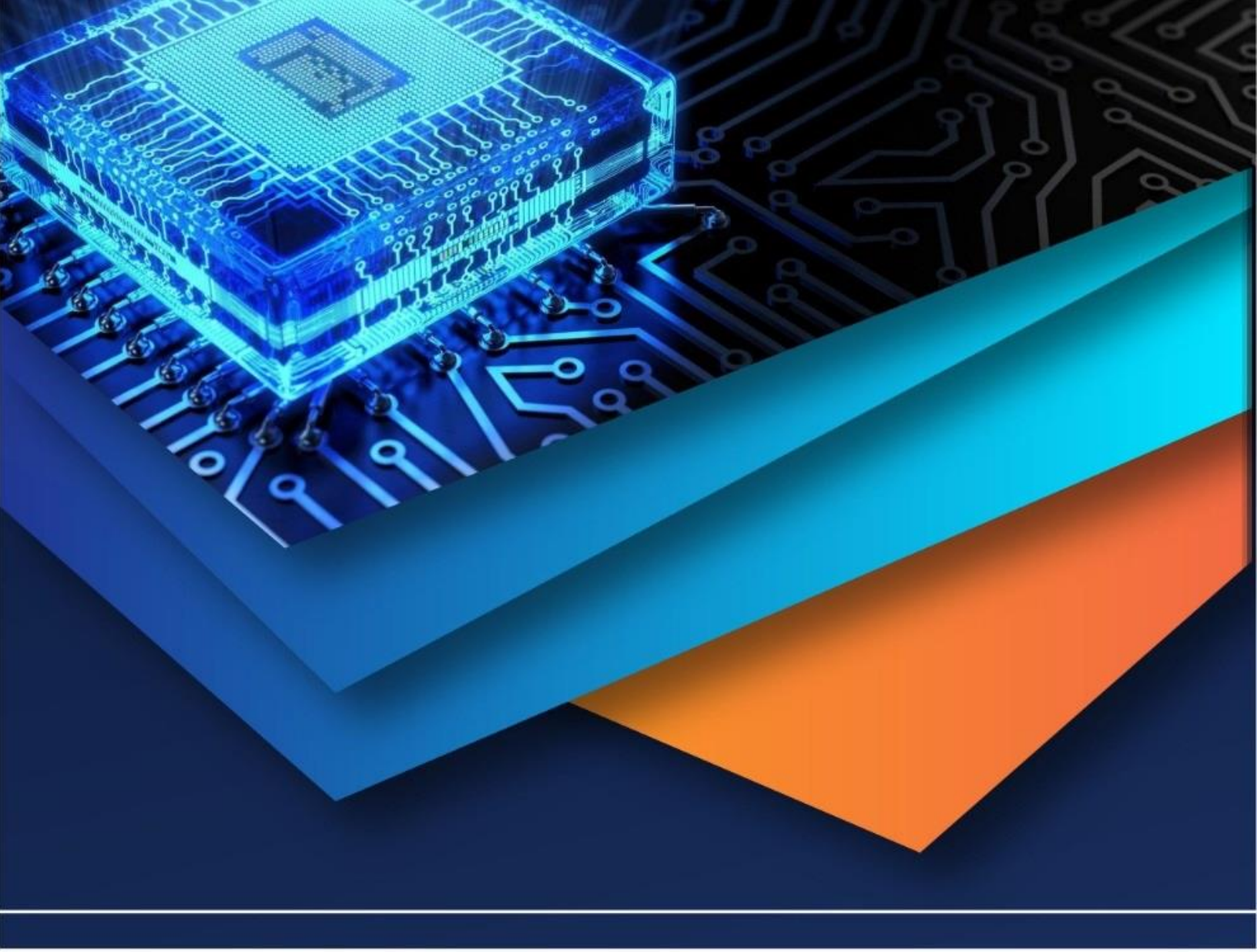

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