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Sigma Delta Modulators: A Review

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Abstract: with ever growing technology scaling, low power operation has become a necessity in VLSI design. Sigma Delta ADC consists major portions of the modern VLSI designs, thus efforts are being made to design low power ,small area sigma delta ADCs using different topologies and methodologies. This paper discusses various existing Sigma Delta modulator designs and topologies, consisting of different number stages and optimizations from one another. This paper focuses on the study of these designs and their comparison on the basis of parameters like power dissipation, structure order, bandwidth, OSR, FOM etc. All the designs studies are application and technology specific but the output bit patterns are similar for similar inputs with variations in rate of output. The simulation environment for the structures was chosen to be PSPICE A/D 16.6 and Sigma Delta Toolbox of MATLAB R2014a.

Keywords: Sigma Delta ADC, Oversampling, SNR, SNDR, FOM, PSPICE.

I. INTRODUCTION

Sigma Delta modulators (DSMs) are a class of oversampling analog-to-digital converters (ADCs) that perform "quantization noise shaping," thus achieving a high signal-to-noise ratio (SNR). An efficient solution for resolutions above approximately 12 bits, DSMs are extensively used in analog and RF applications. In this article, we study the fundamentals of this vast field. Sigma-delta (SD) analog-to-digital converters (ADCs) are employed over a wide range of applications, from low frequency instrumentation to high-speed communication circuits .Continuous-time sigma-delta modulators (CT-SDMs) provide meaningful advantage over their discrete-time (DT) counterparts, as such as lower power consumption, wider input signal bandwidth and implicit anti-alias filter (AAF). Thus, they have been a good choice for power-efficient, high and medium to high resolution SD ADCs targeted to wireless wideband high-speed applications in advanced CMOS technologies. Based on this properties many CTSDM with signal bandwidth of 0.5 MHz to 20 MHz are reported in the literature. Discrete-time (DT), switched-capacitor circuits are a widespread tool for implementing SD data converters. These data converters are pushed by an increasing demand for higher rates and lower consumption SD converters in order to handle, e.g. current mobile high bandwidth communication systems. DT Modulators have enhanced their performance due to the improvement in microelectronics manufacturing methods along with architectures that work accurately in the discrete domain. Sigma-delta converters operation is based on the quantization noise shaping principle. The signal processing path is built in such a way that noise spectrum transformation is different from signal spectrum transformation. In this case signal transformation is characterized by signal transfer function (STF) while noise transformation is characterized by noise transfer function (NTF).[1]

The evolution of the CMOS technology during the last decades has allowed the presence of electronic systems in many aspects of our daily life: automotive, communications, consumer electronics, information technology, medicine, etc. Clearly, the most important evolution is the geometry dimension reduction of the devices and interconnections of the CMOS technology. In addition, the power supply voltage has been to maintain moderate electric fields inside the device thus avoiding large leakage currents. Consequently, the power consumption of the digital circuits has diminished, further enhancing their performances. The mentioned features have permitted to integrate complete electronic systems on a single chip. This is commonly known as system-on chip (SOC). The essential part of the interfacing circuits on a SOC is done by the ADC and the digital-to-analog converter (DAC). Among the existing ADC topologies, the SD ADC is the more suitable solution for SOCs implementations since it is able to achieve high accuracy at a reasonable speed conversion, leverages the digital CMOS process features and is relatively insensitive to fabrication process variations. This balance is obtained using noise shaping technique and high sampling rate at the cost of the circuit complexity.[2]

A SD modulator inside a SD ADC utilizes the concept of oversampling. From the Nyquist theorem, it is known that the minimum frequency (called Nyquist frequency fN) to sample a signal with bandwidth fb is 2fb. Hence, the oversampling ratio (OSR) quantities by how much the sampling frequency (fs) is greater than the Nyquist frequency:

$$OSR = \frac{fs}{fN} = \frac{fs}{2fb}$$

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When an ADC operates with an OSR greater than one, it is called an oversampling ADC. This architecture adds a decimator to the process conversion to filter the oversampling data and reduces the sampling frequency by the same value as the OSR.[3]

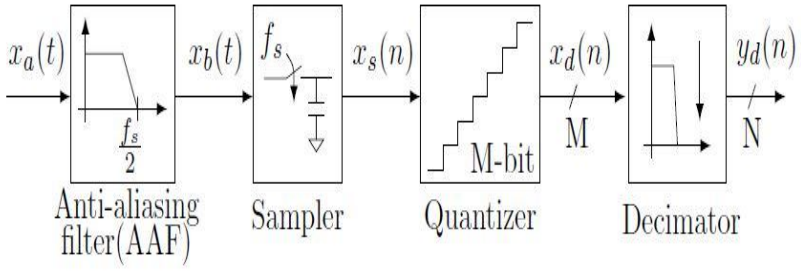


Fig 1. : Basic oversampling ADC.

An advantage about using oversampling ADCs is that the specifications of the AAF are relaxed because the signal bandwidth is smaller than fs=2 and hence the images of the signal are more separated than in a Nyquist-rate converter .Furthermore, the quantization noise power is reduced since only a fraction of the total noise affects the signal.

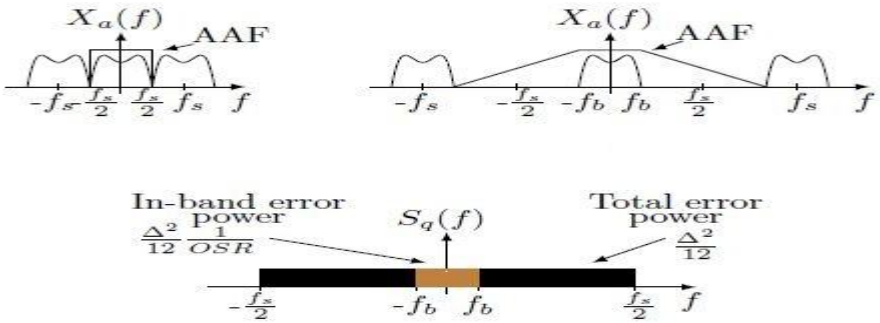


Fig 2: Quantization noise power in OS ADC.

The oversampling idea was initially conceived to improve the transmission of the pulse code modulation (PCM). It consists of transmitting the sample changes at high sampling rate instead the actual samples. The idea was based on the operation of the human brain, whereby the physiological signals are transmitted to the brain by a series of electrical pulses in the nerve system. Figure 3 shows a block diagram where if the ADC is a 1-bit quantizer, the structure is called delta modulator and if it is a multi-bit quantizer, it is called as differential PCM. The basic operation consists of comparing the input signal with an estimate of the output data and quantizing this error. The feedback signal is obtained by integrating the DAC output which is the analog estimation of the digital output. This structure is advantageous for oversampling signals since the amplitude of the difference signal is much smaller than that of the input signal.[4]

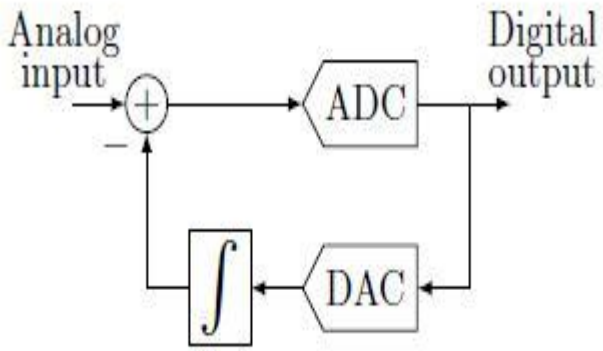


Fig.3: Delta Modulator

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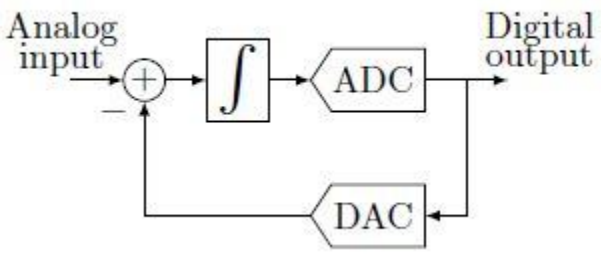


Fig. 4: Sigma Delta Modulator.

Since the SD modulator is the key of the converter operation, a basic modulator is analyzed to understand its operation. Assuming that the loop filter is a discrete time (DT) forward-Euler integrator,[5]

$$H(Z) = \frac{Z^{-1}}{1 - Z^{-1}}$$

The linear model of a first order SD modulator can be represented by the block diagram shown in Fig. 2.8 whose output is:

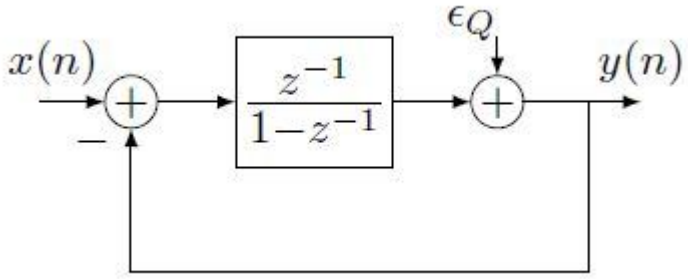


Fig. 5: linear Model.

$$Y(Z) = \big(X(Z) - Y(z)\big)\frac{Z^{-1}}{1 - Z^{-1}} + E_Q$$

Which leads to:

$$Y(z) = X(z)Z^{-1} + E_Q(1 - Z^{-1}) = STF(Z)X(Z) + NTF(Z)E_Q$$

Where STF and NTF are the signal transfer function and noise transfer function, respectively. From these expressions it is clear that the input is replicated at the output only delayed by one clock period and the quantization noise is shaped by a high-pass filter.[6]

II. DIFFERENT MODULATOR DESIGNS

Low power modulators receive more attention in industry, and the following reviews include several modulators targeting industrial applications. This paper targets low power SDM design with low-megahertz sampling rates with output resolutions larger than 10 bits. Since performance and power consumption are the most critical factors in these designs, the following criterion was used to compare modulators across different architectures.[7]

A. An area-efficient feed forward multi-bit sigma-delta modulator is designed in this paper. By adopting fourth-order 17-level quantization structure, the modulator can achieve 20-bit resolution of 20 kHz signal bandwidth with 64 oversample ratio. A novel full feed forward architecture is employed in this modulator, which minimize every stage load to save chip area and power consumption by select relatively large coefficients without compromising the stability. In addition, a 4-bit quantizer is composed of only 9 comparators. A simple data weighted averaging (DWA) is used to relieve the 1st integrator feedback capacitor mismatch problem. The modulator is implemented in high voltage 0.35J.tm CMOS process with 5V supply voltage. The simulated signal-to-noise-and-distortion-ratio (SNDR) of the modulator is 117.8dB with -6dBFS sinusoidal input.[1]

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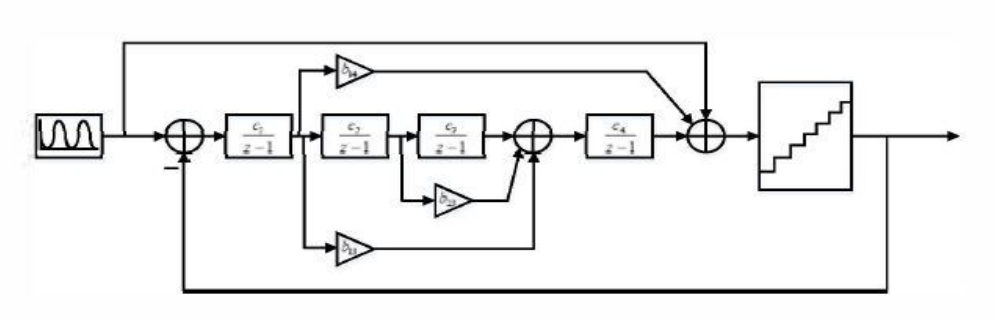


Fig. 6: Structure of 4Th order area efficient SDM

B. This paper describes the design and implementation of a low-pass third-order single-loop single-bit continuous-time sigma-delta modulator (CT-SDM) in a 130 nm CMOS process. To reduce clock jitter effects and operational amplifiers requirements a non-return-to-zero (NRZ) digital-to-analog converter (DAC) pulse shape was employed. Post-layout simulation results indicate that the modulator achieves 56 dB of dynamic range, 57.31 dB of peak SNDR or 9.23 bits of effective resolution over a 1 MHz signal bandwidth with an oversampling ratio (OSR) of 64. The CT-SDM draws 5.91 mW from a 1.2 V power supply providing a figure-of-merit (FOM) of 4.93 pJ/conv. The CT-SDM core area is 0.31 mm^2.[2]

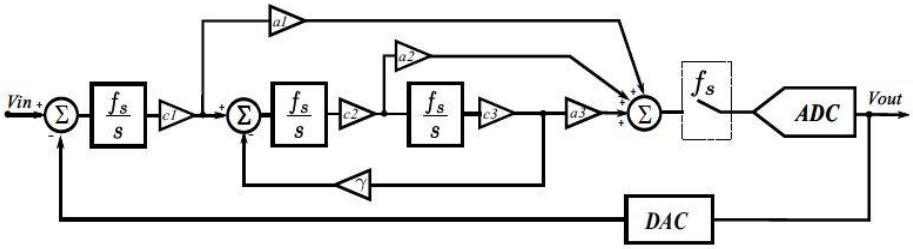


Fig. 7: Structure of 3rd order SDM.

C. Matrix form representation of sigma-delta modulator structure allows to easily obtain its signal and noise transfer functions. Those functions are necessary to analyze important modulator features: potential signal to noise ratio and stability of the modulator.[3]

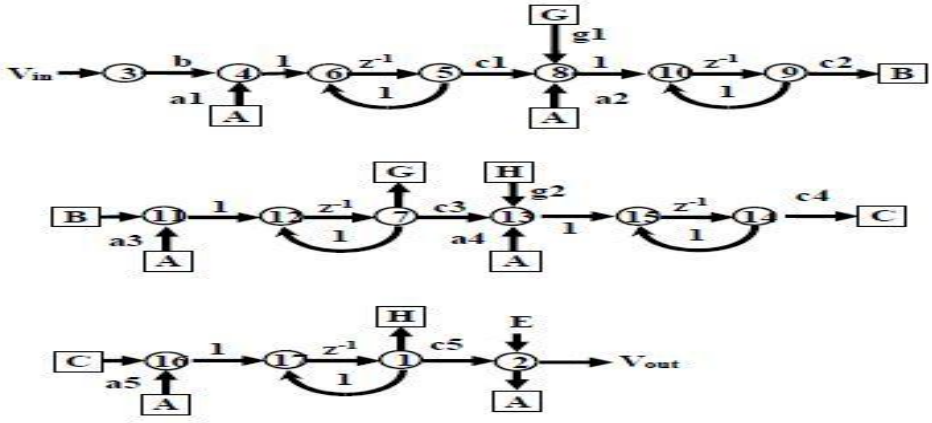


Fig.8: Signal flow representation of 5th order SDM.

D. The paper presents deep insights of design and simulation of the Delta-sigma modulation scheme to convert Analog signals to Digital Signals using Cadence Virtuoso Design tool. Here Sigma Delta Modulator analog signals are encoded into digital signal as in regular ADC. The main thrust behind the Delta modulation was to accomplish higher transmission proficiency by transmitting the progressions (delta) in quality between the back to back examples instead of genuine samples themselves. Since there is no restriction to the quantity of pulses of the similar sign that may happen, this frameworks are equipped for

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following signals of any adequacy. In this work, it is explained about the design and simulation of Integrator, Latched Comparator, Ring Oscillator, Digital To Analog converter which are combined together to form the Sigma Delta Modulator using the 350nm CMOS technology.[4]

E. A low-voltage low-power 3th-order continuous time (CT) sigma-delta (ΣΔ) modulator is presented in this paper for biomedical applications. In order to lower the power consumption, a new loop filter with a single-opamp resonator, a 4-bit asynchronous successive-approximation register (SAR) analog-to-digital converter (ADC) and a capacitance digital-to analog converter (CDAC) have been employed. The single-opamp combined with the passive elements can benefit the power consumption as well as the stability. The feedforward compensation scheme is employed to further reduce the power consumed by opamp, and the chopper stabilization technique is used to eliminate the 1/f noise. Moreover, the multi-bit SAR ADC and the DAC reduce the effects caused by clock jitter and thus improve the signal-to-noise ratio (SNR). The ΣΔ-modulator is designed in a 0.18µm CMOS process, which totally consumes 1.7µW in a 0.8V supply with 50KS/s sampling rate and results in a FOM of 25.9fJ/conversion. Within the 500 Hz bandwidth, the circuit achieves peak SNR of 104.5dB, SFDR of 114.0dB and DR of 72dB, respectively.[5]

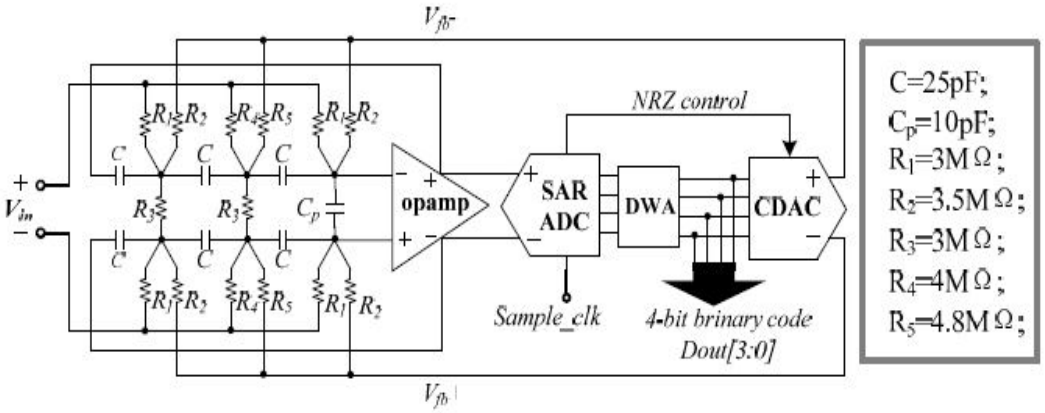


Fig. 9: Prosed Scheme for CT SDM.

F. This paper summarizes the research work carried out during a doctorate studies, which is focused on the synthesis and design of a 4th Order SD Modulator in Discrete Time (DT) implemented in a 130nm CMOS process. By means of SIMSIDES the high-level simulation of the modulator is analyzed in order to translate the design specifications into a set of values such that the transistor level blocks be established by the desired performance of the proposed architecture. At the transistor level design, special attention is focused to the OTA, since this block is the main source of non-idealities in a Switched Capacitor (SC) Integrator. Moreover, the gm=ID methodology is implemented into this stage as a tool to obtain the optimum circuit performance based on power consumption and better signal-to-noise ratio.[6]

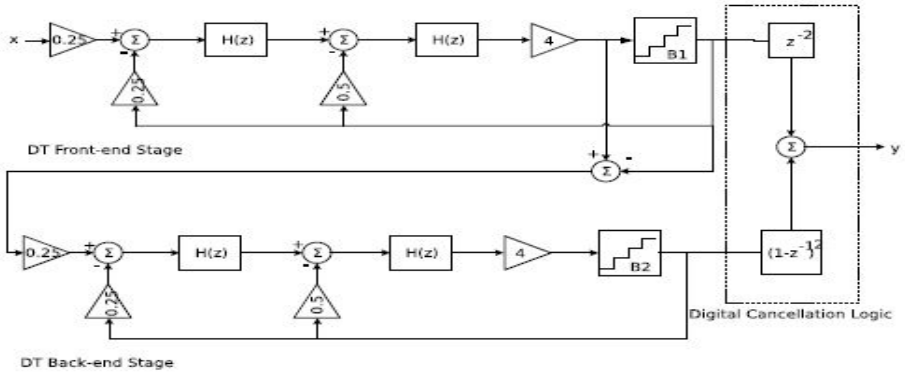


Fig.10: Fourth order DT SDM.

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G. Integrating sigma-delta modulator (SDM) in FPGA causes to have quantization noise inside interested bandwidth. This paper compares and analyzes between two possible FPGA based SDM structures which are non-noise shaper SDM and noise-shaper SDM. The difference between these two structures is in the integrator block. All other SDM constitutive components are the same for both structures. First-order noise-shaper SDM with its maximum integration for FPGA implementation is reported. The advantages of noise-shaper SDM over non-noise shaper SDM are the elimination of input peak signal error as well as the increment of input voltage range. Moreover, higher suppression in signal harmonics results in better reconstruction of input signal at the output. However, the most important outcome is the improvement of quantization noise shaping out of the interested bandwidth which results higher SNR at the output.[7]

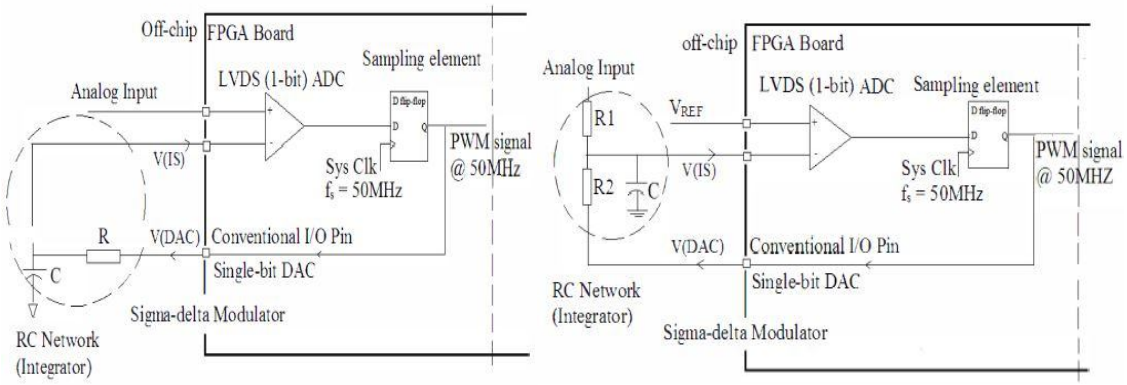


Fig .11: 2 SDM architectures using passive components.

H. This paper discusses the use of a low gain amplifier and a passive switched-capacitor (SC) network to enable the SC integrator function. The method is applied to a delta sigma modulator to achieve high resolution as proved by the 65-nm CMOS technology test vehicle. Compared with the conventional operational amplifier (op-amp)-based SC integrator, this solution utilizes a low-gain open-loop amplifier to drive a passive SC integrator with positive feedback. Since the open loop amplifier requires a low dc gain and implements an embedded current adder, the power consumption is very low. Power reduction for single bit is obtained by using passive feedforward with built-in adder to assist the first amplifier. The low swing obtained at the output of the active blocks relaxes the slew rate requirement and enhances the linearity. Implemented in 65-nm digital CMOS technology with an active area of 0.1 mm2, the test chip achieves a dynamic range of 91 dB, peak signal-to-noise ratio of 88.4 dB, peak signal-to-noise-plus-distortion ratio of 88.2 dB, and a spurious free dynamic range of 106 dB while consuming 73.6 μW in a 25-kHz signal bandwidth at 1 V supply, yielding a FoM Walden of 70 fJ/conv-step and FoM Schreier of 176 dB.[8]

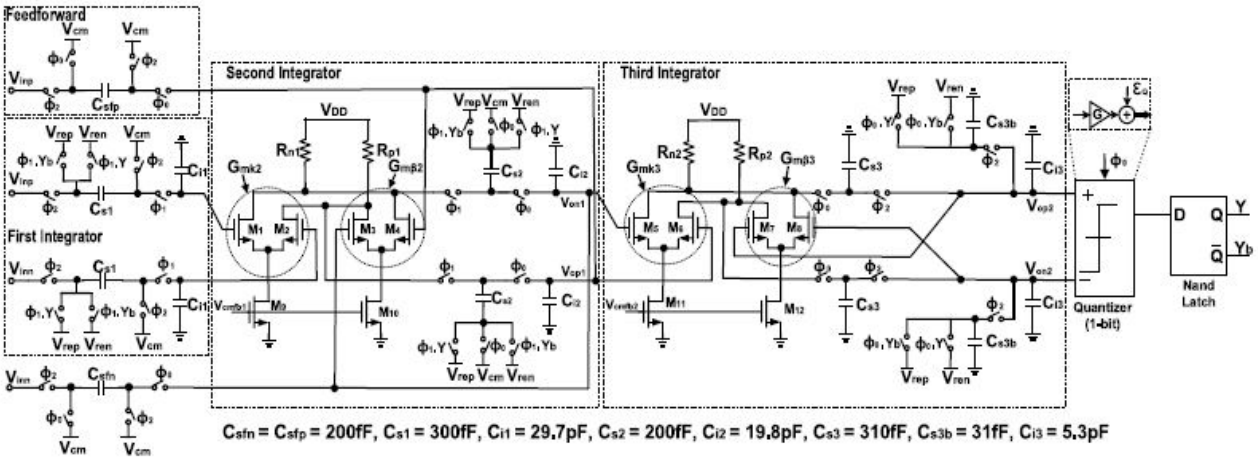


Fig.12: Fully differential SC 3rd order SDM

I. There is developed the simulation model of single bit third order sigma-delta modulator. It provides investigation of the influence of components' parameters on modulator's error. It is presented results of investigation of integrator's nonlinearity on integral nonlinearity of this modulator. The presented results provides purposeful selecting of correction function for correction

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nonlinear error of analog to digital converters based on presented modulator. Also the proposed methodology provides opportunity of parametric optimization in development of sigma-delta modulators.[9]

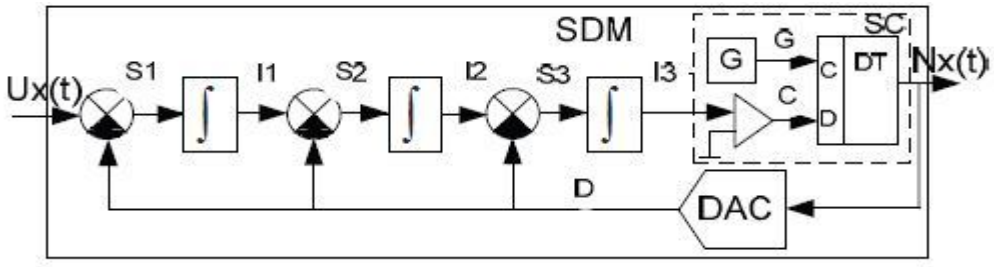


Fig. 13: 3rd order single bit SDM

J. This paper presents a MASH __M using only passive integrators and simple differential pairs as low-gain blocks. Instead of high-gain power hungry op-amps it uses more processing gain from the comparator (1-bit quantizer) as a part of the loop gain. The proposed approach allows the design of a continuous-time, 2-1 MASH __M in a 65-nm CMOS technology occupying an area of just 0.027 mm2. Measurement results show that the modulator achieves a peak SNR/SNDR of 76/72.2 dB and a DR of 77 dB for an input signal bandwidth of 10 MHz, while dissipating 1.57 mW with 1 V supply. The proposed __M achieves a Walden figures of merit (FoM) of 23.6 fJ/level and a Schreier FOM of 170 dB.[10]

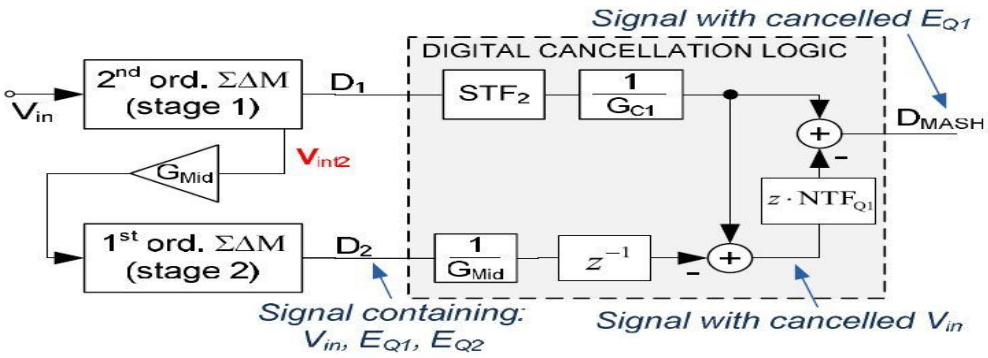


Fig.14: 2-1 MASH SDM.

K. A passive 2nd-order sigma-delta modulator using switched-capacitor based filters was designed, fabricated, and tested. A novel 2nd-order single feedback path topology is used. All circuitry is optimized for low power operation through the use of minimum size MOSFETs, component reduction and topology choice. The modulator was fabricated in On Semiconductor's C5 500-nm process. The implementation achieves a typical SNDR of above 50 dB for tested frequencies of 10 Hz to 3 kHz and has a peak SNDR of 57.8 dB, which corresponds to an ENOB of 9.3 bits. With a 2.5 V supply, the power consumption of the sigma-delta modulator is 6.75 µW. The modulator achieves a FOM of 1.78 pJ/step.[11]

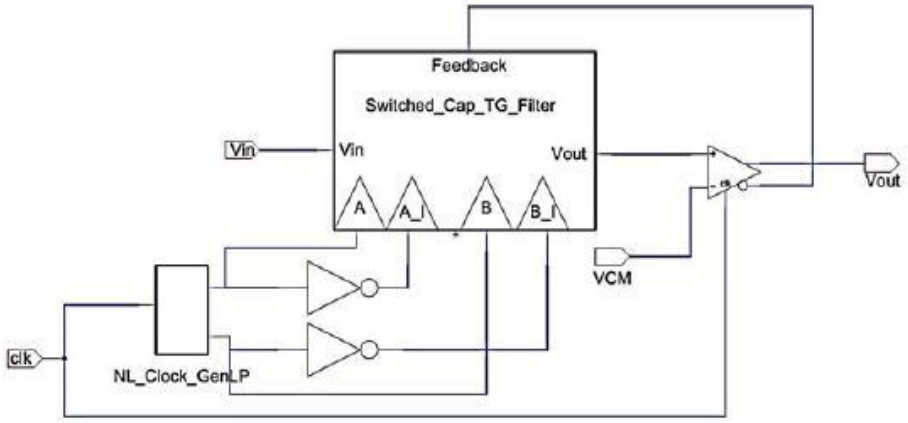


Fig. 15: 2nd order SDM.

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L. In this work, a 3-bit feedforward 3rd order sigma delta analog-to-digital converter (ADC) is presented. In this proposed architecture, feedforward paths and multibit design help the integrator output swings to become smaller, which renders the exploitation of a telescopic cascode opamp in the integrators possible. Moreover, a double sampling method is used to relax the opamp specifications. The proposed sigma delta ADC consumes 28.2 µW and has 81.3 dB SNDR according to post layout simulations.[12]

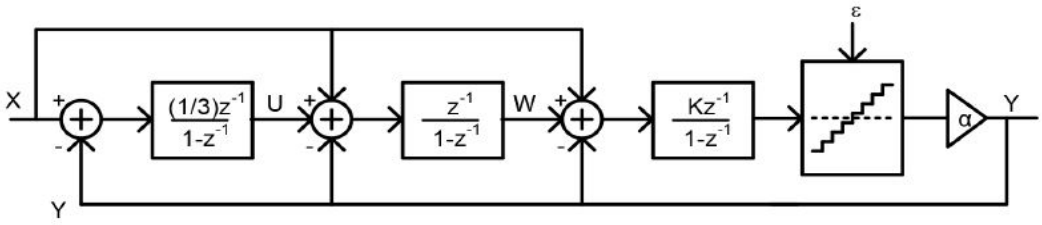


Fig. 16: 3rd Order SDM.

III. RESULTS & DISCUSSIONS

In this section all the existing SD modulators designs and topologies are compared on the basis of below listed parameters in Table 1.The results were obtained by designing all the structures in their respective technologies using PSPICE A/D and Delta Sigma Toolbox.

The FOM parameter is obtained as:

$$FOM = power/(bandwidth * 2^{ENOB})$$

Where ENOB is the effective number of bits given as:

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

Table I
Comparisons

Work	Process	Supply (V)	Structure (order)	Bandwidth	OSR	SNDR (Db)	Power	FOM (J/con)
[1]	0.35 µm	5	4th	20Khz	64	117.8	6.78mW	0.32p
[2]	130nm	1.2	3rd	1Mhz	64	57.31	5.91mW	4.93p
[4]	350nm	1.8	1st	2Khz	32	48.21	32.8mW	19.21p
[5]	0.18 µm	0.8	3rd	500Hz	64	98	1.69 µW	25.9f
[6]	130nm	0.6	4th	10Mhz	10	80.2	3.2mW	5.2p
[8]	67nm	1	3rd	25Khz	260	88.2	73.6 µW	70f
[10]	65nm	1	3rd MASH	10Mhz	256	72.2	1.57mW	23.6f
[11]	500nm	2.5	2nd	3Khz	170	57.8	6.75 µW	1.78p
[12]	180nm	1.8	3rd FF	25Khz	64	81.3	28.2 µW	59f

It can be observed from the above table that the process technology plays an important role in the overall efficiency of the structure. Smaller the process technology, smaller if the FOM which is supposed to be low for better structure.

IV. CONCLUSION

Sigma-delta ADCs and DACs have proliferated into many modern applications including measurement, voice band, audio, etc. The technique takes full advantage of low cost CMOS processes and therefore makes integration with highly digital functions such as practical applications in DSP. Resolutions up to 24-bits are currently available and the requirements on analog anti-aliasing /anti-imaging filters are greatly relaxed due to oversampling.

In this paper we presented an extensive review of existing Σ-Δ modulators in literature. We conclude that the following few points:

1) Low order modulators are easy to design but have sufficient noise still present at the output, even though the design is simple, occupy less area and consume less power but the SNDR value id low around 50dB.

2) The process technology is inversely proportional to the FOM of the structure.

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3) In order to decrease the supply voltage for low power operation, we need to shift to a lower process technology, else the system switch level operation reduces greatly in efficiency.

4) In case we use the same supply voltage for the two process technologies, the chances of leakage current increment increases greatly.

5) The order of the filter is directly proportional to the SNDR and FOM.

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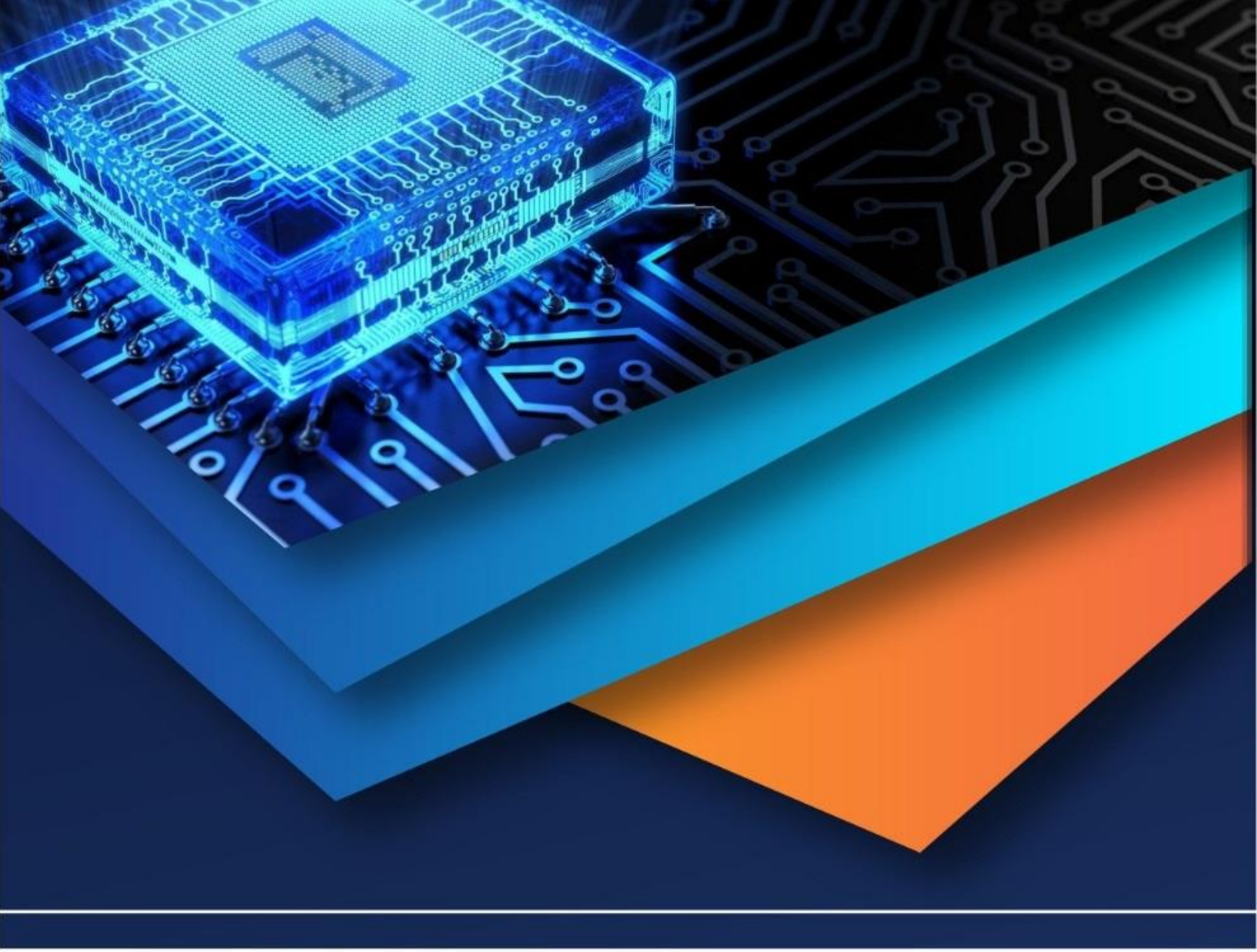
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