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# Low Power Design Techniques in CMOS Circuits : A Review

Agrakshi[#1], Suman Rani[#2]
[#]*Electronics and Communication Department, PPIMT Hisar, Haryana, India*

***Abstract*— In the design of digital integrated circuits, power consumption is an important criterion. That indicates that low power circuits are now a days, emerging as an utmost priority in modern VLSI design. This is in contrast with the early 70s, when providing high speed operation with the least area was the main aim of design. But of course, other factors like area, propagation delay, leakage current etc. also can not be ignored in the design process. Out of these techniques, some are quite efficient in reducing static (leakage) power .This paper is prepared to review the available low power design techniques that are pivotal in designing various digital circuits.**

**Keywords—** ***Leakage Power, Low Power, Power Dissipation, Power Management, Sleep Transistor***

## I. INTRODUCTION

Power consumption (dissipation) in digital circuits is a primary concern as it affects the chip life and circuit's efficiency due to overheating of circuit [27].Thus there is a need to reduce the power dissipation as much as possible. There are different reasons for reducing power consumption depending upon a particular application. For instance, in the field of mobile communication, battery life needs to be maximized. This demands low power consumption by these devices. As the technologies are getting miniaturized ,power management has become a challenge. There are many techniques available today that help in achieving the aforementioned goal i.e. reducing power consumption. Some of them are power gating, clock gating while some are drain gating techniques. A review of some of these techniques as discussed in [3], [4], [8], [20], is done, mentioning their pros and cons.

## II. LOW POWER DESIGN TECHNIQUES

### *A. Sleep Transistor Technique*

In the traditional sleep technique, additional 'sleep' transistors are inserted between power supply and ground. The 'sleep' pMOS transistor is placed between Vdd and the pull-up network of a circuit and an additional 'sleep' nMOS transistor is placed between the pull-down network of the circuit and GND. In idle mode, these sleep transistors turn off the circuit by cutting off the power rails thereby reducing the leakage power. In the active mode, however, these sleep transistors are turned on thereby providing a low resistance path and un-affecting the circuit performance.

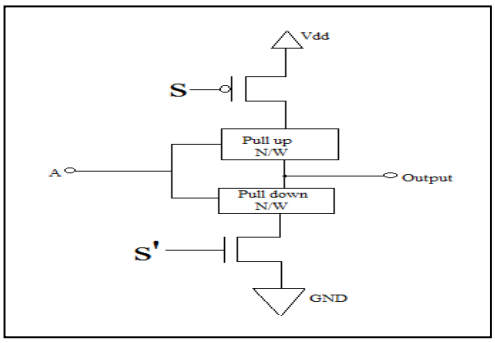


Fig. 1 Sleep Transistor Circuit

1) *Advantages:* With a simple implementation, it is efficient in controlling leakage current.
2) *Disadvantages:* It is not suitable for state retention. It leads to floating output voltage in sleep state. Also, an increase in layout area and delay is observed. Moreover, it needs an additional control circuitry.

*B. Power Gated Sleep Approach*

A new approach is as discussed in [16], called power gated sleep method.

This method operates in 3 modes:

Active mode (AM).

Standby mode(SM).

Sleep to active mode transition (SAM).

In AM, logic '1' is applied to the sleep signal and both the sleep transistors E1, E2 remain ON. Then a low resistance path is offered by P1, P2 which makes the virtual ground (VGND) node potential, pulled down to the GND potential.

In SM, initially, the sleep signal is held at logic'1' and both the sleep transistors P1, P2 remain ON. Simultaneously, the control transistors E1 & E2 are switched OFF by giving logic'0'. In this case too, a low resistance path is offered by P1, P2 which makes the virtual ground (VGND) node potential, pulled down to the GND potential. As P1 and P2 are turned off, they produce a stacking effect thereby reducing the leakage current (power). The opposite occurs for the upper switch.

During SAM, P1 and P2 are turned ON after a small duration of time. That implies that the logic circuit is isolated from the ground for a short duration of time. During this duration the leakage current is reduced by the stacking effect.

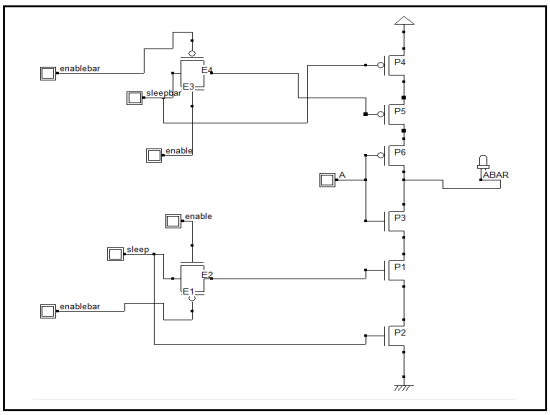


Fig. 2 Power gated sleep method (for inverter)

1) *Advantages:* It takes the benefit of stack effect for reducing leakage current with appreciable performance without the need of a variable threshold device. It provides state retention.

2) *Disadvantages:* It increases the layout area and propagation delay.

*C. LECTOR Technique*

Leakage Control Transistor (LECTOR) is another way to be used as a low power retention technique. In this approach, two extra LCTs: a pMOS and an nMOS are inserted within the circuit. It is a kind of drain gating technique. The gate terminal of each LCT is controlled by the source of the other. This effective stacking of transistors in the path from Vdd and GND helps in reducing leakage power and enhances the circuit performance. One of the LCT is always "near to its Cut-off" voltage region of operation regardless of any input combination.

1) *Advantages:* It utilizes both idle and active states of the circuit for leakage reduction. It uses stacking approach between the power supplies for leakage current reduction. Resistance path between the power rails is increased as one of the LCT is always in OFF state. No additional circuit is required for control. Exact logic state is maintained as it works in both the idle and active mode [15].

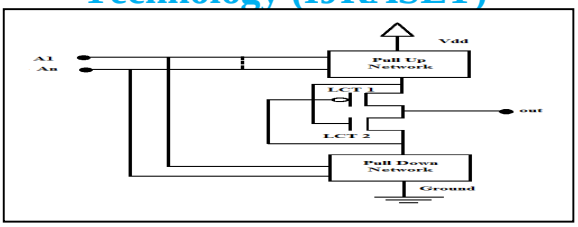


Fig. 3 LECTOR Technique.

*D. GALEOR Technique*

It is another way of introducing stack effect in the logic gate to reduce leakage current. In this technique a gated leakage nMOS transistor is placed between output and pull up circuit and similarly a gated leakage pMOS transistor is placed between output and pulled down circuit [8].
GLTs used in this technique are high threshold voltage devices.

1) *Advantages:* It introduces stack effect between the power rails which helps in leakage control. With the introduction of variable threshold devices between the logic, it effectively reduces the leakage power.

2) *Disadvantages:* Its major disadvantage is that it reduces voltage swing at the output which further results in an increased propagation delay in the circuit.

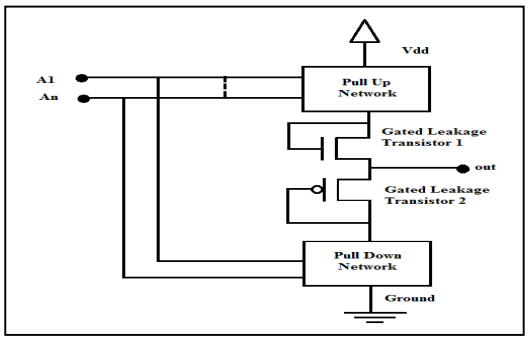


Fig. 4 GALEOR Technique.

*E. GDI (Gate Diffusion Input) Technique*

GDI method is a highly efficient method that helps in reducing area, power and delay in digital circuits. It is based on the use of a simple cell as shown in Figure 8. A GDI cell consists of 3 inputs: G (common gate input of pMOS and nMOS), P (input to the source/drain of pMOS), and N (input to the source /drain of nMOS) [3].

Added features:

- The source of PMOS in a GDI cell is not connected to VDD and source of NMOS is not connected to GND. This increases the flexibility of circuit design with GDI cell.
- Bulks of both NMOS and PMOS are connected to N or P (respectively).

1) *Advantages:* It uses less number of devices as compared in CMOS and PTL. Also there is a significant reduction in power dissipation.
Complex logic functions can be easily 2-transistor implemented. Layout area occupied is less as compared to conventional techniques.

2) *Disadvantages:* It must be noticed that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS technologies [3].

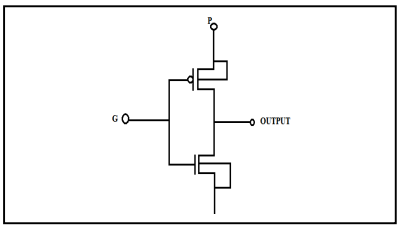


Fig. 5 Basic GDI Cell

TABLE I
GDI Logic Functions

| S. No. | N | P | G | Output | Function |
|---|---|---|---|---|---|
| 1. | B | '1' | A | Abar+B | Function 1 |
| 2. | '0' | B | A | AbarB | Function 2 |
| 3. | B | '0' | A | AB | AND |
| 4. | '1' | B | A | A+B | OR |
| 5. | '0' | '1' | A | Abar | NOT |
| 6. | C | B | A | AbarB+AC | MUX |

*F. AVL (Adaptive Voltage Level) Technique*

An adaptive voltage level technique as described in [13], [20], [23], [24] can be used to control circuits either at the upper end of the cell (to bring down the supply voltage value) ,called AVLS Scheme; or at the lower end of the cell (to lift the potential of ground node ),called AVLG Scheme.

1) *AVLG Technique:* In this technique, two pMOS transistors and one nMOS transistor are connected in parallel. pMOS transistors are connected to ground while an input clock pulse is applied at the nMOS. This circuit is connected between pulled down network and ground. This increases the ground node potential. pMOS transistors are always in ON state since they are forward biased, while nMOS is switched between states. Thus leakage current flowing through nMOS of AVLG circuit is reduced and hence the power consumption is also reduced.

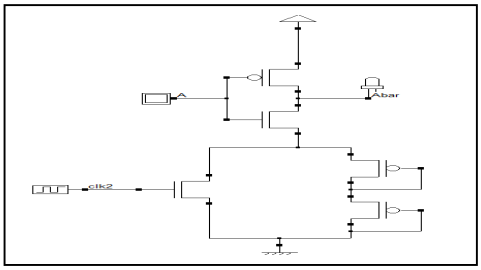


Fig. 6 AVLG Technique at Inverter Circuit

2) *AVLS Technique:* In this technique, two nMOS transistors and one pMOS transistor are connected in parallel. nMOS transistors are connected to supply voltage while an input clock pulse is applied at the pMOS. This circuit is connected between pulled up network and supply voltage. This reduces the supply node potential. nMOS transistors are always in ON state since they are forward biased, while pMOS is switched between states. Thus leakage current flowing through pMOS of AVLS circuit is reduced and hence the power consumption is also reduced.

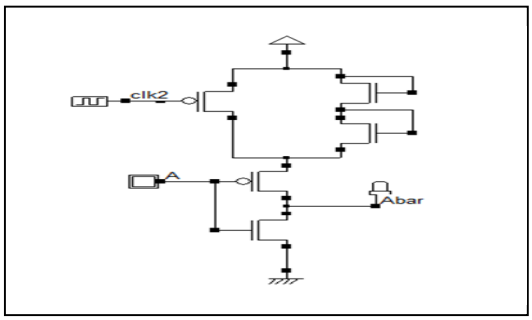


Fig. 7 AVLS Technique at Inverter Circuit.

*3) Advantages:* This method is highly efficient in reducing both the leakage power and the dynamic power.It eliminates the use of variable threshold devices.This approach is highly advantageous for state retention.

*4) Disadvantages:* This method increases propagation delay. Also, the layout area increases.

## III. CONCLUSION

Today, as the technology feature size is shrinking, it has become a challenge for the designers to maintain the power consumption in the tolerable limits without affecting much the other dependent parameters like area and delay overhead. In this paper, review of some of the commonly used low power design techniques is presented. Each of the discussed technique has its own merits and demerits. The designers may wisely select the one that best fits their requirement and design criteria.

## IV. ACKNOWLEDGMENT

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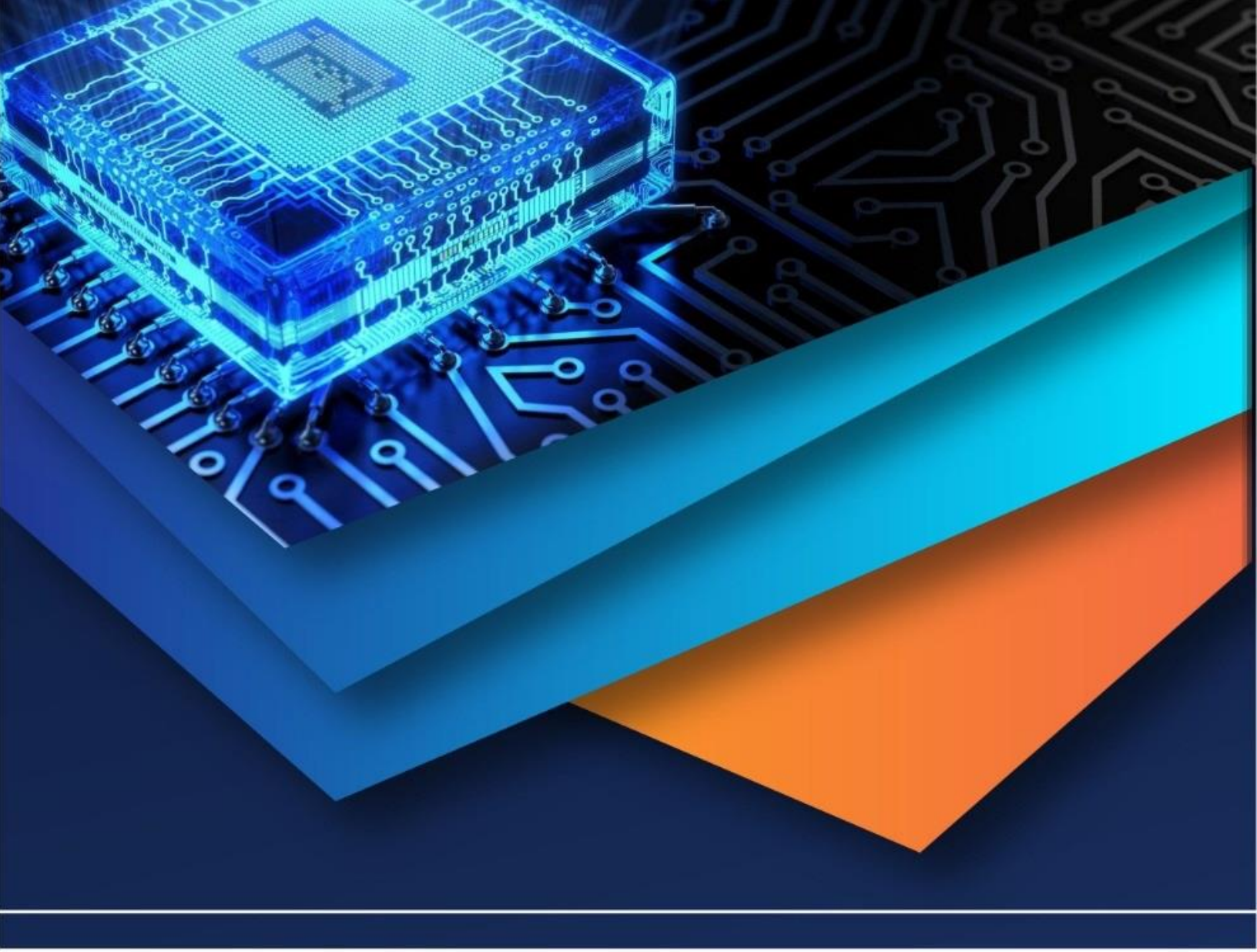

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