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A Novel Nine-Switch Nine-Level Hybrid Inverter

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Abstract: ***Voltage Source Multilevel Converters (VSMCs) have been developed in the last years for high-power applications, due to their capability to work at medium-voltage levels without power transformers. With higher number of voltage levels, smoother AC voltage with reduced harmonic distortion can be generated by the multilevel inverter. Symmetrical inverter topologies allow expanding the topology to an arbitrary number of levels by stacking basic cells. But it results in more complexity and becomes impractical when the number of voltage levels increases. Also these topologies suffer a natural voltage unbalancing on the DC bus capacitors, which requires extra hardware or intelligent control of the switching sequences in order to counteract this effect, a novel nine-switch nine-level hybrid inverter combining the features of the conventional flying capacitor type, diode-clamped type converter and H bridge topology is proposed. The proposed novel topology employs only nine active switches, two discrete diodes and three capacitors. This work also presents the comparative study of control strategies using various Multicarrier Pulse Width Modulation techniques. Performance factors such as THD, efficiency, rms value of fundamental component etc. are measured for two modulation techniques and the results were analyzed. The simulation of nine-switch nine-level hybrid inverter is done by using MATLAB/ SIMULINK software. Arduino is used for generating control pulses for the switches. The prototype of proposed inverter is setup and verified its performance.***
Keywords: Hybrid inverter, SPWM, Level Shifted SPWM, ANPC, THD

I. INTRODUCTION

This document is a template. For questions on paper guidelines, please contact us via e-mail. Multilevel Inverters have received increased attention in both academia and industry nowadays as one of the optimal solutions of power conversion for medium and high power applications. For medium-power application, the motivation for the use of multi-level inverters is to reduce the switch voltage stress as well as the output filter size. They also have the advantages of improved output quality, lower Total Harmonic Distortion (THD), lower common-mode voltage, and lower electromagnetic interference in contrast to their two-level counterparts. Furthermore, the multilevel inverters have possibility to achieve higher efficiency over the conventional inverters due to the use of low voltage stress devices, leading to their low voltage application such as photovoltaic (PV) cells. Three types of symmetrical multilevel inverter topologies: neutral point clamped (NPC) type, flying-capacitor (FC) type and cascaded H-bridge (CHB) type, are used to develop this hybrid topology.

The NPC-type multilevel inverters generate the voltage levels from the neutral point voltage by adopting the clamping diodes. However, when voltage level increases, more clamping diodes, active semiconductor switches, and dc-link capacitors are needed. The dc-link voltage balancing problem is another issue for higher levels NPC inverters. [1] The FC type inverter produces the required output voltage levels by summing the FC and dc-link voltages. The increased number of capacitors in higher levels leads to complex control method to balance the voltages of both dc-link capacitors and FCs. The higher switching frequency to keep the capacitors properly balanced and capacitors maintenance costs result in the less industrial penetration of FC type topology. [2]

The CHB multilevel inverters use series-connected H-bridge cells with an isolated DC voltage sources connected to each cell. Similarly, to have more output levels, more cells are needed. This will lead to impracticality of this type of topology since more isolated dc sources are required. [2]

Active neutral point clamped (ANPC) converter topologies combine some features of NPC and FC that provides the possibilities to take advantages of both topologies. 5L-ANPC inverter combines a 3L-ANPC leg with a 3L-FC power cell. The number of levels is increased with the levels introduced by the FC. This topology enables the modularity factor that is lacking in the NPC type inverter by adding the FC to reach higher level without adding series connected diodes. In addition, the ANPC inverters splits the dc-link into two capacitors, hence the complexity of dc-link capacitor voltages balancing is reduced compared to the conventional NPC type and FC type inverters which need four dc capacitors in series. [3]-[6]

It is observed that for the existing conventional 5L-ANPC inverter topologies, at least eight active switches are required. For better performance, theory of H bridge inverter is applied to the 5L-ANPC topology to form a novel nine-switch nine-level hybrid inverter. So as a result a Novel nine-switch nine-level hybrid inverter is proposed that combines the features of the conventional flying capacitor type, diode-clamped type converter and H bridge topology to generate multilevel voltages. circuit diagram of the hybrid

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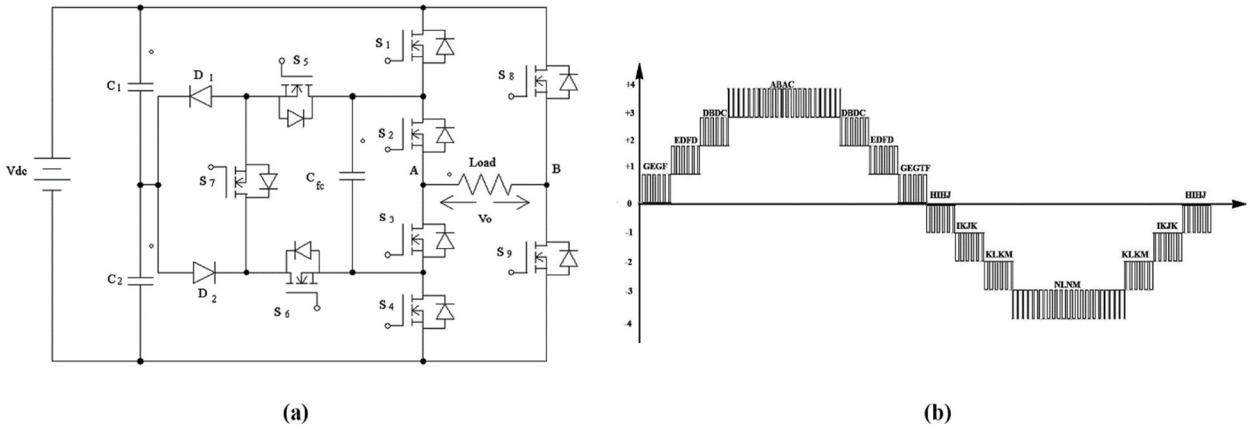
inverter is shown in fig.1 (a). In this work the operation and performance analysis of nine-switch nine-level hybrid inverter is evaluated using two control methods.

II. NINE-SWITCH NINE-LEVEL HYBRID INVERTER

First, the input dc voltage is defined as V_{dc} is divided into two equal voltages by using two dc link capacitors (C_1 and C_2) and flying capacitor C_{fc} is flying in between 0 to V_{dc} /4 voltage. So it is difficult to balance voltage across the flying capacitor, hence a robust control strategy is required for balancing the flying capacitor. Switch S_8 and S_9 performs ground altering actions. Theoretical output voltage waveforms is shown in Fig.1 (b)



(a) (b)

Fig. 1 (a) Proposed Nine-Switch Nine-Level Hybrid Inverter (b) Theoretical Output Waveform

The function of S_7 and two discrete diodes D_1 and D_2 is to provide bidirectional current paths for O to P and O to Q. Nine-switch nine-level hybrid inverter has fourteen switching states to generate nine output levels. Table. I lists all switching states and their impact on C_{FC} voltage

TABLE I
SWITCHING STATES

Switching States (Modes of Operation)	Conduction states of Active switch									Output Voltage Level	Flying capacitor (I_o >0)
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9		
A	1	1	0	0	0	1	0	0		+4	-
B					1					+3	Charge
C	1	0	1	0	0	1	0	0	1	+3	Discharge
D	0	1	0	0	0	1	0	0	1	+2	-
E	0	0	1	0	0	1	0	0	1	+1	Charge
F	0	0	1	0	1	0	1	0	1	+1	Discharge
G	0	1	0	1	1	0	1	0	1	0	-
H	0	0	1	1	1	0	1	0	1	0	-
I	1	1	0	0	0	1	0	1	0	-1	Charge
J	0	1	0	0	0	1	1	1	0	-1	Discharge
K	1	0	1	0	0	1	0	1	0	-2	-
L	0	1	0	0	1	0	1	1	0	-3	Charge
M	0	1	0	1	1	0	0	1	0	-3	Discharge
N	0	0	1	0	1	0	0	1	0	-4	-
	0	0	1	1	1	0	0	1	0		

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A. Modes of Operations

The proposed hybrid inverter generates a multilevel AC voltage which has V_{dc} /4 voltages in each level where V_{dc} is the input voltage. Input is divided into two equal voltages by using two dc link capacitors(C_1 and C_2) into V_{dc} /2 and flying capacitor C_{fc} is charged to V_{dc} /4 voltage. Operation of nine level hybrid inverter can be explained using 14 modes. Nine output voltage levels + V_{dc}, +3 V_{dc} /4, + V_{dc} /2, + V_{dc} /4, 0, − V_{dc} /4, − V_{dc} /2, −3 V_{dc} /4 and − V_{dc} (which are defined as +4, +3, +2, +1, 0, −1 , −2, −3 and −4 respectively for simplification) are obtained by summing algebraically the dc capacitor, FC voltages and by changing the references. Table I lists all fourteen switching states and their impact on FC voltage and Fig.2 shows the circuit diagram of the specific fourteen switching states and its current paths. From Table .I, it is observed that four pairs of redundant switching states (+3: B and C), (+1: E and F), (-1: I and J), (-3: I and J) have impact on FC voltage regulation. The effect of redundant switching states on the FC voltage is opposite. Therefore, the regulation of FC voltage can be achieved by proper selection of redundant switching states. Additionally, to keep FC voltage balanced, the sign of output current i_o and the actual value of FC voltage are required to decide which redundant switching state is to be selected.

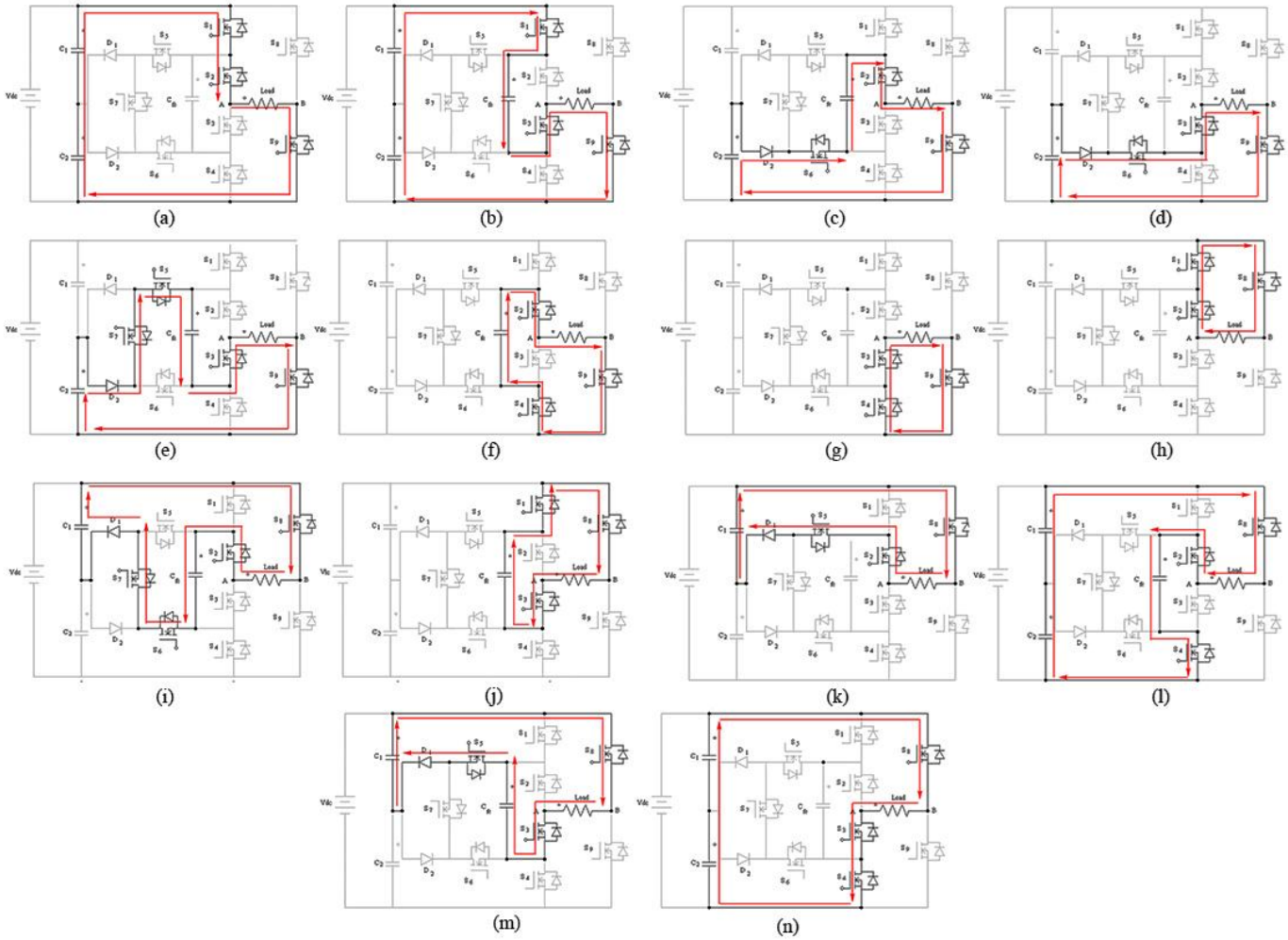

Fig. 2 Switching States (a) State A (b) State B (c) State C (d) State D (e) State E (f) State F (g) State G (h) State H (i) State I (j) State J (k) State K (l) State L
(m) State M (n) State.N

B. Design of Components

For the design of components several assumptions are made [5]. Voltage across flying capacitor is 75 V and the load is 1000W, 10 ohm. So V_{fc}=75 V, R=10Ω, fs=15 kHz.

Ripple voltage (ΔVfc)□□□□1% □of V_{fc} □□□

Flying Capacitor (C_{fc})□□□□i/(2∗ΔV∗f_s) □□□

III. CONTROL STRATEGY

To synthesize multilevel output AC voltage using different levels of DC inputs, switching in the semiconductor devices must be done in such a way that desired fundamental is obtained with minimum harmonic distortion, to attain sudden balancing of flying capacitor, good fundamental value and negligible DC value. There are different types of approaches for the selection of switching techniques for the multilevel inverters. SPWM can be differentiated in terms different modulating signals such as Sinusoidal, Rectified sinusoidal, Sampling type, Trapezoidal, Third harmonic injected type etc. and also differentiated in terms of carrier signal. Here we use Level Shifted SPWM. [8]

A. Level Shifted SPWM

The Principle of Level-Shifted SPWM technique make use of several carriers with single modulating waveform. In Phase Disposition all the carriers are in phase and the carriers are disposed so that the bands they occupy are continuous. In phase disposition method all the carriers are in phase with each other. For Phase Opposition Disposition (POD) modulation all carrier waveforms above the sinusoidal reference zero point are 180^0 out of phase with those below the zero point all the carriers have the same frequency and amplitude. This method uses eight carrier signals to generate nine level output voltage. It is based on the comparison of a sinusoidal reference waveform with vertically shifted carrier waveform as shown in fig.3. [6-7].

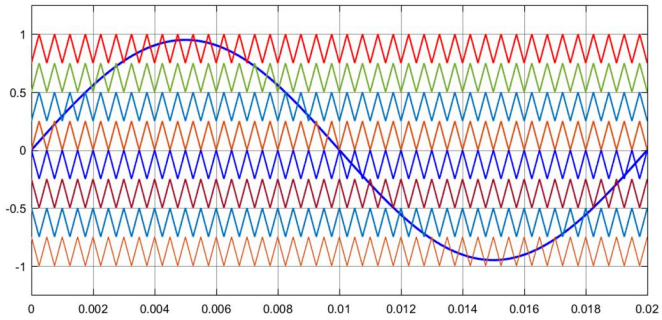

Fig. 2 Level Shifted SPWM

IV. SIMULATION STUDIES

For an output of 230V rms, 300 V input dc source, switching frequency fc as 15 kHz and reference frequency fm as 50 Hz is used. The proposed multilevel inverter was simulated in MATLAB R2017a. The DC link capacitance C1 and C2 can be determined properly considering the voltage ripple of the capacitors . Here 2000 µF is chosen for C1 and C2. By proper design 310 µF capacitor is used as flying capacitor. The smaller voltage ripple of these capacitors leads to the higher efficiency.

A. Simulink Model and Simulation Results

The detailed MATLAB/Simulink model for nine switch nine level hybrid inverter is shown in fig.4. There are nine MOSFET switches (S_1, S_2, S_3, S_4, S_5, S_6, S_7,S_8,S_9), in this S_8, S_9 are worked on power frequency 50Hz. The gate signal for the inverter switches are generated by using logical operator and repeating sequence stair block and SPWM is applied to the switches. C_1 and C_2 are the DC link capacitors and C_{fc} is the flying capacitor.

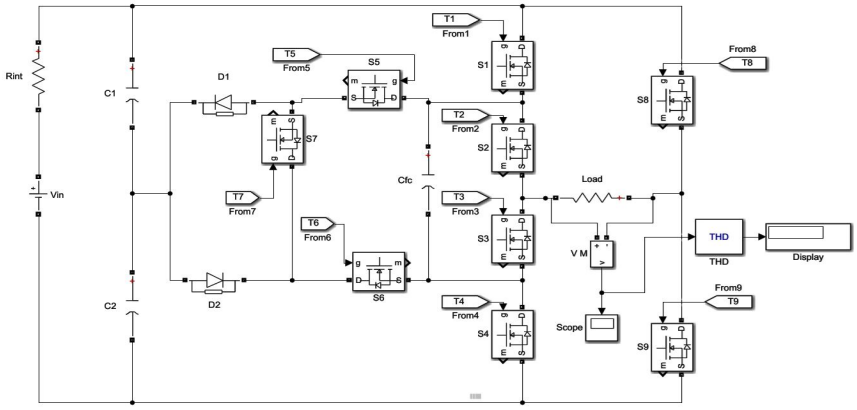

Fig. 4 Simulink Model of Nine-Switch Nine-Level Hybrid Inverter

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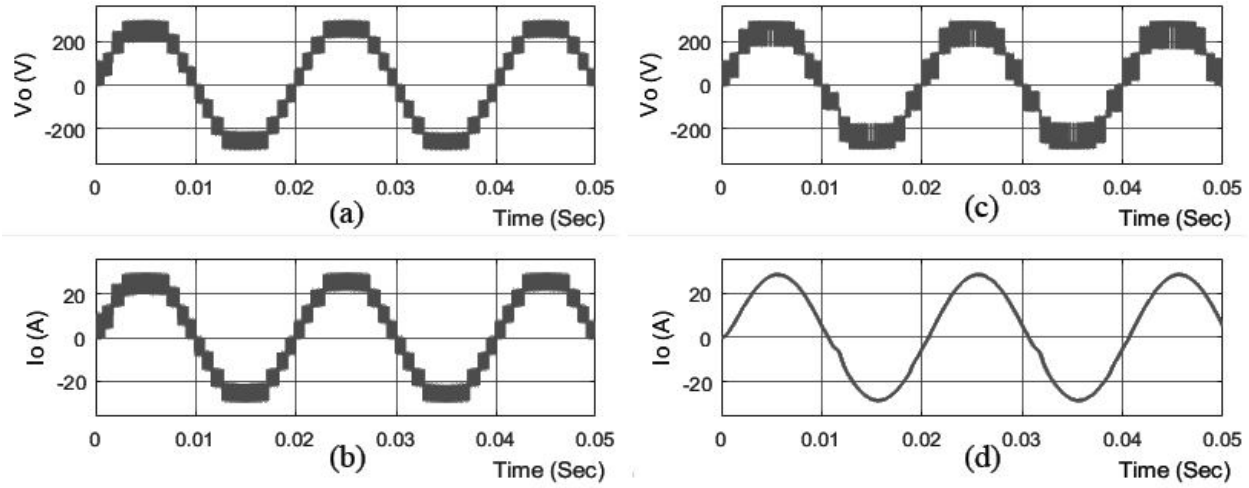

Fig. 5 Simulation Results (a) V_o (R Load) (b) I_o (R Load) (c) V_o (RL Load) (d) I_o (RL Load)

Analysing the fig.5 it is observed that there is a voltage unbalance in +3,+1, -1 and -3 levels and it is due to the flying capacitor. The voltage variation is reduced after each cycle. With RL load of power factor 0.98 (R=10 ohm, L=6.4 mH), the flying capacitor become unbalanced which results in distorted output voltage waveform, while output current waveform is smooth sinusoidal wave with THD less than 1% .

B. Simulation Analysis

By using nine level hybrid inverter with Level Shifted SPWM the obtained Total Harmonic Distortion (THD) value is 13.71 % for voltage waveform. From the analysis, the odd harmonics is more predominant especially fifth harmonics. For an input voltage of 300V here we get a fundamental of 204.87 V rms. Detailed THD Analysis for nine switch nine level hybrid inverter is shown in Table II. For these strategies the most of the harmonics are distributed in Higher order.

TABLE III
DETAILED THD ANALYSIS

Control Strategy	Level-Shifted SPWM
THD (%)	13.71
Fundamental Component (V_{RMS} (V))	204.87
DC Component (%)	0.03
2nd Harmonics (%)	0.02
3rd Harmonics (%)	0.17
4th Harmonics (%)	0.03
5th Harmonics (%)	0.05
6th Harmonics (%)	0.02
7th Harmonics (%)	0.06
Other Higher order Harmonics (%)	13.33

Efficiency curve for a nine-switch nine-level hybrid inverter is shown in fig 6 (a). for R load The load is varied from 1000 W to 4000 W, then the variation of efficiency is in between 96-98%. For RL load efficiency curve is shown in fig.6 (b). For 1000W load L is varied for pf 0.7 to upf. By varying load variation in THD is very less and it is nearly 3%.For a load condition of 2000 W the conduction loss of 48 W distribute across the devices, S_8 and S_9 has the more losses (about 8.2 W) because these switches conduct more time.

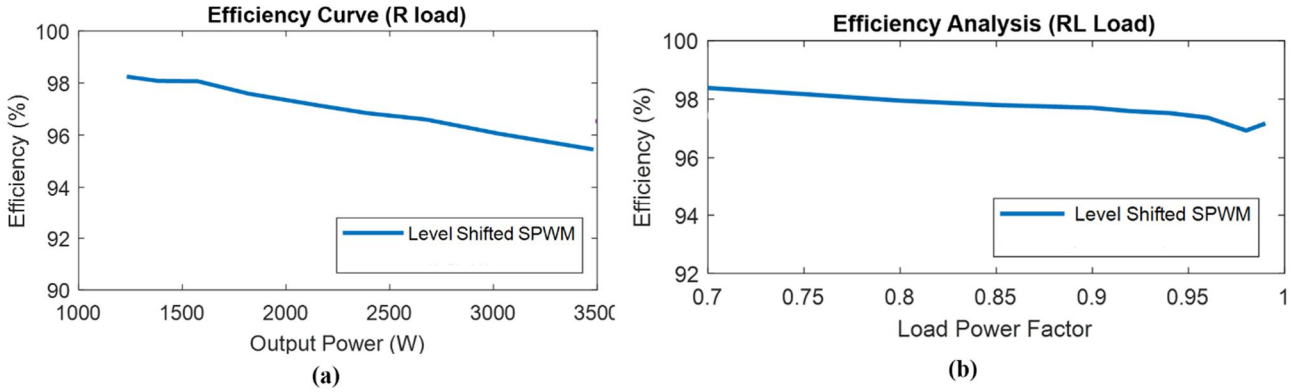

Fig. 6 (a) Efficiency Curve For R load (b) Efficiency Curve For RL load

V. HARDWARE IMPLEMENTATION

The simulation results are verified experimentally by implementing the hardware. Due to the lack of 300V power supply and other availability of devices, the hardware is done by reducing the parameters of prototype to 72 V as the input and for load of 200 ohm. The Fig 7 (a). shows the hardware setup of the hybrid inverter. Switching pulses obtained from Arduino mega 2560 micro controller is given to the driver circuit. Opto-coupler TLP250 provides the isolation between the driver and power circuits. Nine isolated supply is given to each driver circuit by using two multiple pulse 12V transformer.

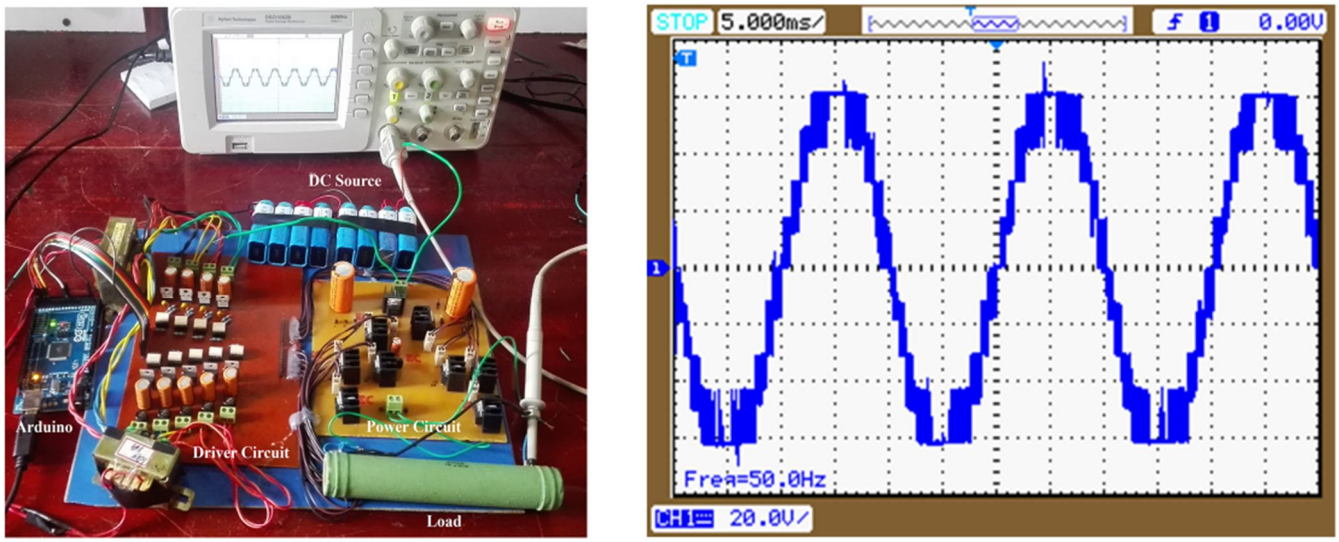

Fig. 7 (a) Experimental Setup (b) Experimental Output

From the experimental setup we can assure that the hardware setup is working and produces the desired output. Due to the voltage drop across the four switches used in the bridge converter and the diodes, maximum output voltage is less than the input. The output waveforms are shown in Fig.7 (b).

VI. CONCLUSIONS

A novel nine-switch nine-level hybrid inverter has been simulated and from its theoretical analysis, experimental result of the prototype and simulation diagrams, it is obtained that this inverter has the following advantages. High conversion efficiency, flying capacitor balances immediately, minimum THD is 13.71% by using Level Shifted SPWM, voltage utilization ratio is doubled as compared to ANPC and also the proposed inverter has the lowest components as compared to other symmetric topologies. From the simulation the max efficiency of the inverter is found to be 97.65% and it is obtained when the source voltage 300V and 2000W load. In the prototype simulation the output voltage is 72V AC, but from hardware only nearly 65V AC is found, the reduction is due to drop across the components. Efficiency and detailed THD analysis are done for R and RL load.

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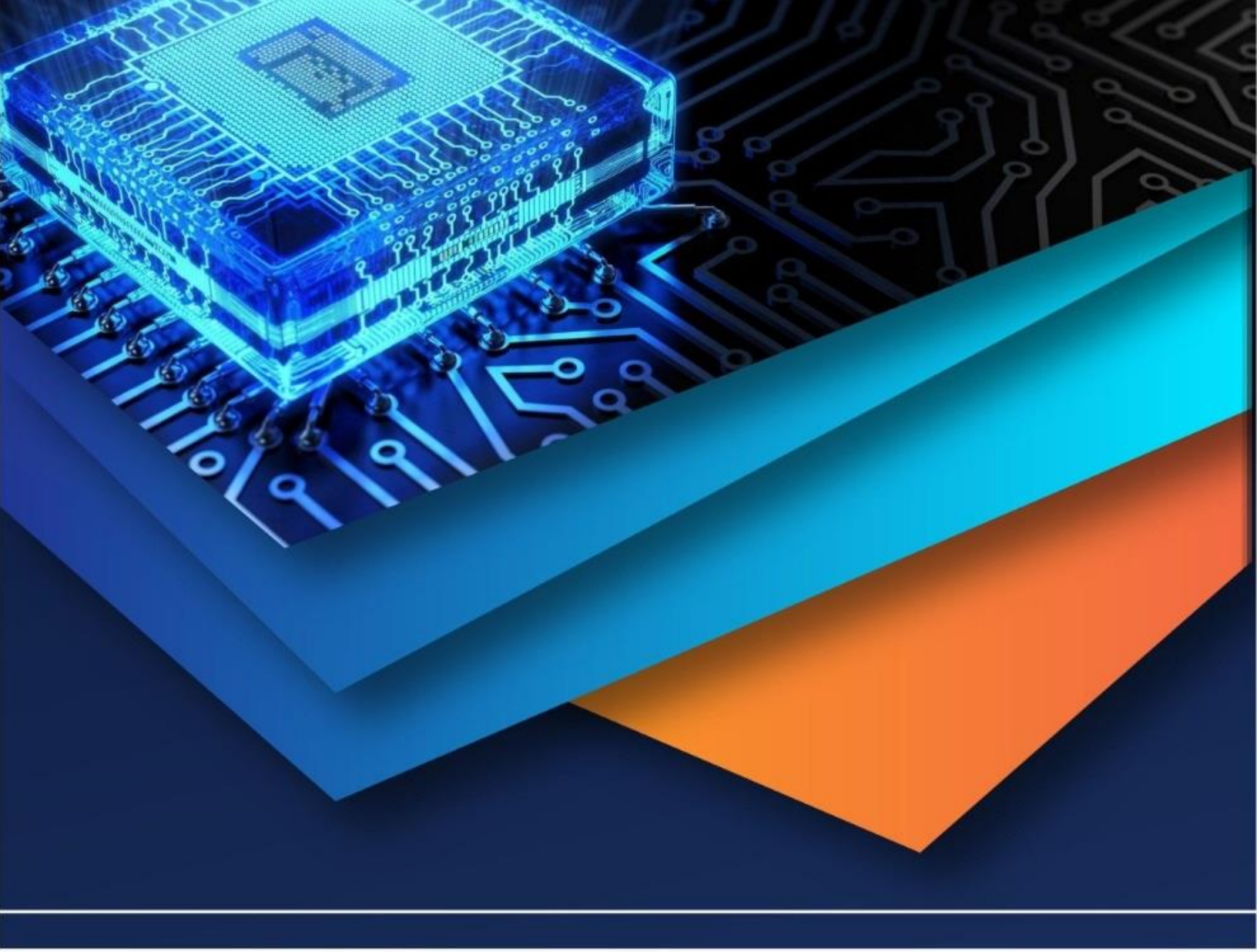

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