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Hybrid Nine Level Inverter

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Abstract: ***A nine level hybrid inverter is introduced here. It is a combination of diode clamped and H bridge topology. The power switches are gated using APOD SPWM technique at a switching frequency of 10 kHz. The number of levels can be increased by the addition of capacitors, switches and diodes. The capacitor voltage is balanced using a Resonant Switched Capacitor Converter (RSCC) circuit. The performance analysis is carried by MATLAB 2017/Simulink environment. With an input voltage of 155V DC and an output voltage of 110V RMS is obtained. The THD is found to be 13.93 %. The hardware implementation of the control strategy is done by using PIC16F877A microcontroller and Arduino MEGA 2560 microcontroller. MOSFET IRF540 is used as switching device. The prototype of the hardware is implemented for an input voltage of 36V and an output of 35.6 V, 50 Hz is obtained.***

Keywords: ***Ddiode clamped inverter, RSCC, APOD.***

I. INTRODUCTION

An inverter is defined as a device that converts direct current DC into alternating current AC. Inverters can come in many different varieties differing in price, power, efficiency and purpose. The multilevel inverter offers several advantages as compared to hard-switched two-level pulse width modulated inverters such as their capabilities to operate at high voltage with lower dv/dt per switching, high efficiency and lower electromagnetic interference. Multilevel inverter (MLI) can easily be applied for high power applications such as large motor drivers and utility supply. Owing to the recent popularity and immense industrial usage of multilevel inverters, a lot of research is going on in the field of multilevel inverter topologies. All these topologies have various applications along with their inherent limitations. The most common MLI topologies are classified into three types: Neutral Point Clamped (NPCMLI) or Diode Clamped MLI (DCMLI) [1], Flying Capacitor MLI (FCMLI), and Cascaded H-Bridge MLI (CHBMLI). Different topologies can be combined to form new topologies and can be termed as hybrid topology. Here a diode clamped topology is combined with an H bridge topology. Basic five level, seven, and nine level topologies can be derived from the new topology. Compared to basic nine level diode clamped or H bridge circuit, this circuit has less number of switches.

II. HYBRID NINE LEVEL INVERTER

Among the different multilevel topologies, a diode clamped and H bridge topology is combined to form a hybrid topology. The basic seven level topology [6] is as shown in Fig. 1.

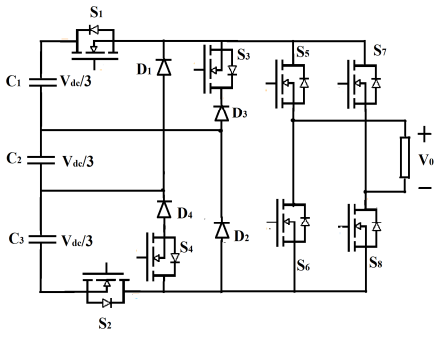

Fig. 1 Basic Seven Level Inverter

Two more switches are added to obtain a nine level inverter, which is also combination of diode clamped and H bridge multilevel inverter. Ten power switches, four DC link capacitors and six diodes are used to form the nine levels. The input DC voltage is divided among the four capacitors. Each level can be obtained by either including or excluding one or more capacitors. The H bridge circuit is used to reverse the polarity of the output voltage. In order to balance the voltage across the capacitor a voltage balancing circuit called resonant switched capacitor circuit [7] is used.

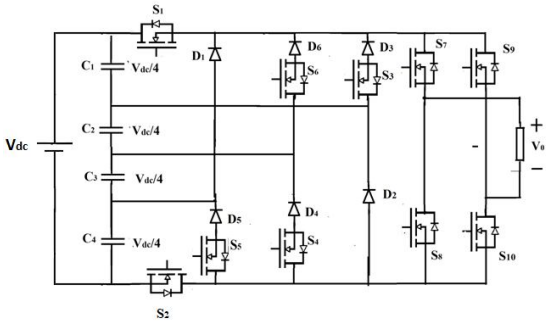

Fig. 2 Hybrid Nine Level Inverter

A. Modes of Operation

There are nine modes of operation for this inverter. The input voltage V_{dc} is divided among the four capacitors. Each level can be obtained by including or excluding capacitors using different switching combinations. In order to explain the working of the proposed inverter, it is assumed that all the switches and diodes as ideal, the input voltage splits equally among all the capacitors and the input DC voltage is ripple free. There are nine levels, four levels in positive half cycle and four levels in negative half cycle. Each voltage level is $V_{dc}/4$. To get 230 V RMS, an input voltage of 325 V DC and for 110V RMS a DC input of 155V is required. The switching states of the proposed nine level inverter are as shown in Table 1.

TABLE I

Levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
$4V_{dc}/4$	1	1	0	0	0	0	1	0	0	1
$3V_{dc}/4$	1	0	0	0	1	0	1	0	0	1
$2V_{dc}/4$	1	0	0	1	0	0	1	0	0	1
$1V_{dc}/4$	1	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	1	0	1	1
$-1V_{dc}/4$	0	1	0	0	0	0	0	1	1	0
$-2V_{dc}/4$	0	1	0	0	0	1	0	1	1	0
$-3V_{dc}/4$	0	1	1	0	0	0	0	1	1	0
$-4V_{dc}/4$	1	1	0	0	0	0	0	1	1	0

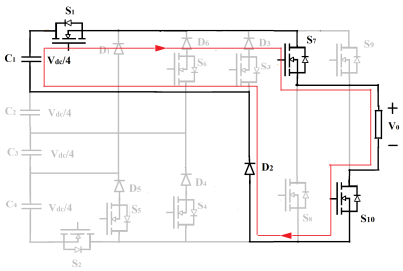

Fig. 3 Mode 1

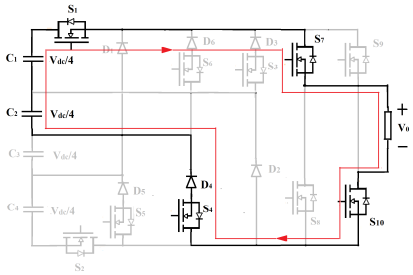

Fig. 4 Mode 2

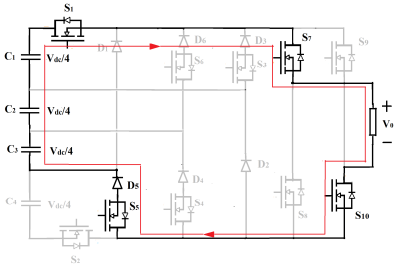

Fig. 5 Mode 3

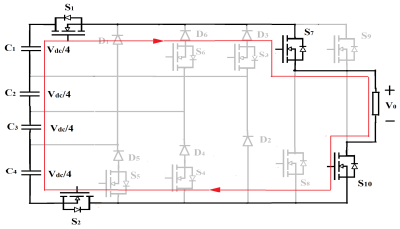

Fig. 6 Mode 4

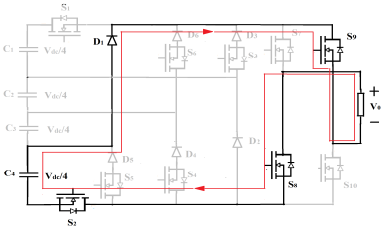

Fig. 7 Mode 5

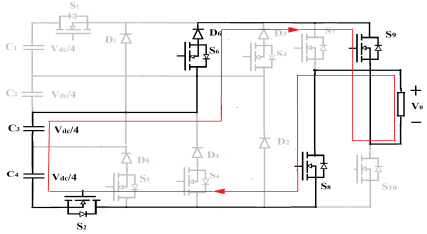

Fig. 8 Mode 6

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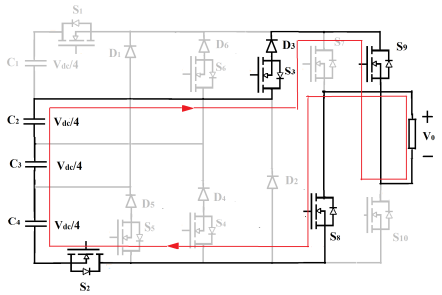
Fig. 9 Mode 7

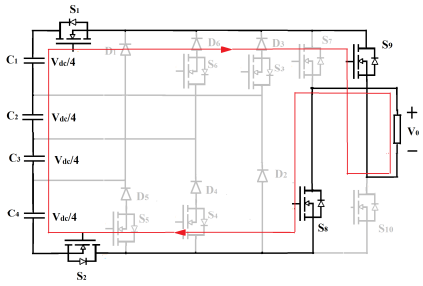
Fig. 10 Mode 8

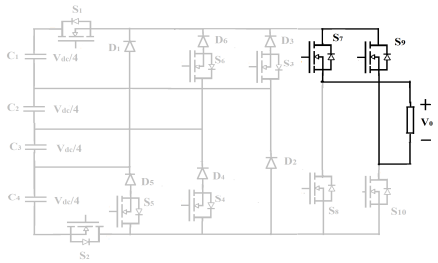
Fig. 11 Mode 9

III. CAPACITOR VOLTAGE BALANCING

An inherent problem with diode clamped multi level inverter is the unbalancing of DC link capacitors. Several methods have been adopted to eliminate the voltage unbalance. The methods are, using space vector modulation, using DC chopper circuit [5], using Redundant States and by using RSCC Circuit [7]. Here Resonant Switched Capacitor Converter (RSCC) circuit is used to balance the DC link capacitors [7]. It consists of a resonant capacitor and a resonant inductor. Transferred energy is stored in resonant capacitor C_r. The resonant inductor L_r is used to suppress the current spikes.

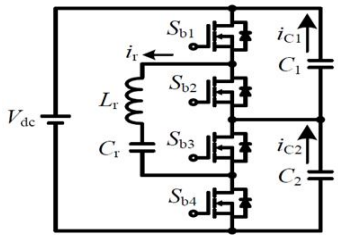

Fig. 12 Resonant Switched Converter Circuit

The circuit consists of two half-bridge inverters with four switching devices S_{b1} to S_{b4} and a series resonant circuit L_r and C_r. The DC terminals of the half-bridge inverters are connected in parallel with the DC capacitor, while an AC terminal is connected to the other one through the series resonant circuit. DC voltage source $2V_{dc}$ keeps the total capacitor voltage $V_{C1} + V_{C2}$ as $2V_{dc}$ [7]. The switching pulses to the switches in RSCC are as shown in Figure 12. The pair of switches S_{b1} and S_{b3} are turned on simultaneously and S_{b2} and S_{b4} are turned on simultaneously.

IV. CONTROL STRATEGY

The switching pulses for the inverter are obtained by Sinusoidal Pulse Width Modulation. In SPWM, the amplitude of the carrier is compared against the amplitude of the modulating signal to obtain the switching pulses. For the nine level inverter eight carriers are required. Four above the zero and four below the zero.

Among the different control methods, Alternate Phase Opposition Disposition PWM (APOD) is used. In APOD every carrier waveform is phase shifted by 180^0 from its adjacent carrier waveform. All the carrier waveforms have same frequency and same amplitude, but every carrier is phase shifted 180^0 from its neighbour carrier waveform. Odd carrier waveforms are in phase but compare to even carrier waves they are out of phase with 180^0. It also requires (m - 1) carrier waveforms for m multilevel output voltage.

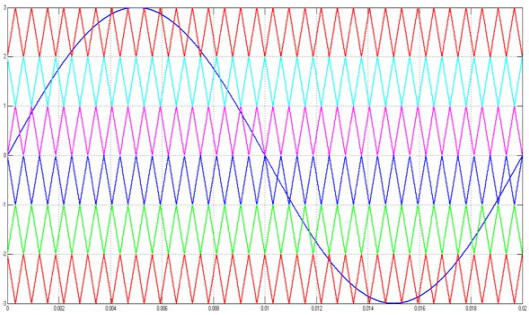
Fig. 13 APOD Carrier and modulating signal

V. SIMULATION MODEL OF HYBRID NINE LEVEL INVERTER

An input voltage of 325 V DC is given to obtain an RMS output voltage of 230 V. The of switching frequency can inuence the THD of the inverter. There is no considerable variation in THD with increasing switching frequency. So it is chosen as 10 kHz. Inorder to reduce the ripple in the output waveform DC link capacitor values are taken as 1000 micro Farad. In the RSCC circuit, increase in resonant frequency distorts the input current also higher value of capacitor causes an increased voltage spike across the RSCC capacitor. So a resonant frequency of 2 kHz and capacitance of 2.2 micro Farad is chosen. Using the values the simulation of inverter is done in Matlab.

A. Simulation Results

The simulation model of proposed nine level inverter is sim-ulated and analysed to obtain certain results. Fig. 14 and 15 shows the input and output voltages and currents of the inverter for an R load of 50 Ohm and RL load of 50 Ohm, 143 mH.

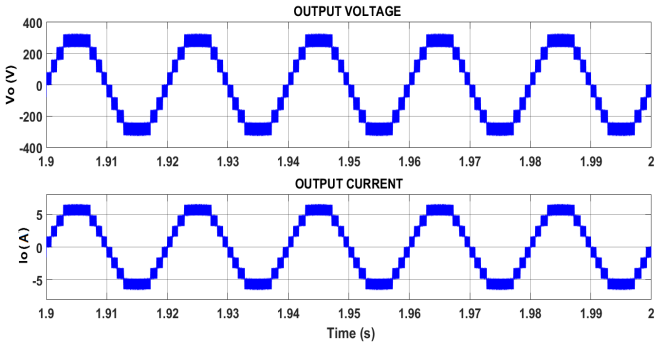

Fig. 14 Output Voltage and Output Current for R load

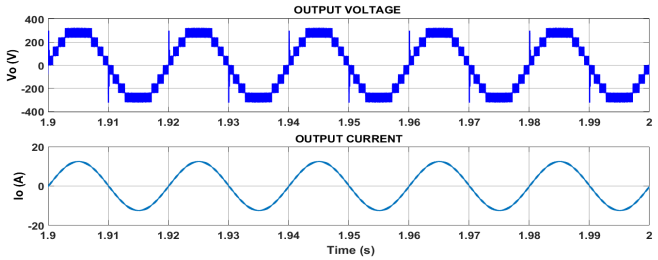

Fig. 15 Output Voltage and Output Current for R-L load

Total Harmonic Distortion (THD) signifies the degree of distortion in a waveform. More the THD more the distortion. The output of an inverter need to be sinusoidal. The variation of waveform from the sinusoidal nature is termed as THD. THD is related to certain parameters such as switching frequency, modulation methods, input voltage etc.

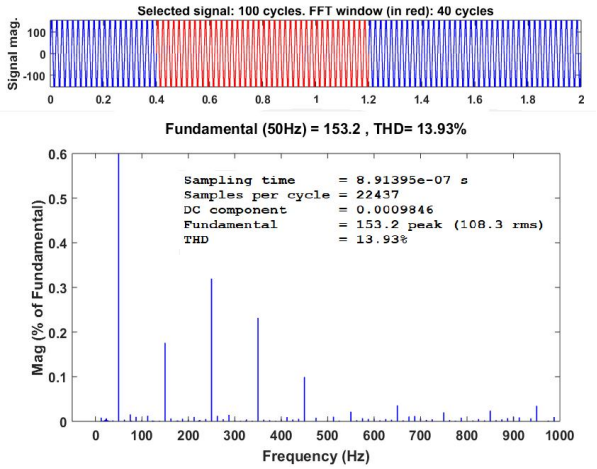

Fig. 16 FFT Analysis of nine level inverter

From FFT analysis we can infer that the THD is 13.93%. The DC component is found to be 0.0009846. Less the DC component, more the symmetry of the waveform. The following figure shows the three phase output of the proposed inverter.

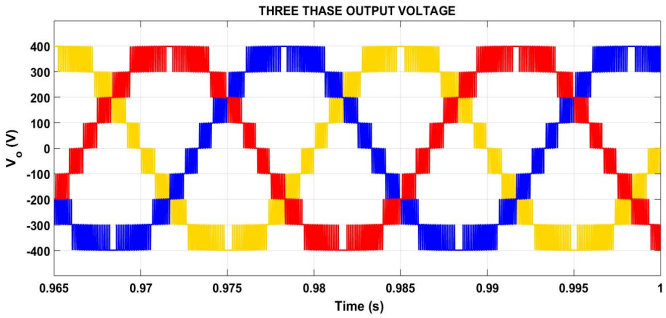

Fig. 17 Three phase output voltage

When three phase output is considered, we can use space vector modulation for control strategy. So there is no need of balancing circuit.

VI. EXPERIMENTAL SET-UP AND RESULTS

The experimental prototype of the nine level hybrid inverter is as shown below. An input voltage of 36V DC is given. The output waveform is obtained with a peak of 32V. PIC16F877A and Arduino is used to obtain switching pulses. TLP250 is used as the optocoupler for the MOSFET switches IRF540.

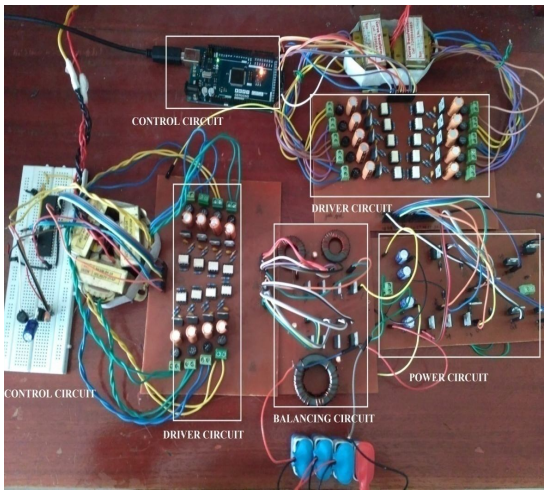

Fig. 18 Experimental set-up

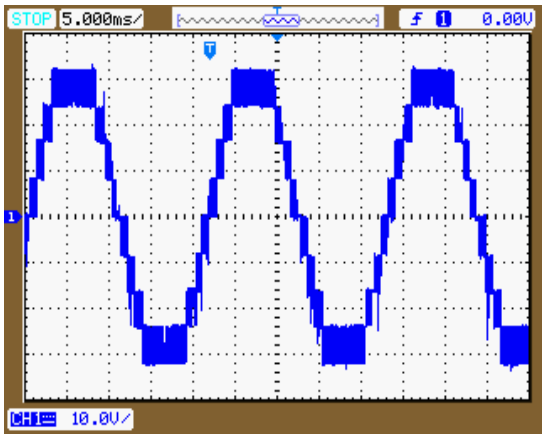

Fig. 19 Output waveform

The output voltage waveform is as shown in Fig. 19. The switching frequency used is 10kHz. The number of levels can be increased by the addition of more number of switches and diodes. However there should be a compromise between the cost and complexity of balancing circuit.

VII. CONCLUSION

A hybrid nine level inverter is introduced here. It is a combination of H bridge and diode clamped topologies. Compared to conventional H bridge and diode clamped topology, it has less number of device counts. However there is a problem of unbalancing of the DC link capacitors. The different operating modes are also discussed. The circuit is simulated in Matlab 17 software. From the performance analysis of the inverter, the efficiency of the inverter is found to be 97.6\ and the THD is 13.93 \%. The variation of THD with different control methods, modulation index, different loads etc. is analysed. THD is less for unity modulation index and unity power. Among different control methods APOD technique offers less DC component value. The switching pulses are obtained using PIC16F877A. The program for obtaining switching pulses is coded in microC software. In the experimental set up the the PCB layout of the driver as well as power circuit is drawn in Eagle software. The circuit is tested for an input voltage of 36V and output voltage waveform is obtained with peak of 32V.

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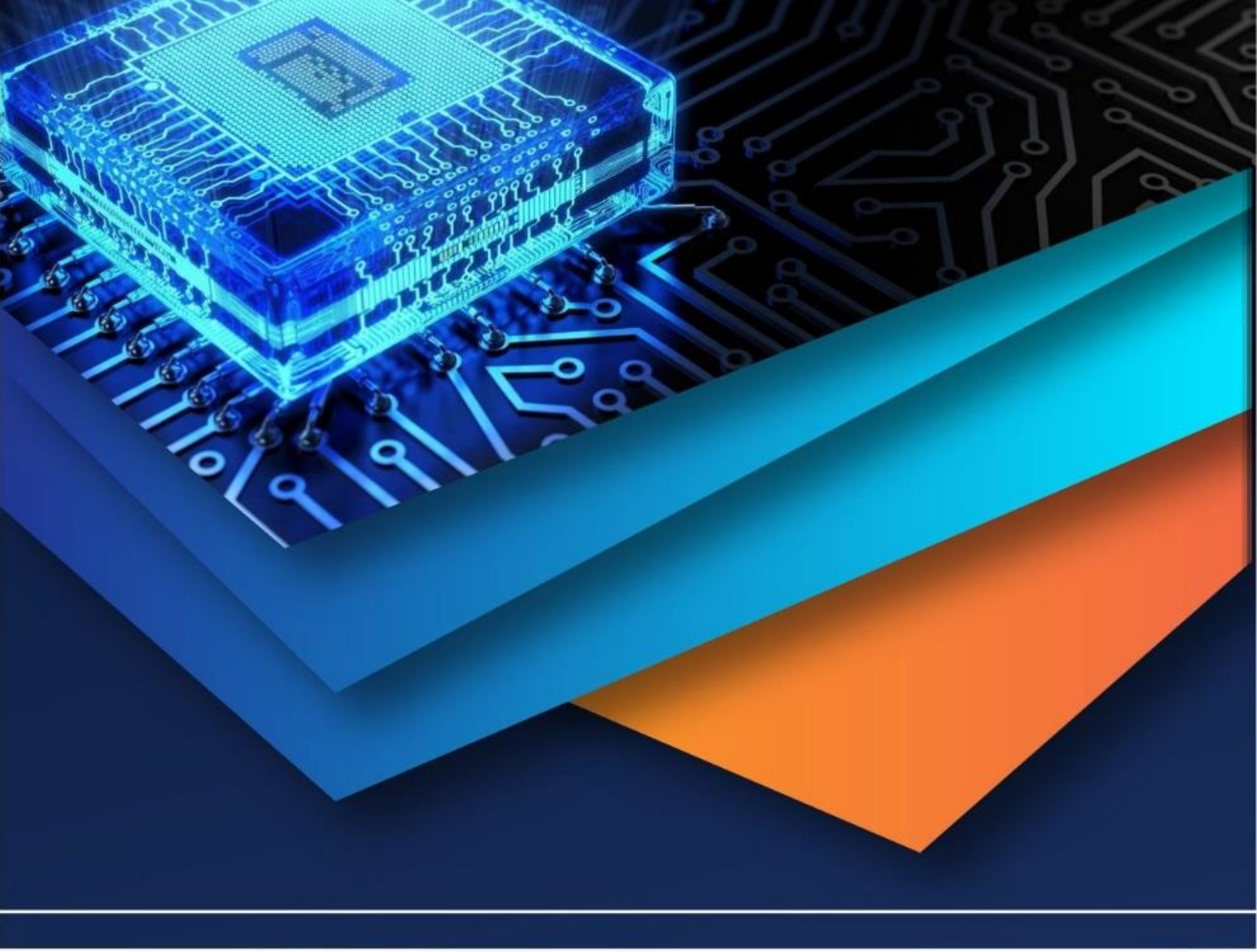

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