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VLSI Design of a Novel Architecture for Data Encoding with Golay codes

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Abstract**: There is an expanding interest for productive and dependable transmission of computerized information. A noteworthy worry here is the control of blunders for dependable generation of information. By appropriate encoding of data to a codeword with the assistance of Error Correction Codes (ECC), errors induced can be reduced. The proposed architecture parallelizes the comparison of the data and that of the parity information. To further reduce the latency and complexity, in addition, a new butterfly-formed weight accumulator (BWA) is proposed for the proficient calculation of the Hamming separation. Grounded on the BWA, the proposed design analyzes whether the approaching information coordinates the put away information if a specific number of wrong bits are amended. . The proposed engineering is actualized by utilizing xilinx14.7 form and the trial comes about demonstrate that the proposed design lessens the dormancy and the equipment multifaceted nature separately. In expansion we do Golay code for more decrease in the idleness. Golay code is a different mistake adjusting parallel code equipped for remedying a blend of three or couple of arbitrary blunders in a piece of 23 digits. The Comparison of Golay Code and BWA is due to Delay and Speed.

Keywords: Data Comparison, Hamming distance, Systematics codes, Tag matching, Error correcting codes (ECCs), Encoder, CRC, Golay code.

I. INTRODUCTION

Information examination is generally utilized as a part of processing frameworks to perform numerous activities, for example, the label coordinating in a store memory and the virtual-to-physical address interpretation in an interpretation look aside support (TLB). An interpretation look aside support (TLB) is a memory store that is utilized to diminish the time taken to get to a client memory area. It is a piece of the chip's memory-administration unit (MMU). The TLB stores the current interpretations of virtual memory to physical memory and can be called an address-interpretation reserve [1]. A TLB may dwell between the CPU and the CPU store, between CPU reserve and the fundamental memory or between the distinctive levels of the multi-level reserve [2]. The greater part of work area, workstation, and server processors incorporate at least one TLBs in the memory-administration equipment, and it is almost constantly exhibit in any processor that uses paged or divided virtual memory [3]. In view of such pervasiveness, it is critical to execute the correlation circuit with low equipment many-sided quality. Moreover, the information examination more often than not lives in the basic way of the segments that are contrived to build the framework execution, e.g., stores and TLBs, whose yields decide the stream of the succeeding tasks in a pipeline [4]. The circuit, in this way, must be intended to have as low inactivity as could reasonably be expected, or the segments will be excluded from filling in as quickening agents and the general execution of the entire framework would be seriously crumbled. As late PCs utilize blunder remedying codes (ECCs) to ensure information and enhance dependability [5]. In registering, media transmission, data hypothesis, and coding hypothesis, a blunder remedy code, once in a while mistake redressing code, (ECC) is utilized for controlling blunders in information over inconsistent or boisterous correspondence channels. The focal thought is the sender encodes the message with a repetitive as an ECC [6]. confounded interpreting system, which must go before the information examination, prolongs the basic way and fuels the multifaceted nature overhead. Accordingly, it turns out to be significantly harder to meet the above plan requirements. In spite of the requirement for complex outlines as depicted, the works that adapt to the issue are not generally known in the writing since it has been typically treated inside enterprises for their items. As of late, be that as it may, set off the fascination of an ever increasing number of considerations from the scholarly field [7]. The most recent solution for the matching problem is the direct compare method [8], which encodes the incoming data and then compares it with the retrieved data that has been encoded as well. Therefore, the method eliminates the complex decoding from the critical path.

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II. EXISTING SYSTEM

A. Decode-and-Compare Architecture

Give us a chance to consider a reserve memory where a k-bit tag is put away as a n-bit codeword subsequent to being encoded by a (n, k) code. In the unravel and-think about engineering delineated in Fig. 1(a), the n-bit recovered codeword should first be decoded to extricate the first k-bit tag. The extricated k-bit tag is then contrasted and the k-bit label field of an approaching location to decide if the labels are coordinated or not. As the recovered codeword ought to experience the decoder before being contrasted and the approaching tag, the basic way is too long to ever be utilized in a functional reserve framework intended for fast access. Since the decoder is a standout amongst the most entangled handling components, moreover, the multifaceted nature overhead isn't unimportant.

B. Encode-And-Compare Architecture

Note that translating is typically more perplexing and takes additional time than encoding as it includes a progression of mistake location or disorder count, and blunder adjustment [7]. The execution brings about help the claim. To determine the disadvantages of the unravel and-think about engineering, along these lines, the deciphering of a recovered codeword is supplanted with the encoding of an approaching tag in the encode-and-look at design More correctly, a k-bit approaching tag is first encoded to the relating n-bit codeword X and contrasted and a n-bit recovered codeword Y as appeared in Fig. 1(b). The examination is to analyze what number of bits the two code words vary, not to check if the two code words are precisely equivalent to each other. For this, we figure the Hamming separation d between the two code words and order the cases as per the scope of d. Let tmax and rmax signify the quantities of maximally correctable and discernible blunders, separately. The cases are outlined as takes after.

If d = 0, X matches Y exactly.

If $0 < d \leq$ tmax, X will match Y provided at most tmax errors in Y are corrected.

If tmax $< d \leq$ rmax, Y has detectable but uncorrectable errors. In this case, the cache may issue a system fault so as to make the central processing unit take a proper action.

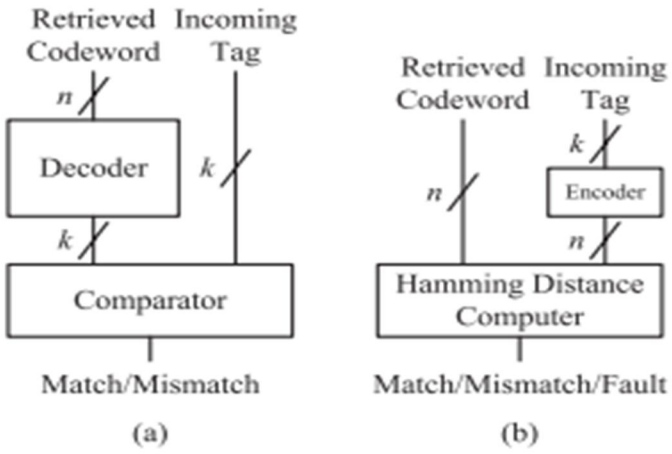

Fig. 1.(a) Decode-and-compare architecture and (b) encode-and-compare architecture.

Since the above strategy needs to process the Hamming separation, exhibited a circuit devoted for the calculation. The circuit appeared in Fig. 2 initially performs XOR activities for each match of bits in X and Y in order to create a vector speaking to the bitwise contrast of the two code words. The accompanying half adders (HAs) are utilized to include the quantity of 1's two neighboring bits in the vector. The quantities of 1's are amassed by going through the accompanying SA tree. In the SA tree, the collected esteem z is soaked to rmax + 1 in the event that it surpasses rmax. All the more accurately, given data sources x and y, z can be communicated as takes after:

$$z = \begin{cases} x + y, & \text{if } x + y \leq \text{rmax} \\ \text{rmax} + 1, & \text{otherwise.} \end{cases} \quad (1)$$

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The final accumulated value indicates the range of d. As the compulsory saturation necessitates additional logic circuitry, the complexity of a SA is higher than the conventional adder

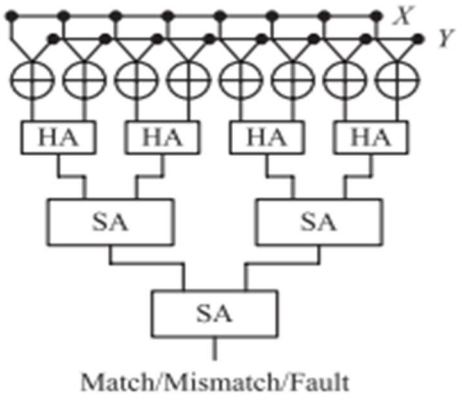

Fig. 2. SA-based architecture supporting the direct compare method.

III. BWA ARCHITECTURE

This section presents a new architecture that can reduce the latency and complexity of the data comparison by using the characteristics of systematic codes. In addition, a new processing element is presented to reduce the latency and complexity further.

A. Datapath Design for Systematic Codes

In the SA-based architecture, the comparison of two code words is invoked after the incoming tag is encoded. Therefore, the critical path consists of a series of the encoding and the n-bit comparison as shown in Fig. 3(a). However, did not consider the fact that, in practice, the ECC codeword is of a systematic form in which the data and parity parts are completely separated as shown in Fig. 4. As the data part of a systematic codeword is exactly the same as the incoming tag field, it is immediately available for comparison while the parity part becomes available only after the encoding is completed. Grounded on this fact, the comparison of the k-bit tags can be started before the remaining (n–k)-bit comparison of the parity bits. In the proposed architecture, therefore, the encoding process to generate the parity bits from the incoming tag is performed in parallel with the tag comparison, reducing the overall latency as shown in Fig. 3(b).

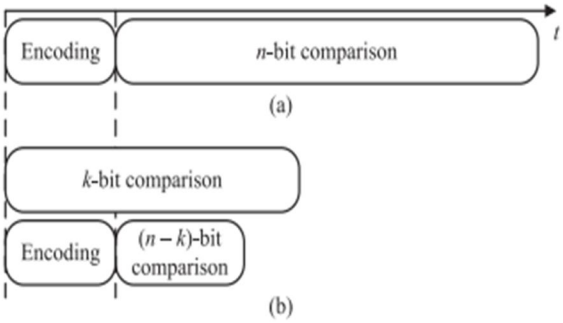

Fig. 3. Timing diagram of the tag match in (a) direct compare method
(b) proposed architecture.

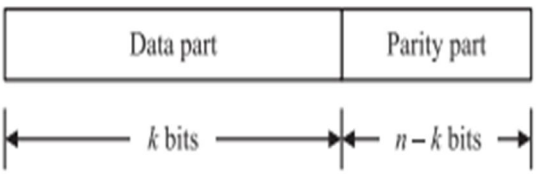

Fig. 4. Systematic representation of an ECC codeword

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B. Architecture for Computing the Hamming Distance

The proposed architecture grounded on the datapath design is shown in Fig. 5. It contains multiple butterfly-formed weight accumulators (BWAs) proposed to improve the latency and complexity of the Hamming distance computation.

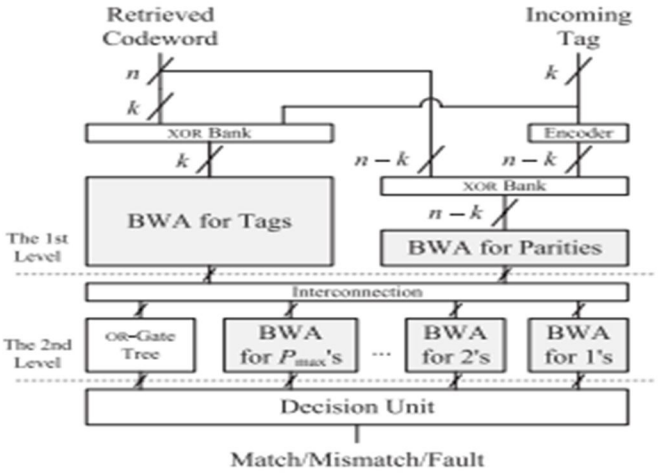

Fig. 5. BWA architecture for systematic code words

The basic limit of the BWA is to count the amount of 1's among its information bits. It contains different periods of HAs as showed up in Fig. 6(a), where each yield bit of a HA is connected with a weight. The HAs in a stage are related in a butterfly shape with a specific end goal to accumulate the pass on bits and the total bits of the upper stage freely. All things considered, the two commitments of a HA in a stage, except for the primary stage, are either pass on bits or whole bits figured in the upper stage. This affiliation methodology prompts a property that if a yield bit of a HA is set, the amount of 1's among the bits in the ways accomplishing the HA is proportional to the largeness of the yield bit. In Fig. 6(a), for example, if the pass on bit of the diminish shaded HA is set, the amount of 1's among the related data bits, i.e., A, B, C, and D, is 2. At the last period of Fig. 6(a), the amount of 1's among the data bits, d, can be found out as

$$d = 8I + 4 (J + K + M) + 2 (L + N + O) + P. \quad (2)$$

The corresponding first and second level circuits are shown in Fig. 7. Note that the encoder and XOR banks are not drawn in Fig. 7 for the sake of simplicity. Since rmax = 2, Pmax = 2 and there are only two BWAs dealing with weights 2 and 1 at the second level. As the bits of weight 4 fall in the fourth range, they are ORed. The remaining bits associated with weight 2 or 1 are connected to their corresponding BWAs. Note that the interconnection induces no hardware complexity, since it can be achieved by a bunch of hard wiring.

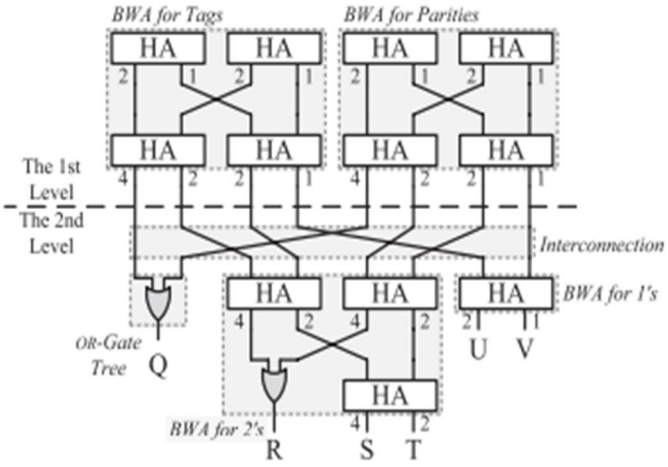

Fig. 6. First and second level circuits for a (8, 4) code.

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IV. EXTENSION

By proper encoding of information to a codeword with the help of Error Correction Codes (ECC), errors induced can be reduced [9] [10]. The (23, 12) Golay code is a multiple error correcting binary code capable of correcting an combination of three or few random errors in a block of 23 digits. For hardware implementation of encoding process, Linear Feedback Shift Register (LFSR) based cyclic redundancy check (CRC) generation method is preferred conventionally [11]. Due to drawbacks like high latency and less throughput, this technique is not a suitable solution for high-speed applications. Here, a technique based on CRC method, without using LFSR's, proposed in [12] is considered for the encoding of golay code.Golay code with minimum distance of seven is the only known multiple error correcting binary perfect code. The binary Golay code is represented as (23, 12, 7) that depicts that length of codeword is 23 bits, while message is of 12 bits and the minimum distance between two binary Golay codes is 7.This code can be in cyclic form, hence it can be decoded or encoded using its cyclic structure. The generation of coding sequence needs a generator polynomial. The possible generator polynomials over GF (2) for Golay (23, 12, 7) code are

$$G(x) = x11 + x10 + x6 + x5 + x4 + x2 + x1$$

$$G(x) = x11+x9+x7+x6+x5+x1+1.$$

Encoding can be done by eleven stages Shift Register (SR) with feedback connections according to either of the above given G*(x)*. The remainder of the long division gives the required check bits. Finally, appending the generated check bits with the message gives us the Golay codeword.

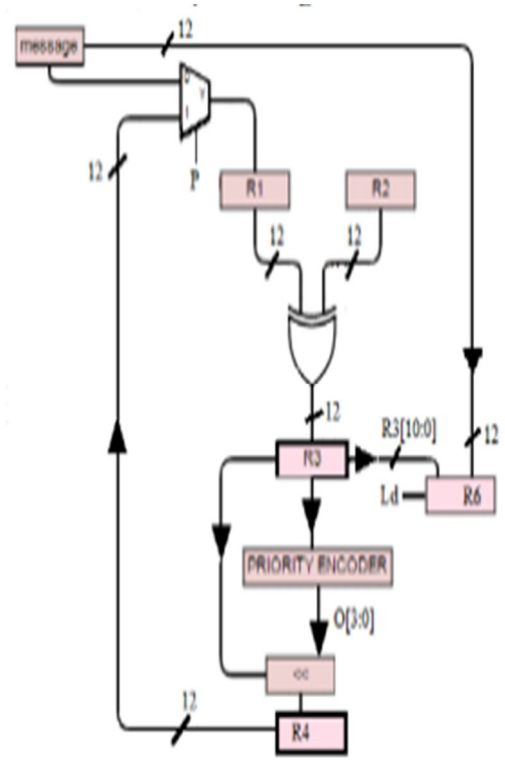

Fig.8 Architecture for generation of binary golay code

A. G23 Golay Code Generation

In each progression amid polynomial division, essentially twofold XOR activity happens for modulo-2 subtraction. The remaining outcome acquired at each progression amid the division procedure is circularly left moved by number of driving zeros present in the outcome. The leftover outcome acquired after twofold XOR activity is put away in R3 enroll. The estimation of the generator polynomial (here, 1010 1110 0011) with which the XOR activity happens is put away in the R2 enroll. A 12:4 need encoder productively distinguishes the quantity of driving zeros previously initial 1 bit in the lingering result in each progression and its yield is signified by o[3:0]. A round move enlist (<<) is utilized to move the transitional outcome by the quantity of driving zeros i.e. the yield of need encoder. The outcome acquired in the wake of moving task is put away in R4 enroll. A 2:1 multiplexer is utilized to choose either the underlying message or the circularly moved middle of the road result from the R4 enlist. The control flag utilized for the multiplexer is meant as p, which takes an esteem zero when the message comes and an esteem one after that.

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V. RESULTS

A. *Proposed*

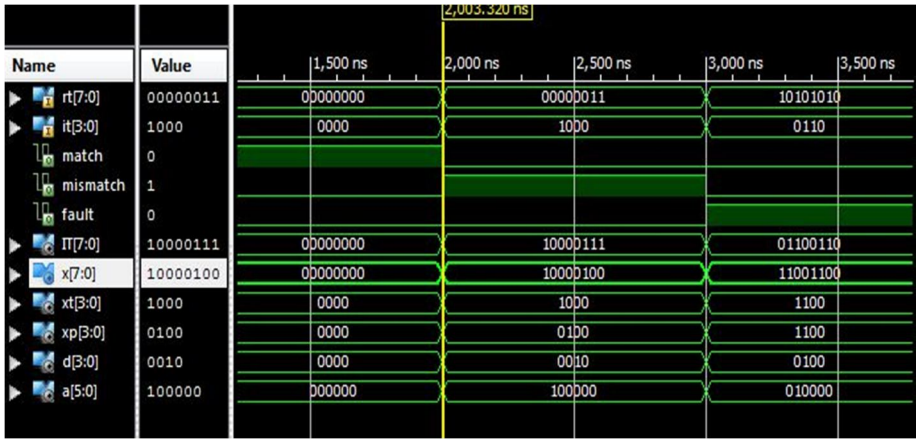

Fig. Simulation.

B. *Extension*

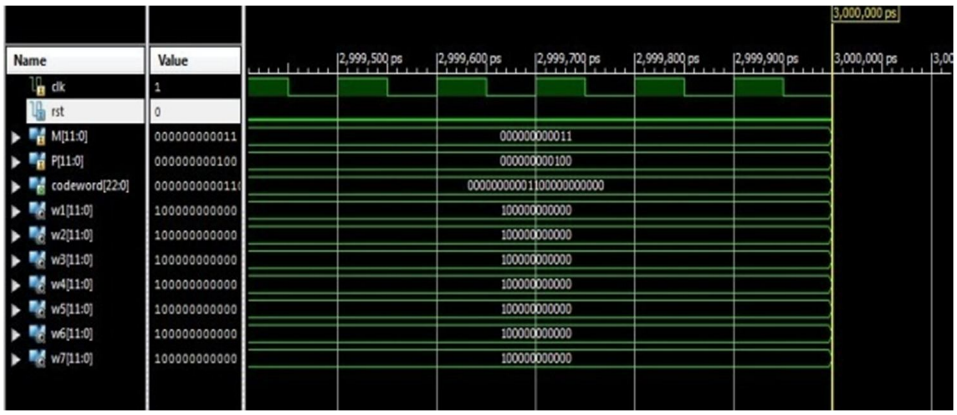

Fig. Simulation.

Comparison Table

Design	Delay(ns)
Proposed	1.899
Extension	0.284

VI. CONCLUSION

To reduce the latency and hardware complexity, another engineering has been exhibited for coordinating the information secured with an ECC. The proposed design looks at whether the approaching information coordinates the put away information if a specific number of incorrect bits are redressed. To lessen the idleness, the examination of the information is parallelized with the encoding procedure that creates the equality data. The parallel activities are empowered in view of the way that the precise codeword has isolate fields for the information and equality. What's more, a productive preparing design has been displayed to additionally limit the inertness and multifaceted nature. As the proposed design is successful in diminishing the idleness and additionally the multifaceted nature impressively, it can be viewed as a promising answer for the correlation of ECC-secured information. In expansion to diminishing idleness, Golay code is an impeccable code that can redress up to 3 blunders in a square of 24bits. Different encoder models were produced to encode. Being a cyclic code, encoders for golay code were for the most part in light of LFSR's. The applications used in digital communication systems and high speed.

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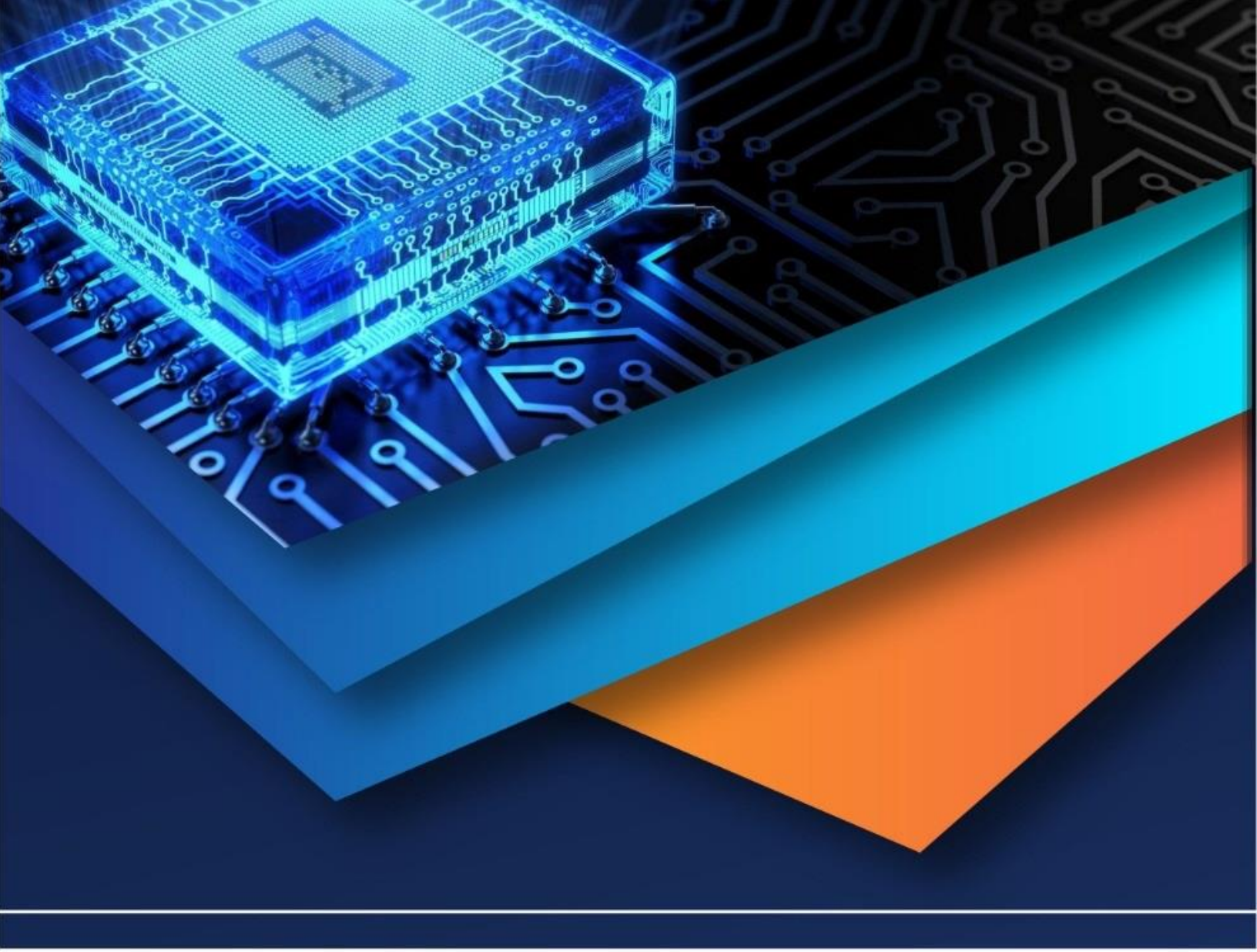

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