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# An Approach for Generating the Self-Checking Test-Bench

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***Abstract:*** ***To verify the complex functionalities for an IP core or testing of critical IP core under module level testing giving more complexity at the time of simulation to analysis the output at accurate level due this fact, the engineer takes more time to finalize the outputs at different level. Due to that, the complexity of IP core at market level gets down. Complex critical functionalities and to verify the IP core as per Do-254, in any case, confirmation of necessities by test during board testing is challenging and time-consuming in some cases like normal, boundary and robustness test benches. This paper clarifies the critical functionalities with one of technique i.e. self checking test bench, and gives proposals how to beat them. The efficiency of the self-checking test bench is demonstrated with FIFO as case study.***

***Keywords: DO-254, FPGA, Assertion, FIFO, Coverage***

## I. INTRODUCTION

Do-254/ED-80 is a method for consistence to flight directions for all aeronautical electronic equipment named custom small scale coded devices for example FPGA, ASICs and PLDs, these devices are frequently as unpredictable as programming controlled microchip based frameworks along these lines they require a stringent improvement way to deal with fulfil airworthiness necessities. The principle motivation behind the direction is to guarantee that the device assembled meets the necessities and securely plays out all proposed works under typical and unusual working conditions [1]. Keeping in mind the end goal to get consistence the candidate must actualize the stringent advancement and check procedure of do-254 and fulfill the fundamental goals at the target level. The structure of hardware design life cycle and the information created in the process are for and particular to the device itself.

To verify the design under test (DUT) as per DO-254 consistently is basic in demonstrating that the device meets the necessities. In any mode of testing for device at target level (normal, boundary, and robustness test cases) is very crucial role to confirming the particular pre-requisites for a prohibitive action take place. This document encloses the purposes for these difficulties are examined and proposals how to defeat them are given. The methodology for testing the FPGA objectives at target level to be accurate, it should be done with one of the technique like self checking test bench [2].

## II. THE CHALLENGE

The standard way to deal with check electronic segments and guarantee legitimate practical conduct is to utilize simulation tool. The check/verify is then in view of timing models of the constitutive components of a FPGA. The device may be demonstrated to meet the do-254 level A desires. Implementation in FPGA using self checking test bench for accuracy needs to satisfy the customer needs as well to increase the percentage of FPGA safety critical design [6].

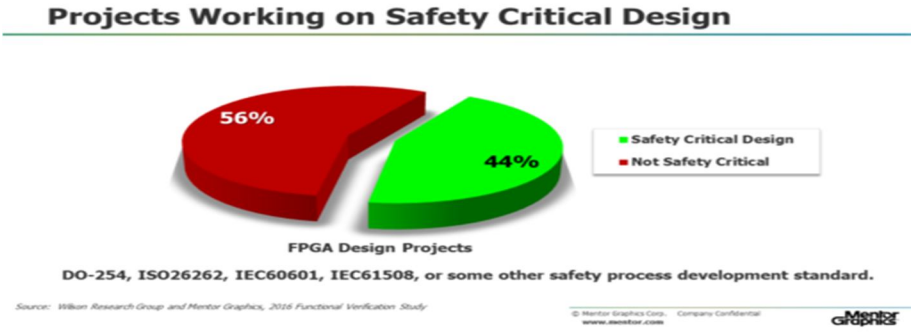


Fig. 1. Percentage degradation for Avionics critical system as per DO-254[7]

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## III. CHECKING/VERIFICATION PROCESS

The confirmation steps are indispensable and a key component to demonstrating that the device fabricated meets the requirement functionality. The confirmation procedure gives a specialized evaluation of rightness of the plan against the necessities. The key factor in planning an effective confirmation design/verification design is to comprehend the reason destinations and exercises of the confirmation steps as characterized in the direction

The logic for checking the procedure for confirming that device should map the pre-requisites. The design under target level of testing should convince the applicant with that must fulfil the necessities. The confirmation/verification exercise with the combination of audits, examinations and tests as prescribed by the applicant in the confirmation of design and it should be follow during all periods of life cycle of hardware.

Validation and Verification Process ensures that test cases, methods, procedures, pass/fail criteria and results/coverage are reviewed to determine whether the developed test cases, methods, procedures, pass/fail criteria satisfy the objectives of RTCA/DO254[8].

Verification of the implementation is the verification (e.g. post layout simulations) of the Detailed Design after place and route and of the device itself.

### *A. Review and analysis*

The entry criteria to perform the review of test cases, methods, procedures, pass/fail criteria and results/coverage are release of initial version of those data items and other supporting hardware verification data will be under configuration control as appropriate. Designers will perform the review of these test cases, methods, procedures & pass/fail criteria and provide the feedback to the testing team [10].

The verification on device level, to assess unacceptable robustness defects through RBT (requirement based testing) to cover the normal and abnormal input conditions and operating conditions. This document will be prepared to justify for level of implementation (RTL, post layout, physical device, board level) and the type of the planned verification activities (test, simulation, analysis, inspection etc.,)using self checking test bench as to improve the performance of the design.

At the post-design level of confirmation for the HDL level verification which is done by means of HDL coding standard (HCS) which potentially records the dynamic timing simulation (DTS) and static timing simulation (STS) and essential examination which can be investigate with code coverage under design level test or the verification of design under test inside the element is done by means of device testing. Remember that all design or elements are required to confirm all FPGA necessities by test which is the genuine trail for the applicant [11].

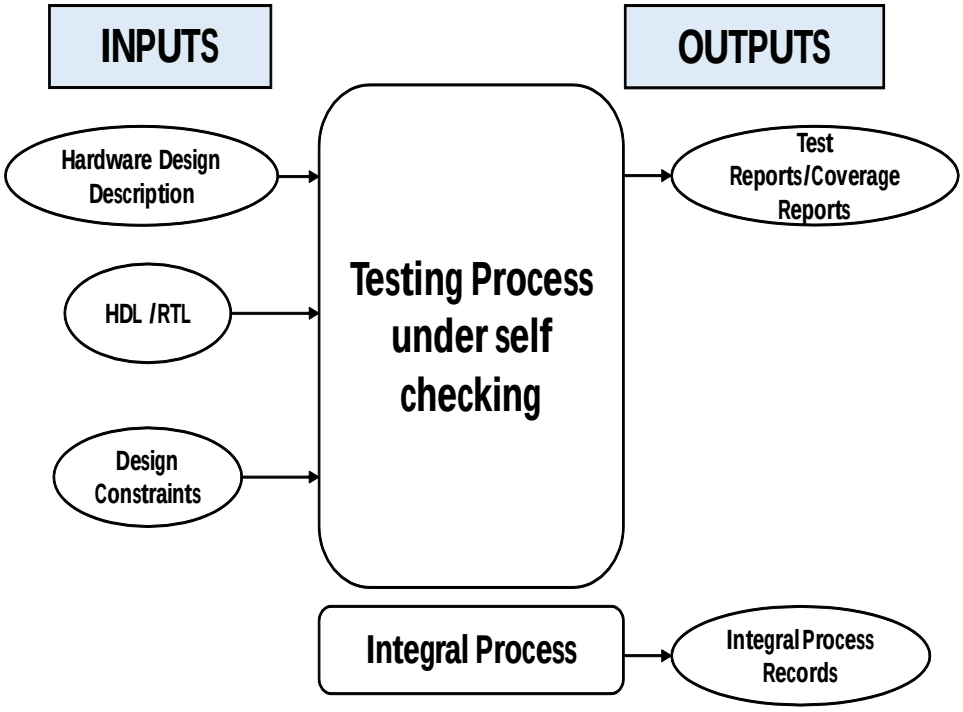


Fig. 2. Flow of testing process under self checking [12]

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As per DO-254, it guides the particular idea to complete the entire design which encloses the requirement to DUT level of testing, considering all modes of scenario test cases. To achieve pass scenario at module and integration level of testing should verify with the expected outputs via code coverage analysis.

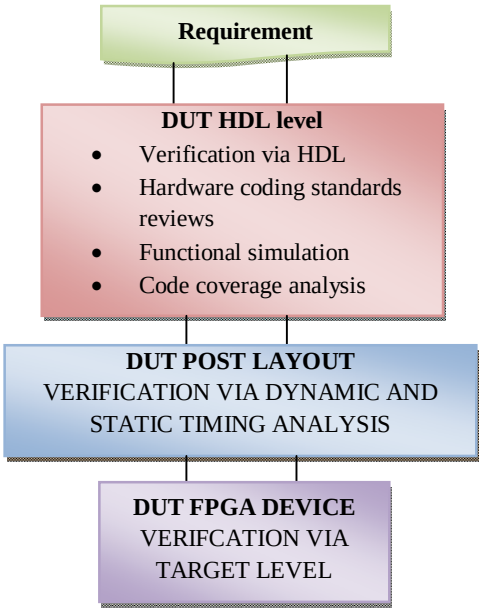


Fig. 3. Flow of Verification of Design And Implementation [13]

*B. Developing Acceptance Coverage by Test*

The following is an overall of outline comments/suggestion that can be executed to expand check by test. The outline of suggestions proposes an approach that can use a similar experiments and test contributions for recreation and target testing considering a substantially more grounded contention of check integrity and legitimacy to the affirmation expert.

*1)* Compose the prerequisites with the end goal that they are obvious at the FPGA stick level. This guarantees the inputs are controllable and the outputs are detectable with the goal that every necessity can be checked by test at the stick level.

*2)* Make test cases should follow the prerequisites, not the design. Experiments portray how to confirm the necessities.

*3)* Make the HDL test bench to actualize the experiments for recreation. The contributions from the test case are connected to the HDL plan and outputs are gathered by means of waveforms. Self-checking test benches can likewise be utilized to computerize checking for PASS/FAIL comes about.

*4)* The test bench can be utilized for utilitarian recreation and code scope examination. A similar test vectors are utilized for useful reproduction, utilitarian re-enactment with scope measurements, post-design timing reproduction and for device testing [14]

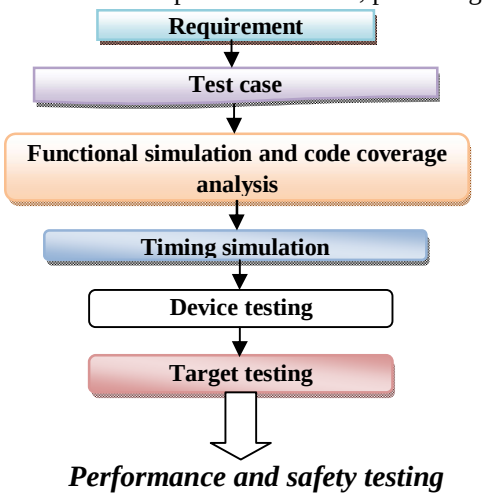


Fig. 3. Flow of FPGA design safety critical [15]

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As a FPGA developer, your life is fundamentally one huge investigates cycle. From the minute you get almost priority from marketing, until creation silicon is prepared, you are searching for issues. When you perceive an issue, at that point remedial activity must be recognized.

*a)* Create an empty test bench

```
entity tb_adder_comb is
.....
end tb_adder_comb;
```

*b)* Add an architecture

```
[header files]
entity tb_adder_comb is
.....
end tb_adder_comb;
architecture test of tb_adder_comb is
begin
end architecture test;
```

*c)* Instantiate the design/unit under test (DUT/UUT)

```
Entity tb_adder_comb is
generic(
N_BITS: positive range 2 to positive'right
);
port (op1:.....N-bit input;
op2:.....N-bit input;
sum:.....(N+1)-bit output
);
```

*d)* The test bench is updated as

```
-create a constant for every generic parameter in the DUT/Uut and assign a value.
-create a signal for every port that is input abd output port
--generics
constant N-bits:positive range 2 to positive'right:=4
--ports
--inputs
signal op1:.....;
signal op2:.....;
--outputs
signal sum:.....;
-- instantiate the DUT
DUT: entity work.adder_comb
generic map(N_BITS=>N_BITS)
port map (OP1=>OP1,
OP2=>OP2,
SUM=>SUM);
```

*e)* Input feeding

```
--inputs from vector1(op1,op2)
--outputs from vector1(sum)
--inputs from vector2(op1,op2)
--outputs from vectors2(sum)
constant time_delta time:=100ns;
--generic
--ports
-- instantiate the DUT
```

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```
--test_adder_comb
simulation:process
begin
--current values
op1<=”000”;--1
op2<=”0101”;--5
wait for time delta;
end process simulation;
end architecture;
```

*f)* To prevent duplication of the code we add a procedure

```
procedure check_add
(constant in 1:in natural;
constant in 2: in natural)is
begin
--current values
op1<= std_logic_vector(to_unsigned(in1,op1’length));
op2<=std_logic_vector(to_unsigned(in1,op2’length));
wait for time delta;
end process;
```

*g)* The self checking test bench has two main parts;

-a report statement and string describing the error using and assert statement.

-a severity statement describing the level of the issue that is note,warning, error or failure.

```
Procedure check_add
(constant in 1: in natural;
constant in 2: in natural;
constant res_expected:in natural:in natural)is
variable res:natural;
begin
--current values
op1<=std_logic_vector(to_unsigned(in1,op1’length));
op2<=std_logic_vector(to_unsigned(in1,op2’length));
wait for time delta;
res:=to_integer(unsigned(sum));
assert res=res_expected;
report”unexpected results.’&”op1=”&integer’_image(in1)&”,”&
.
.
.(repeat for all the other ports)
severity error
end procedure check_add
begin
check_add(12,8,20)--will show a sucess full result
check_add(12,8,21)—will show a failure
.
.
wait
--end process;
--end architecture
```

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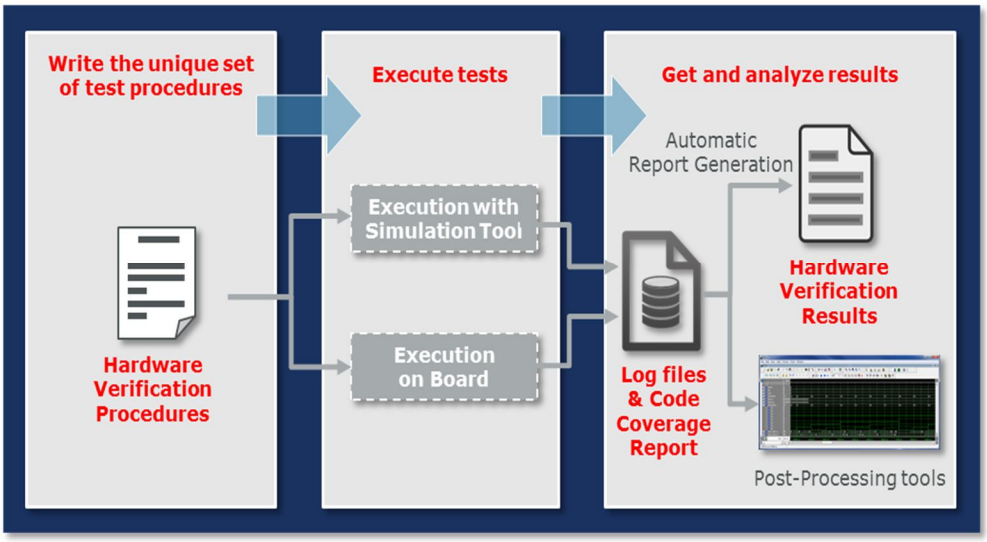


Fig. 4. Procedure of Self-Checking Test-bench [17]

Self-checking test bench (SCTB) has three primary records: the first HDL demonstrates the last gate level demonstrates and a reciprocity block. The test bench (TB) works by contrasting the outcomes from the two FPGA models which both get a similar input i/p stimulus and after that errors any disparities that are found. The genuine power in this strategy is that when a mistake is discovered you can test into the two models and follow signs to perceive what is causing the issue [17]

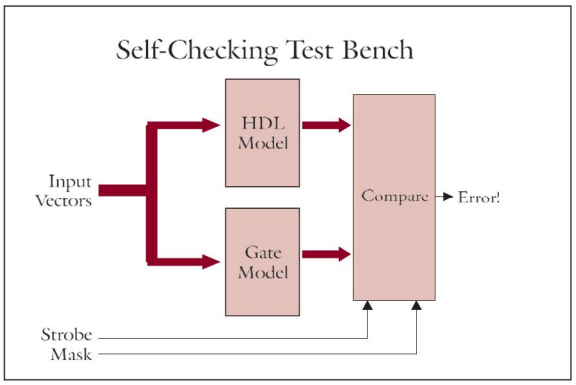


Fig. 5. Structure of Self Checking Test bench [17]

*C. Trace Data Activities in Detailed Design & Implementation Process*

*1)* Link the specific lines of the HDL design source (single line or multiple lines of code) to the related FPGA requirement it covers.

*2)* Generate a downstream traceability to ensure that each FPGA requirement is fully implemented by an HDL function. FPGA designers must create additional functions as needed to fully implement each FPGA requirement.

*3)* Generate an upstream traceability to expose unused HDL design functions. Unused functions of the HDL code may lead to unexpected behavior of the device, and must be removed or updated.

*4)* Ensure that the post-synthesis and post-layout design meet the specified constraints.

*5)* Baseline or record the trace data between FPGA requirements and HDL design data.

*D. Trace Data Activities in Verification process*

*1)* Link each verification test scenario to the related FPGA requirement it covers. Test scenarios are created based on the FPGA requirements, and they are reviewed for suitability and completeness to cover the related FPGA requirement. Test scenarios define how each FPGA requirement will be verified, and includes the appropriate input conditions, test sequence and expected results.

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*2)* Generate a downstream traceability to ensure each FPGA requirement is covered by a test scenario.
*3)* Generate an upstream traceability to expose unnecessary test scenarios.
*4)* Baseline or record the trace data between FPGA requirements and test scenarios.
*5)* Link the specific lines of the test bench (single line or multiple lines of code) to the related test scenario it covers.
*6)* Generate a downstream traceability to ensure that each test scenario is fully implemented by the test bench. Verification engineers must create the test bench with the appropriate test inputs, sequence and expected results as defined in the test scenarios.
*7)* Generate an upstream traceability to expose unused functions or code of the test bench that needs to be removed or updated.
*8)* Baseline or record the trace data between test scenarios and test bench.
*9)* Link the specific simulation results to the related test scenario it covers. Simulation results are a combination of simulation logs, waveforms and coverage data. These results are analyzed and reviewed for correctness.

High level of verification like self-checking test bench is an awesome method for playing out that last check organizes previously making silicon. It gives you the additional certainty that the design will be right and easily roll into generation. Coverage is observed through various methodologies. Code scope and functional scope are utilized as correlative strategies together. also assertion/comparison based scope is a reasonable technique to implement and verify the critical design behaviour.

## IV. CASE STUDY- FIFO

For safety and performance criteria of self checking test bench, hereby to implement and verify a module like FIFO using self checking approach, for better time to market and customer supports. The process needs to proceed the module level testing like FIFO which is need to test the functionality of that particular module which tells input and output behavioural, according to that need to verify the self checking methodology.
The self checking methodology can be placed to normal, boundary and robustness test cases which include:

*A.* Performance
*B.* Safety analysis
*C.* Low latency
*D.* Analysis of Clock Skew, drift factor

*E. Functionality Description*

*1)* Data FIFO block shall be used for storing the user defined data of particular input source
*2)* There shall be a 32 bit data bus to write the user defined data
*3)* Data FIFO block shall an i/p AXI-clock for its internal operation
*4)* Data FIFO shall have a width of 32-bit
*5)* FIFO depth in this block using 16000 words
*6)* There shall be a tvalid input signal to data FIFO, to indicate the valid user defined data
*7)* There shall be a tlast input signal to data FIFO, to indicate the last word (32 bit) of user defined data
*8)* There shall be a tready o/p signal from the data FIFO.

Note 1: t ready set to high shall indicate, FIFO is ready for receiving AXI stream data of 32 bit.
Note 2: t ready set to low shall indicate, FIFO is not ready for receiving AXI stream data.
Below table indicates the following requirement analysis for FIFO as per DO-254

TABLE 1 REQUIREMENT ANALYSIS

| Requirement Identification | Interface Name | Width (in bits) |
|---|---|---|
| XXXXXXXX | FIFO module shall be interfaced with following port for reading from buffer: | |
| | RdClk_i | 1 |
| | rd_en_i | 1 |
| | rd_data_o | 32 |

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| | |
|---|---|
| XXXXXXXX | FIFO module shall be interfaced with following port for writing from buffer: |

| | |
|---|---|
| WrClk_i | 1 |
| Wr_en_i | 1 |
| Wr_data_o | 32 |

## V. RESULTS

Step1: Firstly generation of the RTL for the function of the module

Step2: Secondly, feed the input values in HEX values in stimulus as FILE i/o assertion based testing

file vector_file:text open read_mode is "XXXXXXXXXX";--reading the expected results from read text file

file result_file:text open write_mode is " XXXXXXXXXX ";--writing the compared results in the write text file

--variables Declaration

variable file_line: line;

variable str_stim_in :string(32 downto 1);

variable stim_in :std_logic_vector(31 downto 0);

variable x : std_logic_vector(31 downto 0);

variable y :integer;

variable result_line:line;

variable i :integer :=0;

Step3: Thirdly, as per feeding the input values check the expected values as per feed values which gives the accuracy as per design and engineer will satisfy the requirement given by the organisation. This step tells about the simulation results is PASS/FAIL condition as per analysis.

Step4: Finally as per simulation based testing or assertion included testing which shows PASS/FAIL condition, the engineer or designer come to know the timing analysis of the design for accuracy which gives performance and safety analysis.

### *A. Expected inputs/ feed values*

```
00000000000000000000000000001001
00000000000000000000000000001010
00000000000000000000000000001011
00000000000000000000000000001100
00000000000000000000000000001101
00000000000000000000000000001110
00000000000000000000000000001111
00000000000000000000000000010000
00000000000000000000000000010001
00000000000000000000000000010010
00000000000000000000000000010011
00000000000000000000000000010100
00000000000000000000000000010101
00000000000000000000000000010110
00000000000000000000000000010111
00000000000000000000000000011000
00000000000000000000000000011001
00000000000000000000000000011010
00000000000000000000000000011011
00000000000000000000000000011100
00000000000000000000000000011101
00000000000000000000000000011110
00000000000000000000000000011111
00000000000000000000000000100000
00000000000000000000000000100001
00000000000000000000000000100010
00000000000000000000000000100011
00000000000000000000000000100100
00000000000000000000000000100101
00000000000000000000000000100110
00000000000000000000000000100111
00000000000000000000000000101000
00000000000000000000000000101001
00000000000000000000000000101010
```

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*B. Expected outputs in Simulation Based Testing*

```
test bench
67275000 ps time is:67281250 ps, the output case2 is test case failed, not correct match:= 1
 expected value is 00000000000000000000000000000001 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67281250 ps time is:67293750 ps, the output case2 is test case failed, not correct match:= 2
 expected value is 00000000000000000000000000000001 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67293750 ps time is:67306250 ps, the output case2 is test case failed, not correct match:= 3
 expected value is 00000000000000000000000000000010 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67306250 ps time is:67318750 ps, the output case2 is test case failed, not correct match:= 4
 expected value is 00000000000000000000000000000011 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67318750 ps time is:67331250 ps, the output case2 is test case failed, not correct match:= 5
expected value is 00000000000000000000000000000100 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67331250 ps time is:67343750 ps, the output case2 is test case failed, not correct match:= 6
expected value is 00000000000000000000000000000101 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67343750 ps time is:67356250 ps, the output case2 is test case failed, not correct match:= 7
 expected value is 00000000000000000000000000000110 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67356250 ps time is:67368750 ps, the output case2 is test case failed, not correct match:= 8
 expected value is 00000000000000000000000000000111 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67368750 ps time is:67381250 ps, the output case2 is test case failed, not correct match:= 9
 expected value is 00000000000000000000000000001000 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67381250 ps time is:67393750 ps, the output case2 is test case failed, not correct match:= 10
expected value is 00000000000000000000000000001001 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
67393750 ps time is:67406250 ps, the output case2 is test case failed, not correct match:= 11
expected value is 00000000000000000000000000001010 but its current simulation value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 *************** &&&&&&& ********
```

The below results or cases shows the expected i/o values with cases when feed in to stimulus

Case1: When assertion based testing feed in to stimulus input using FILE i/p

# ** Note: Port mapped signal Areset_i is matched
    #  Time: 5 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal wr_en_i is matched
#  Time: 5 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal full_o is matched
#  Time: 5 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal RdClk_i is matched
#  Time: 5 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal rd_en_i is matched
#  Time: 5 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal wr_data_i is matched  and the value is 00000000000000000000000000001010
#  Time: 5 ns  Iteration: 1  Instance:
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#  Time: 5 ns  Iteration: 1  Instance: /vdb_n
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
#  Time: 5 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal rd_data_o is matched  and the value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
#  Time: 5 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal WrClk_i is matched
#  Time: 5 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal Areset_i is matched
#  Time: 15 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal wr_en_i is matched
#  Time: 15 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal full_o is matched
#  Time: 15 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal RdClk_i is matched
#  Time: 15 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal rd_en_i is matched
#  Time: 15 ns  Iteration: 1  Instance:

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# ** Note: Port mapped signal wr_data_i is matched and the value is 00000000000000000000000000001010
# Time: 15 ns Iteration: 1 Instance:
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
# Time: 15 ns Iteration: 1 Instance:
# ** Warning: There is an 'U'|'X'|'W'|'Z'|'-' in an arithmetic operand, the result will be 'X'(es).
# Time: 15 ns Iteration: 1 Instance:
# ** Note: Port mapped signal rd_data_o is matched and the value is xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
# Time: 15 ns Iteration: 1 Instance:
# ** Note: Port mapped signal WrClk_i is matched
# Time: 15 ns Iteration: 1 Instance:
# ** Note: Port mapped signal Areset_i is matched
# Time: 25 ns Iteration: 1 Instance:
# ** Note: Port mapped signal wr_en_i is matched
# Time: 25 ns Iteration: 1 Instance: # ** Note: Port mapped signal full_o is matched
# Time: 25 ns Iteration: 1 Instance:
# ** Note: Port mapped signal RdClk_i is matched
# Time: 25 ns Iteration: 1 Instance:
# ** Note: Port mapped signal rd_en_i is matched
# Time: 25 ns Iteration: 1 Instance:
# ** Note: Port mapped signal wr_data_i is matched and the value is 00000000000000000000000000001010
# Time: 25 ns Iteration: 1 Instance:
# ** Note: Port mapped signal rd_data_o is matched and the value is 00000000000000000000000000000000
# Time: 25 ns Iteration: 1 Instance:
# ** Note: Port mapped signal WrClk_i is matched
# Time: 25 ns Iteration: 1 Instance:
# ** Note: Port mapped signal Areset_i is matched
# Time: 35 ns Iteration: 1 Instance:
# ** Note: Port mapped signal wr_en_i is matched
# Time: 35 ns Iteration: 1 Instance:
# ** Note: Port mapped signal full_o is matched
# Time: 35 ns Iteration: 1 Instance:
# ** Note: Port mapped signal RdClk_i is matched
# Time: 35 ns Iteration: 1 Instance:
# ** Note: Port mapped signal rd_en_i is matched
# Time: 35 ns Iteration: 1 Instance:
# ** Note: Port mapped signal wr_data_i is matched and the value is 00000000000000000000000000001010
# Time: 35 ns Iteration: 1 Instance:
Case2 : Port mapped signal rd_data_o is matched and the value is 00000000000000000000000000000000
# Time: 35 ns Iteration: 1 Instance:
# ** Note: Port mapped signal WrClk_i is matched
# Time: 35 ns Iteration: 1 Instance:
# ** Note: Port mapped signal Areset_i is matched
# Time: 45 ns Iteration: 1 Instance:
# ** Note: Port mapped signal wr_en_i is matched
# Time: 45 ns Iteration: 1 Instance:
# ** Note: Port mapped signal full_o is matched
# Time: 45 ns Iteration: 1 Instance:
# ** Note: Port mapped signal RdClk_i is matched
# Time: 45 ns Iteration: 1 Instance:
# ** Note: Port mapped signal rd_en_i is matched

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```
#    Time: 45 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal wr_data_i is matched   and the value is 00000000000000000000000000001010
Case 3: Port mapped signal rd_data_o is matched   and the value is 00000000000000000000000000000000
#    Time: 195 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal WrClk_i is matched
#    Time: 195 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal Areset_i is matched
#    Time: 205 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal wr_en_i is matched
#    Time: 205 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal full_o is matched
#    Time: 205 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal RdClk_i is matched
#    Time: 205 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal rd_en_i is matched
#    Time: 205 ns  Iteration: 1  Instance:
Case4: Port mapped signal rd_data_o is matched   and the value is 00000000000000000000000000000000
#    Time: 205 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal WrClk_i is matched
#    Time: 205 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal Areset_i is matched
#    Time: 215 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal wr_en_i is matched
#    Time: 215 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal full_o is matched
#    Time: 215 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal RdClk_i is matched
#    Time: 215 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal rd_en_i is matched
#    Time: 215 ns  Iteration: 1  Instance:
# ** Note: Port mapped signal wr_data_i is matched
```

## VI. CONCLUSION

Before for testing the functionality of any individual module as per DO-254 gives a bad review from a customer side because of the engineer fails to verify the all modes of scenario's which tells the new method which is self checking test bench for performing the final target level testing or verification stage. It gives an accurate measurement to the design for production.

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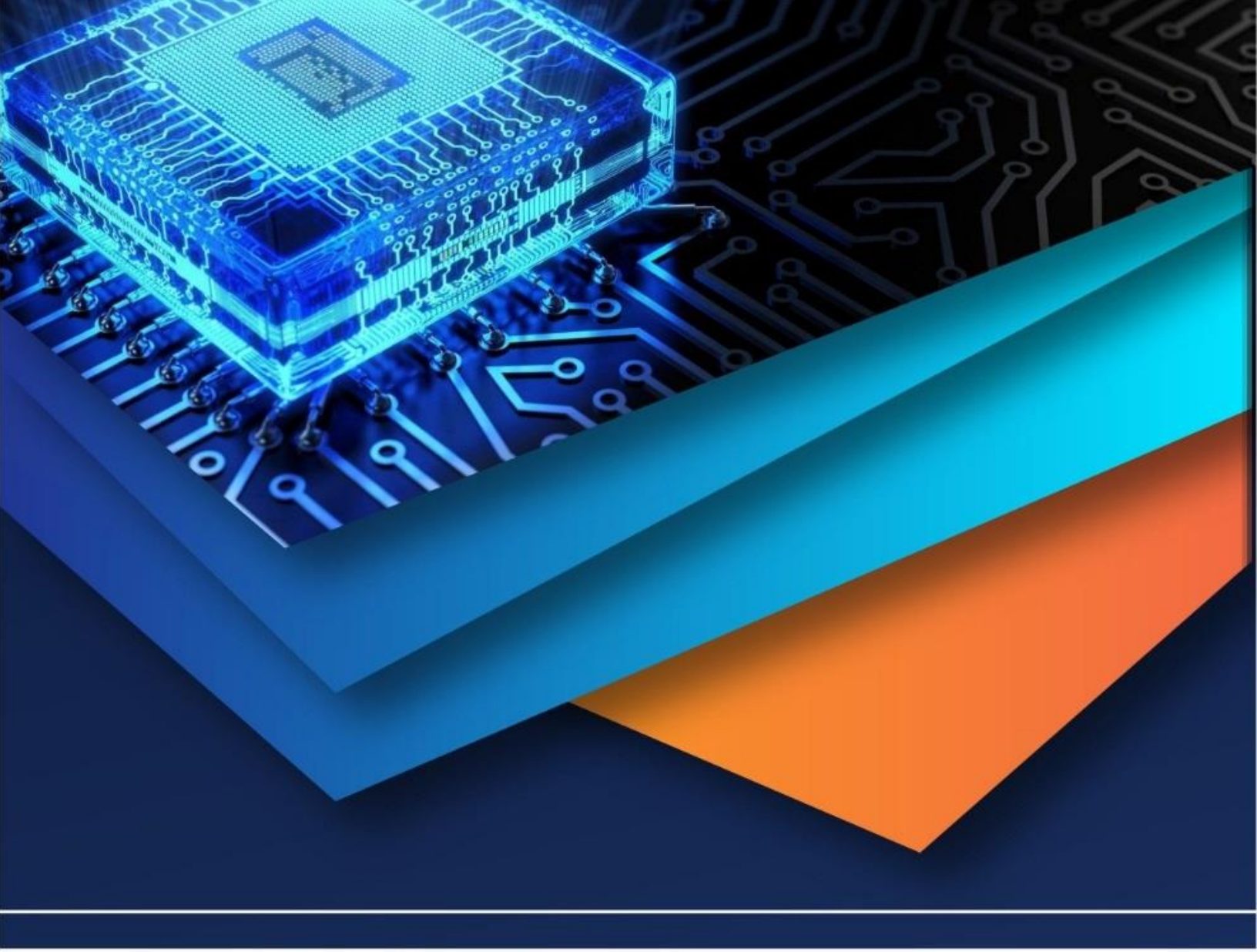

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