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Evaluation of the Parameters of Ring Oscillators Using the CMOS and CNT 32nm Technology

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Abstract: ***In this article a comparative study of various parameters of ring oscillators were evaluated using CMOS and CNT based transistors in 32nm technology. After the comparative study the results exhibited that the CNT based transistor technology displayed better results as compared to the CMOS transistor based technology. The various parameters evaluated were Power Consumption including two factors: leakage power and leakage current as well as Frequency and Delay. In this article to determine these parameters in both CMOS and CNTFET based technology with the help of SPICE simulation tool. The power consumption and delay is reduced in ring oscillators using CNT transistor based technology. The frequency also exhibited better in CNTFET based technology because time duration is reduced in this technology as compared to CMOS transistor technology. Overall concept of this article CNT transistor based technology indicates better evaluation and performance parameters for ring oscillators as compared to CMOS technology.***

Keywords: Carbon nanotubes, CMOS, Ring Oscillators, Power Consumption, Frequency, Delay.

I. INTRODUCTION

There is a ubiquitous oscillatory behavior profound in all physical systems. These behaviors are mostly and especially exhibited in optical and electronic systems. The selection of the channels and the translation of frequency to various information signals is performed via oscillators in different systems of light wave communication and the radiofrequency. These oscillators also perform as the synchronization operations, wherever there is a requirement of time references like as in the clock signal, therefore these are also present in those electronic systems which are digital. A regular periodic signal or the time reference which is exhibited perfectly is designated as perfect oscillator. There are many unwanted factors which hampers the performance of the physical oscillators being perturbation or the noise. Whilst, using the practical oscillators for producing the signals, they were unable to produce the perfectly periodic signals, as it is a physical system which is noisy, and the response which is produced regarding the noisy perturbation is unique and this characteristic makes them unique [1]. The availability of the oscillator are in multiple variety but their performance regarding various performance issues is different amongst the classes of oscillators being the operational principle and working, oscillation band frequency and their performance in the environment of perturbation or the noisy environment. There are a variety of oscillators which re being used but comparing all of them, ith has been noticed that the ring oscillators work better than the relaxation oscillators but on comparing them with the sinusoidal oscillators they are less i.e the performance of the ring oscillators as compared with the two other types of oscillators, relaxation and sinusoidal the ring has been found to perform better than the relaxation but its performance is deprived as compared to the sinusoidal [2]. Various other scientists are working on the improvisation of ring oscillator performances so as to attain excellent and better level of satisfaction. Further, the scientists are also exhibiting better and successful results in the communication systems, as the satisfaction level is attained in both the important parameters being the operational speed and noise performance [1][2]. The basic items of the current electronic and the new technological advancements are the transistors. The materials which can be utilized in these nanostructures are nano-tubes or wires, graphene. The first nano transistor was developed in the year of 1998. This is a new emerging field in the ring oscillators and transistors which is now-a-days replacing and exchanging the existing technology of CMOS (complementary metal-oxide semiconductors) in terms of performance limits which are specified, the potential applications are identified with efficient electronic properties along with the physical modeling. Infact, CNTFET is currently holding the topmost position regarding the nanoelectronics future and have now started being considered as one of the important and favorite alternative for the CMOS devices as the results attained by using the CNT 32nm are better than the CMOS. They cover all the main features within them being the consumption of the power is low and the results accomplished is high. Further, the single wallend carbon nanotube exhibits attractive, different and unique properties. It exhibits high ranges of lengths from few tens of nanometers to various centimeters, showing single digit nanometer and also the thermal stabilities. The consumption of the power is also low as the CNTFET used is single walled carbon nanotube which functions as a channel. Now, there is a fast and speedious growth of CNT technology based

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transistors and oscillators, both theoretically as well as experimentally, because of its increasing demands for their effective and efficient better properties [3]. For the future prospects, it is exhibited that the higher performance of the nano-electronic circuits is only possible using the transistors, amongst them the best results can be attained using the carbon nanotubes field effect transistor. CNTFET can further downscale the digital electronics as compared to CMOS technology as it has reached the physical fundamental limits. The aforementioned downscaling is performed and compared amongst both the technologies using the Moore's law. As, we are heading towards the advanced technology, the demands of the market in the current scenario is enhancing the system on chip significance, i.e the maximum number of transistors which are possible on single chip. For comparing the performance of the digital circuits, the only criteria for comparing should not only be the digital performance [4][5].

II. LITERATURE REVIEW

Saxena et.al 2017 stated that for the production of the ring oscillators the use of carbon nanotube transistors exhibited better results as compared to the silicon based transistors. These results were based on the analysis which was performed using the carbon nanotube field effect transistor based on the ring oscillators. They stated that this CNFET was the nearest and one of the best possible substitution for the silicon based integrated circuit technology, as the increase in the performance of the conventional methods exhibited fundamental physical limits in near future. Their research was highly influenced by the community of material science as there are many existing materials which create obstacles and practically compete with the existing transistors. They compared carbon nanotubes with graphene in their studies and exhibited that the former displayed better properties for the producing the field effect transistor. They also said that the aforementioned can cover the complete production technologies. So they have concludes stating that the CNFET used is better than the silicon based transistor for making ring oscillator [4]. Shivhare et.al in 2016 stated the CMOS ring oscillator which was designed for low power and was used for the analysis of power consumption. In this paper, there was comparison of two designs i.e this low power design for power consumption was compared to various existing designs. In this paper the simulations were performed using the Cadence virtuoso tool 180 nm CMOS technology and the obtained results were analyzed for the power consumption. Further, the positive feedbacks were used by the ring oscillator which was proposed via the circuits which were based on the inverter and were operated with nine cascading CMOS inverter. The results obtained exhibited that when compared to the previous designs the consumption of the power was decreased by 28.4% at 0.9v and 54.6% at 1v [6]. Sarkar et.al 2009 have stated about the operating principle and the structure of the ring oscillators. They have described about the oscillation frequency of a of a CMOS delay cell which is based on the conventional ring oscillator. In their work they have also calculated the propagation delay of the delay stages. They have also exhibited the limitations along with the conventional ring oscillator and they have also suggested and described some of the techniques using which these limitations can be overcome. They have also indicated the modified structures of ring oscillators which can exhibit higher frequency oscillations. The modified structures being negative skewed delay RO, multi feedback RO, coupled Ro etc. they have also investigated about the noise sources effect on the ring oscillator output. They have also stated the applications which were highly efficient for the tuning characteristics of the voltage and were able to exhibit multiphase outputs. These aforementioned applications were based on the ring oscillators [2].

III. RESARCH METHODOLOGY

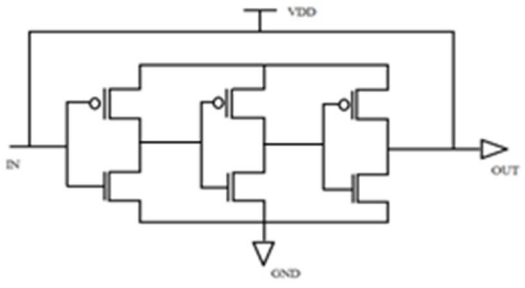

Fig.1 Representation of Three Phase Ring Oscillator Using CMOS Technology

The ring oscillators discussed in the proposed study using the CMOS and CNT 32nm Technology is found to comprise of distinct inverter amplifier phases incorporating a feedback to the input. Further, these devices are found to be utilized in the PLL devices. From this study it can be seen that inverted output is achieved at the odd number of phases were the oscillation starts,as the input is

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provided at the primary phase. The phases considered for the comparison are represented in the below Fig. 1 and fig.2. Indicating three phase Ring oscillator using CMOS and cnt based transistor technology.

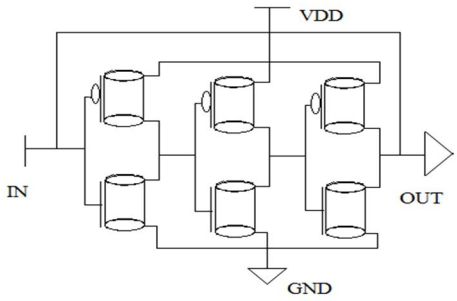

Figure 2: Representation of Three Phase Ring Oscillator using CNT Technology

The design of the ring oscillator is developed considering the significant factor such as gate delay as the gate cannot switch instantly since these are fabricated with MOSFET. Also the charging of the gate capacitance is performed before the flow of current between drain and source such that there is delay within every inverter to deliver output. Therefore, the number of phases has been increased in the ring oscillator to provide higher gate delay. The effect of single inverter amplifier with a negative feedback is provided by considering the odd number of inverter stages that gives a gain of value greater than 1. This process is performed such that an amplified output is obtained in an opposite direction to the input with an amount more than the input. The amplified and inverted output that is obtained is further propagated to the input with delay such that the received output is again amplified and inverted.

IV. RESULTS AND DISCUSSION

In the proposed study is simulated using transient analysis varying from 0 ps to 200 ps to determine the Power consumption as shown in Fig.3. The result obtained indicates that Power dissipation 29.01E-10W at 71 ps and average power dissipation is given by 4.9636E-06W. Also, the power consumption is found to be linear as CMOS transistor takes time to stabilize itself.
Besides, ring oscillator provides the fluctuations in the waveform of power consumption which is found to be considerably varying even at small change.

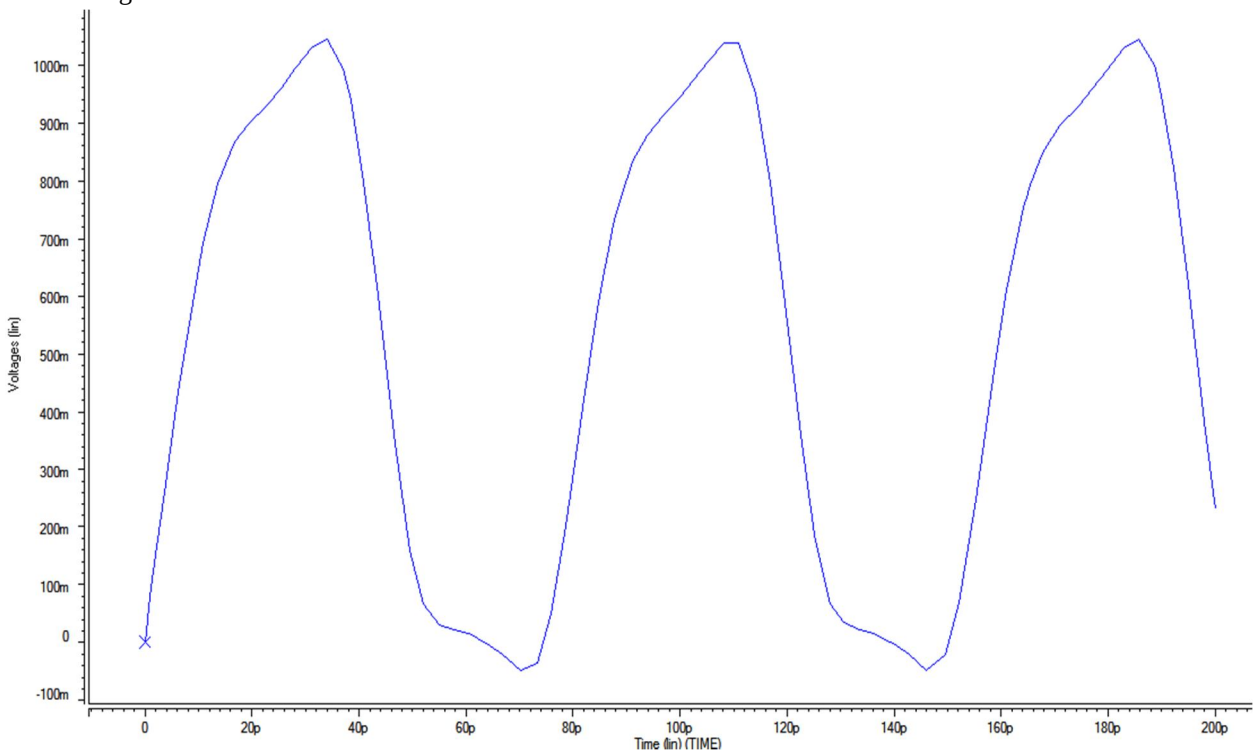

Figure.3. Simulation of Three Phase Ring Oscillator Using CMOS Technology

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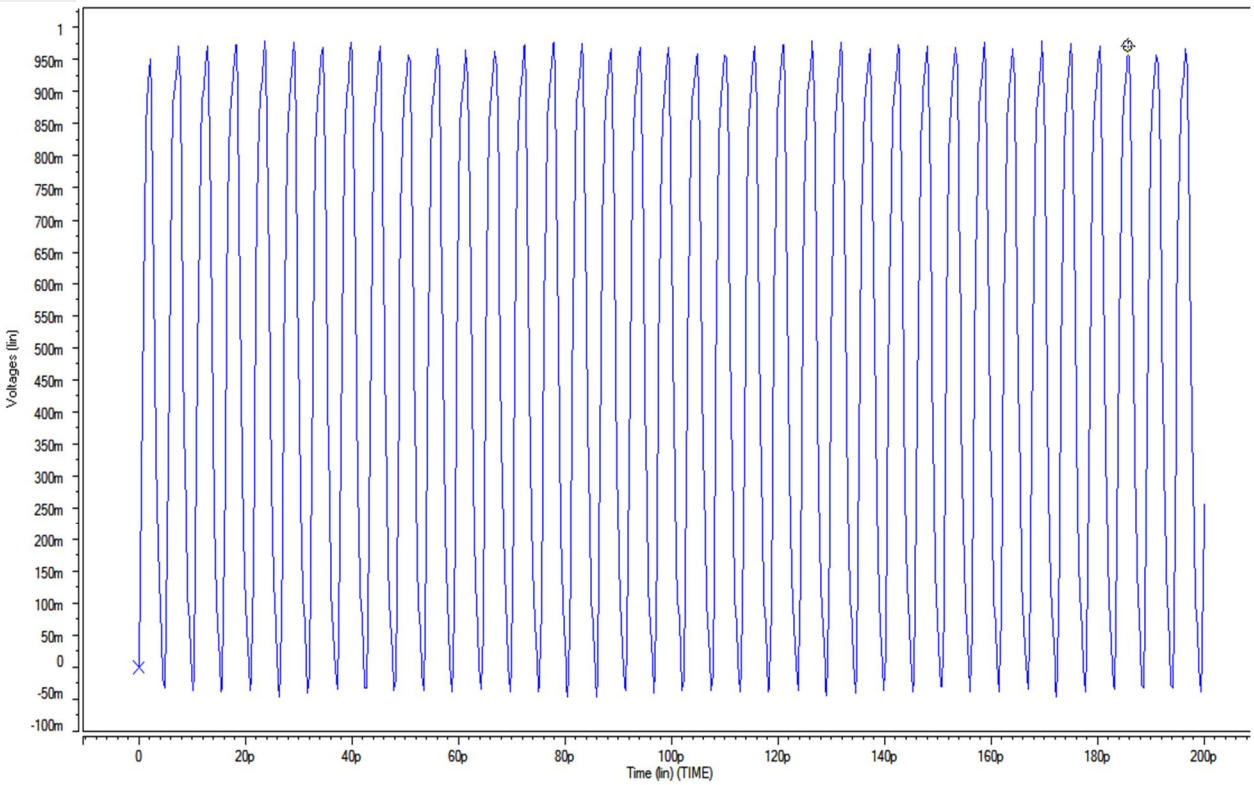

Figure.4: Simulation of Three Phase Ring Oscillator Using CNT Technology.

The transient analysis is performed by maintaining the frequency at 341 MHz. . As the supply voltage is maintained at 1V with a simulated frequency of 1 Hz At 19.95 MHz, the noise is found to be 7.55 kdBc/Hz. Therefore, the Periodic noise response with respect to the transient analysis is found to vary from 0 to 200ps for a period.

Comparative Table of 3 Stage Ring Oscillators with 32nm CNT and CMOS Technology

Performance Parameter	CMOS	CNT
Technology	32nm	32nm
Supply voltage	1V	1V
Frequency	300MHz	340MHz
Average power	4.9636E-06W	8.2689E-07W
Leakage power	29.01E-10W	5.579E-10W
Leakage current	29.01E-10A	5.579E-10A

Table 1 represents the comparison of results obtained in the existing research with that of proposed research. The previous study indicates that unit delay while the proposed research shows the delay of 3-stage. From this research it was observed that the delay increases with the increase in number of stages in the circuit. Furthermore the oscillation frequency of the oscillator is determined by the calculation of PSS. Also, PNOISE is used for the calculation of noise folding and frequency convention effects. In this study, it was noticed that an overall power is reduced by 18.9 %. In addition, a reduction in phase noise and frequency jitter to .34 kdBc/Hz and 31.63 KHz respectively were observed.

V. CONCLUSION

The proposed research has successfully designed a 3-stage ring oscillator and was simulated using spice tool in 32 nm technology. This research also conducted a relative study of various parameters of ring oscillators using the comparative of CMOS and CNT transistor based technology. Further, several significant parameters i.e. delay, power, phase noise were analyzed and reduced to

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enhance the efficiency of ring oscillator. Also, this research has been utilized to decreased power consumption and frequency to perform optimized operation of the ring oscillator.

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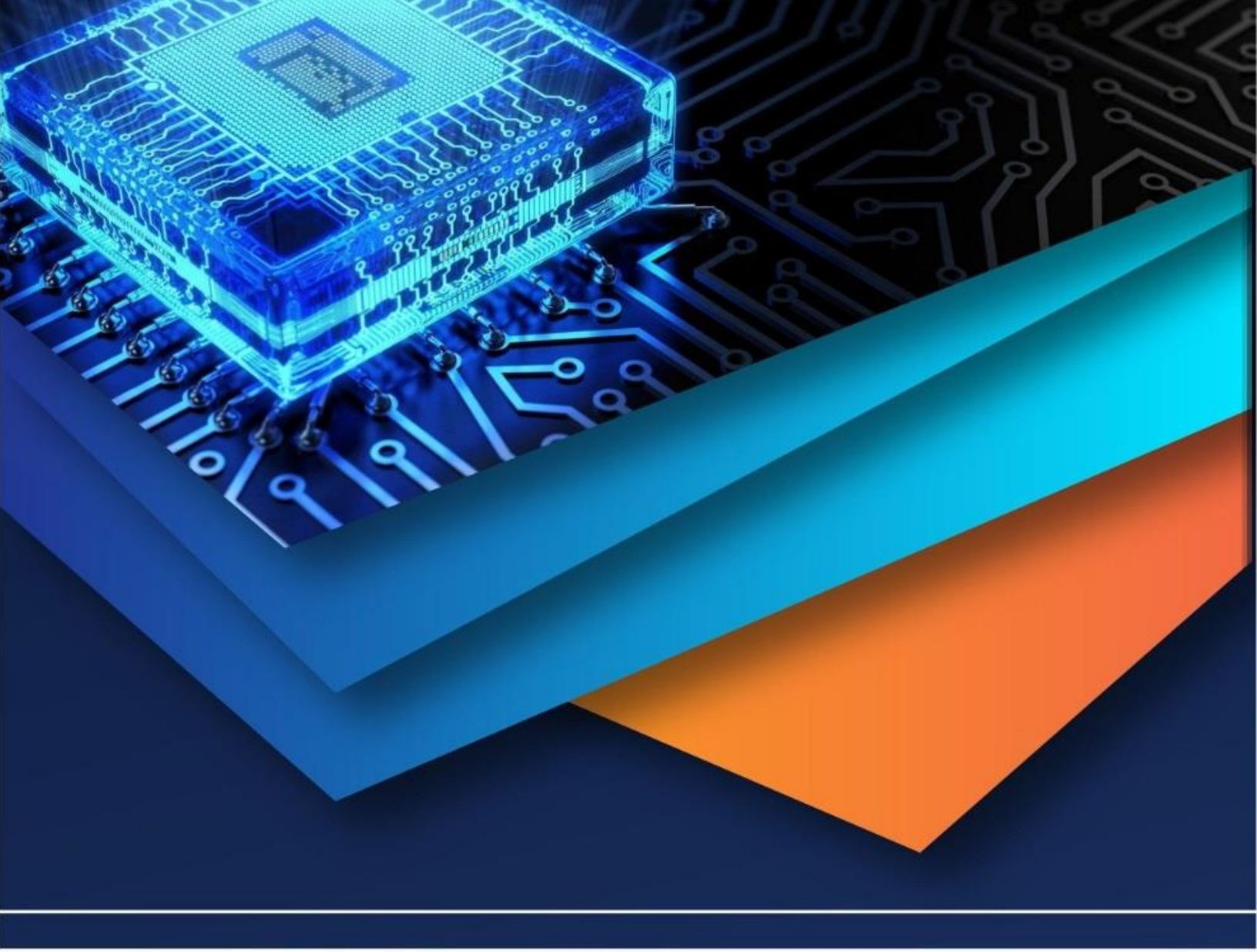

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