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Design and Analysis of Reduced Harmonic Multi-Level Inverter for Solar Integrated Grid Connected System

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***Abstract:** This project proposes a single-phase Three-level, five-level and seven-level inverter for PV grid-connected photovoltaic systems, with a pulse width-modulated (PWM) control scheme. Three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing seven levels of output-voltage levels from the dc supply voltage. Multilevel inverter performance is compared with three level inverter, five level and seven level inverters to reduce their harmonic distortion and by increasing levels with reduced number of switches losses are decreased and harmonics are eliminated. This project presents the cascaded H-bridge multilevel inverters for single phase PV grid connected system and their effects on grid current. Any carrier based PWM is applicable for cascaded H-bridge (CHB). An advanced grid connected PV system consists of PV panel, Single phase three level, five level and seven level inverter, grid side control. The main objective of this paper is to get the reliable and stable output of modular grid connected photovoltaic generation system with single phase seven level inverter topology. It is obtained by using MATLAB software.*

***Keywords:** Multi level inverter; SPWM; harmonic analysis; power electronics;*

I. INTRODUCTION

A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10kW [1]. Types of single-phase grid-connected inverters have been investigated [2]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [3].

Multilevel inverters are promising; they have nearly sinusoidal output voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [4].

Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped, flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel. This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter [5] that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique.

Grid connected photovoltaic (PV) converters represent the most widespread solution for residential renewable energy generation. While classical designs of PV converters feature a grid frequency transformer, which is a typically heavy and costly component, at the interface between the converter and the electrical grid, researchers are now considering transformer less architectures in order to reduce costs and weight and improve efficiency.

Removing the grid frequency transformer entails all the benefits above but worsens the output power quality, allowing the injection of dc current into the grid [6], [7] and giving rise to the problem of ground leakage current [8] to clean the output voltage and current from high frequency switching components. Further reduction in cost and weight and improvement in efficiency can be achieved by reducing the filter size, and this is the goal of multilevel converters. Multilevel converters have been investigated for years [9], but only recently have the results of such researches found their way to commercial PV converters. Since they can

synthesize the output voltages using more levels, multilevel converters outperform conventional two and three-level converters in terms of harmonic distortion. Moreover, multilevel converters subdivide the input voltage among several power devices, allowing for the use of more efficient devices. Multilevel converters were initially employed in high-voltage industrial and power train applications. They were first introduced in renewable energy converters inside utility-scale plants, in which they are still largely employed [10]–[12]. Recently, they have found their way to residential-scale single-phase PV converters, where they currently represent a hot research topic.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

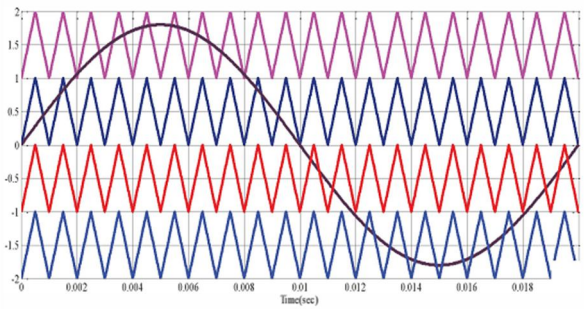
Cascaded H-bridge (CHB) multilevel inverter is one of the popular topology for converter used in high power medium voltage drives. It contains multiple units of single phase H-bridge power cells. The H-bridge cells are normally connected in cascaded on its ac side to achieve low harmonic distortion and medium voltage operation. In practice, the number of power cells in a CHB inverter is mainly determines by its operating voltage and the cost required for manufacturing. The CHB multilevel inverter requires a number of isolated dc supplies each of which feeds an H-bridge power cell [3]. The number of voltage levels in a CHB inverter can be found from

$$m = 2H + 1 \tag{1}$$

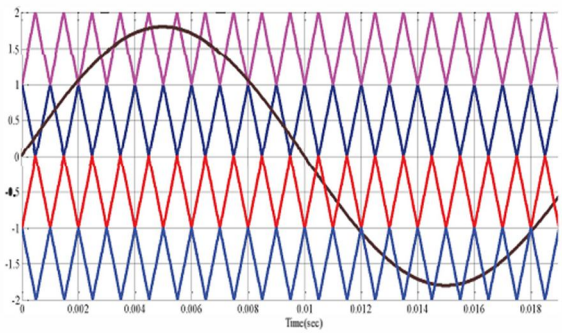
Where H is the number of cells per phase leg in H-bridge. For the CHB inverter, voltage level m is always an odd number while in other multilevel topologies like diode-clamped inverters it can have either an even or odd number of levels. Any carrier based PWM schemes can be used for CHB inverter. The carrier based modulation schemes for multilevel inverter can be classified in two categories as follows

A. level Shifted Multicarrier Modulation

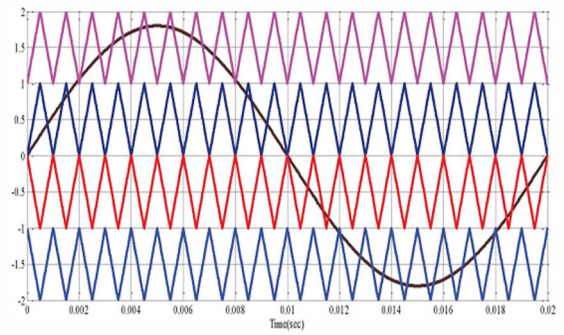
The level shifted modulation scheme requires (m-I) triangular carriers for m level CHB inverter, all the carriers have the same frequency and the same amplitude. The (m-I) triangular carriers are vertically placed such that the bands forms by the carriers are contiguous. Following figure shows three schemes for the level shifted multicarrier modulation. (a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition(APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition(POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference.



(a)IPD.



(b)APOD.



(c)POD.

Fig. 1. Level shifted PWM the frequency modulation index is given by

$$m_f = f_{cr} / f_m \tag{2}$$

Which remains the same as that for the phase shifted modulation scheme whereas the amplitude modulation index is defined as V,

$$m_a = \frac{V_m}{V_{cr}(m-1)} \tag{3}$$

Where Vm is peak amplitude of the modulating wave Vm and Vcr is the peak amplitude of each carrier wave.

B. Phase shifted Multicarrier Modulation

In general, a multilevel inverter with m voltage levels requires (m-l) triangular carriers. In the phase shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak to peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by

$$\phi_{cr} = 360^\circ /(m-1) \tag{4}$$

The modulating signal is usually a three phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with carrier waves.

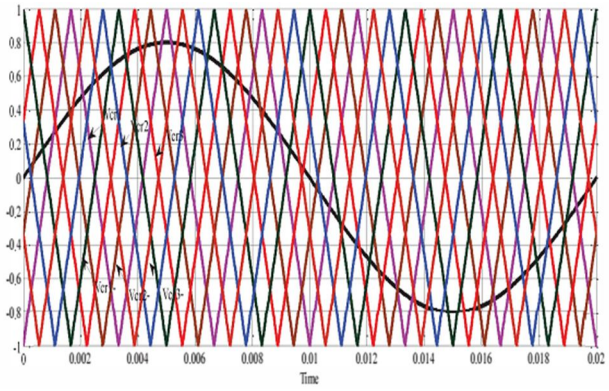


Fig. 2. Phase shift PWM for seven-level inverter.

The principle of the phase-shifted modulation for a seven level CHB inverter is shown in fig. 2, where six triangular carriers are required with a 60° phase displacement (using equation (4)) between any two adjacent carriers. Modulating wave VMA is used. The carriers Veri, Vcr2, and Vcr3 are used to generate gatings for the upper switches QI, Qs, and Q9 in the left legs of power cells HI, H2 and H3 as shown in fig 3., respectively. The other three carriers, Vcrl-, Vcr2-, and Vcr3- , which are 1800 out of phase with Veri, Vcr2, and Vcr3, respectively, produce the gating for the upper switches Q2, Q6 and QIO in the right legs of the H- bridge cells. The gate signals for all the lower switches in the H-bridge legs are not shown since these switches operate in a complementary manner with respect to their corresponding switches [3]. The amplitude modulation index for phase shifted PWM as given in equation (5) is different than level shifted PWM. It does not depend on number of levels

$$m_a = \frac{V_m}{V_{cr}} \tag{5}$$

TABLE I. SWITCHING TABLE

Output Voltage	Switching States		
	(Q1,Q2,Q3,Q4)	(Q5,Q6,Q7,Q8)	(Q9,Q10,Q11,Q12)
3E	(1,0,1,0)	(1,0,1,0)	(1,0,1,0)
2E	(1,0,1,0)	(1,0,1,0)	(1,1,0,0)
E	(1,0,1,0)	(1,1,0,0)	(1,1,0,0)
0	(1,1,0,0)	(1,1,0,0)	(1,1,0,0)
-E	(0,1,0,1)	(0,0,1,1)	(0,0,1,1)
-2E	(0,1,0,1)	(0,1,0,1)	(0,0,1,1)
-3E	(0,1,0,1)	(0,1,0,1)	(0,1,0,1)

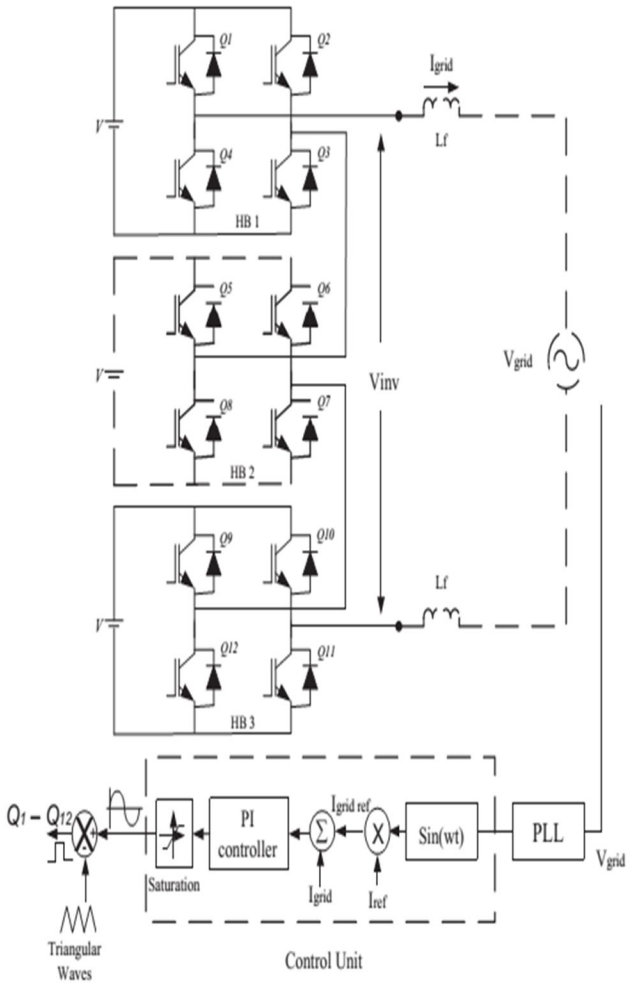


Fig. 3. Circuit diagram of Cascaded Seven level Inverter for single phase Grid Connected System

In this Phase locked loop (PLL) is used to synchronies the grid frequency with the supply frequency which makes the grid voltage and grid current are in phase with each other as shown in simulation result section. The Lf is the current limiting filter to limit the grid current. The current limiting inductor Lf is given by

$$L_f = \frac{V_{DC}}{8 \times f_{sw} \times \Delta I_{L\max}} \quad (6)$$

Where VDC is the DC voltage of the inverter, Is", is switching frequency of the inductor and MLmax is ripple current of the inductor. The feedback current controller is used for this application. In this PI algorithm, Ire fis generated by comparing grid voltage with the reference voltage. Ire f is then multiplied by the output of PLL to generate 19ridre/- The current injected into the grid known as grid current Ignd, was sensed and fed back to a comparator that compared it with the reference current 19ridre/ The error from the comparison process of 19nd and Igridref was fed into the PI controller. The output of the PI controller, also known as Vref, being compared with the triangular wave to produce the switching signals for Q,-Q'2'.

III. MATLAB/SIMULINK RESULTS

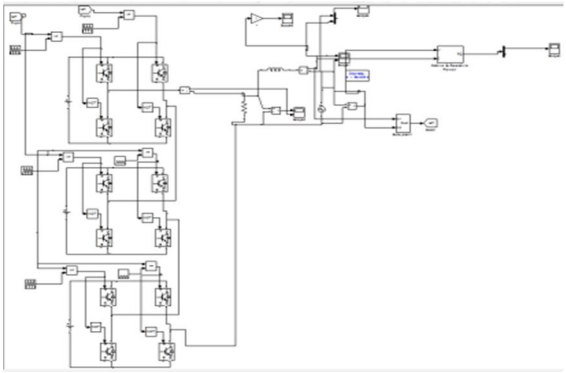
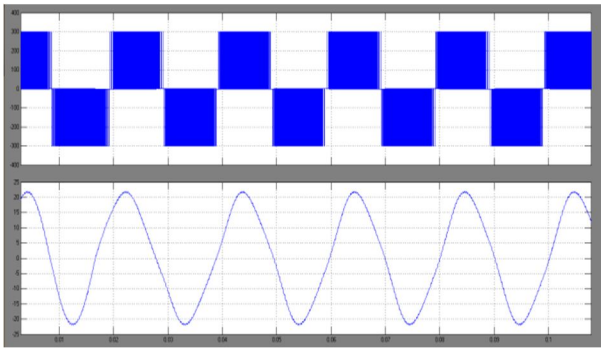


Fig 4 Circuit diagram of Cascaded Seven level Inverter for single phase Grid Connected System.



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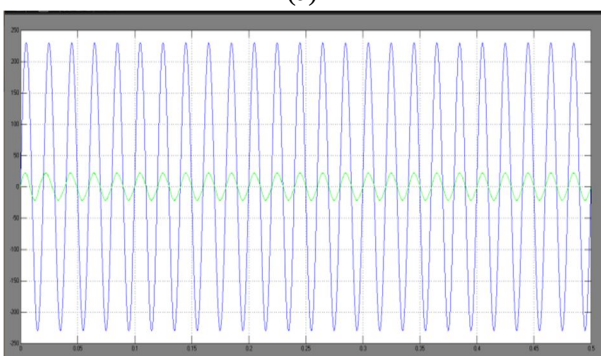

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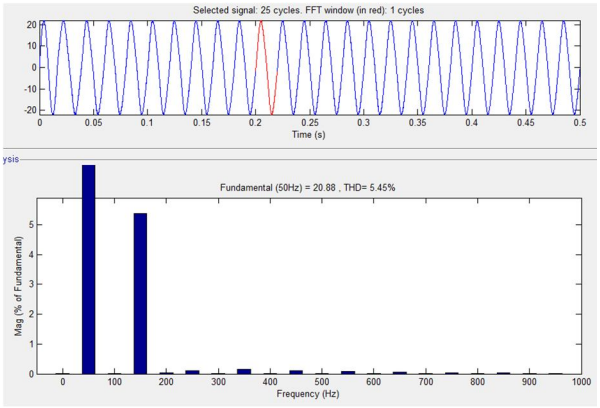

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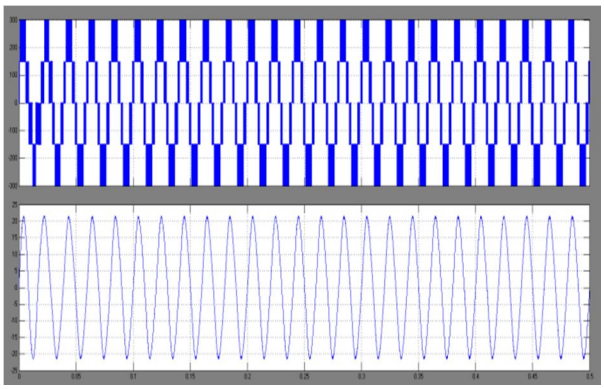
Fig, 5.(a) Three level Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c)Harmonic Analysis of Grid Current.



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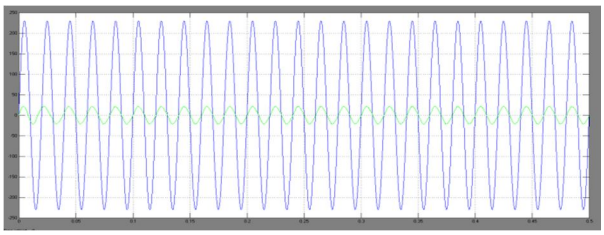

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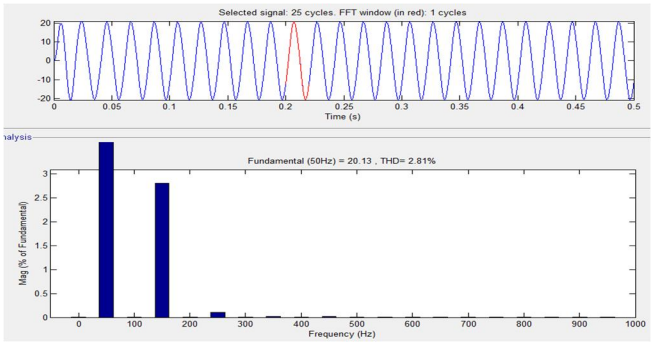
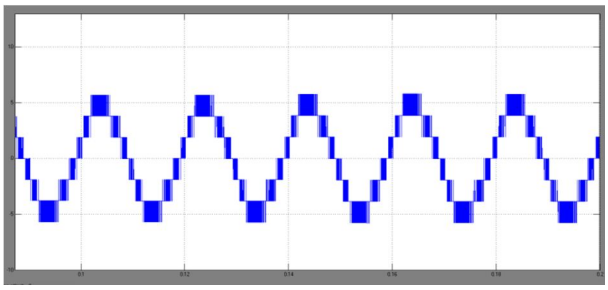


(c)

Fig. 6,(a) Five level Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c) Harmonic Analysis of Grid Current.



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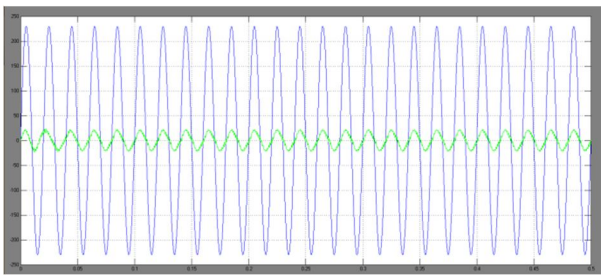

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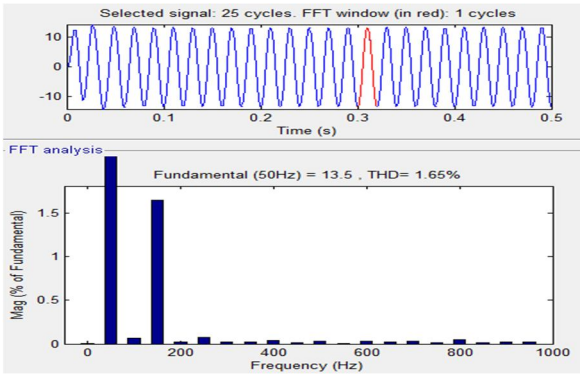


(c)

Fig 7(a) seven level Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c) Harmonic Analysis of Grid Current. Fig

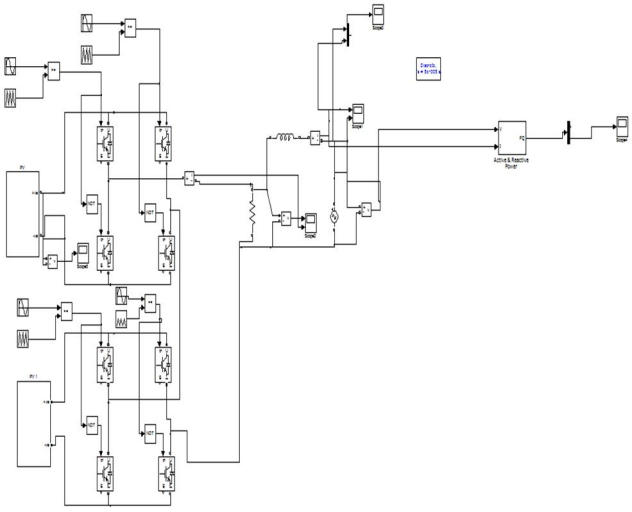
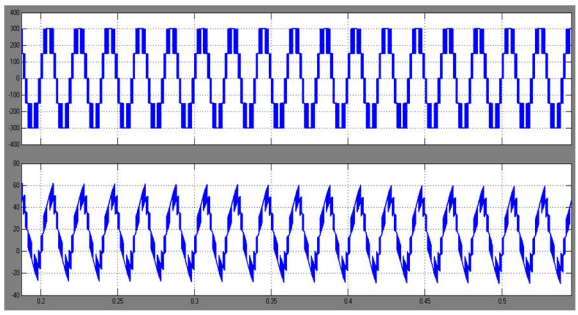


Fig 8 Circuit diagram of Cascaded five levels Inverter for single phase Grid Connected PV System.



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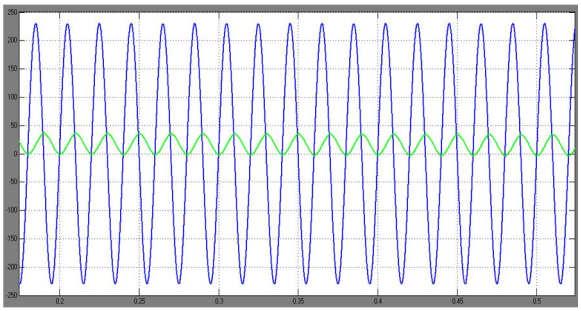

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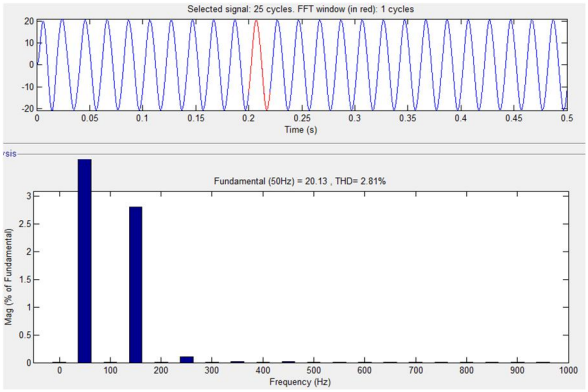

(c)

Fig 9 (a) five level PV Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c) Harmonic Analysis of Grid Current.

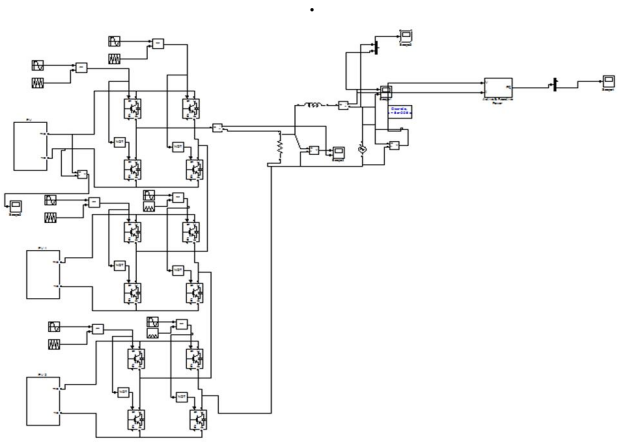

Fig 10 Circuit diagram of Cascaded seven levels Inverter for single phase Grid Connected PV System

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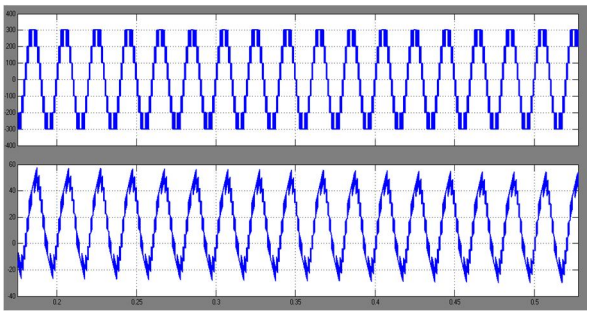

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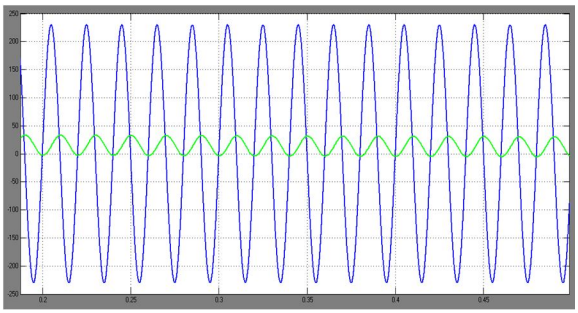

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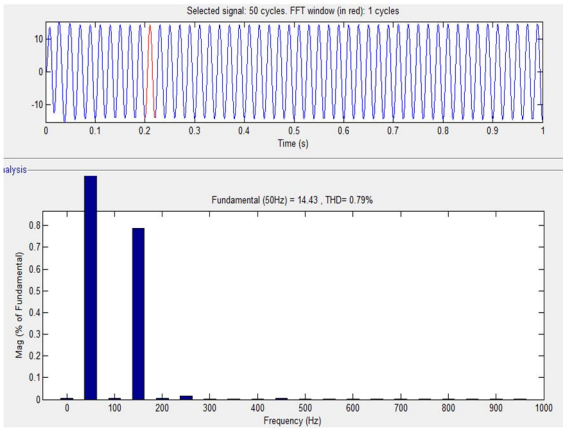


Fig 11 a) seven level PV Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c) Harmonic Analysis of Grid Current.

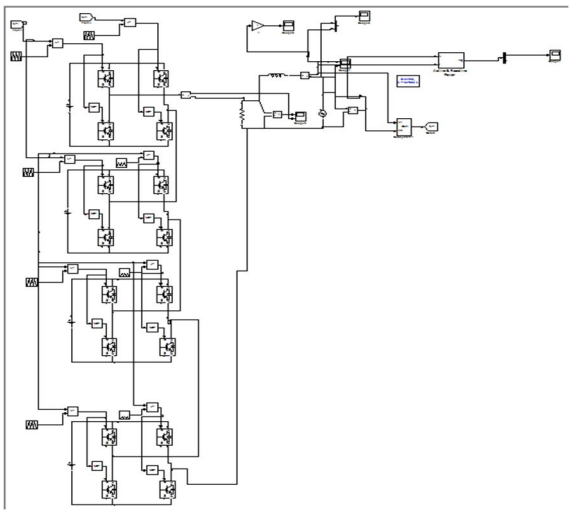
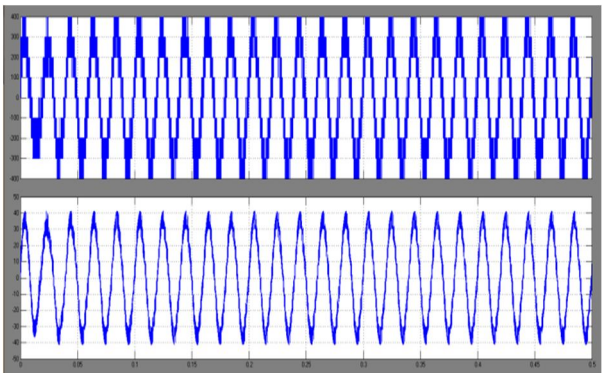


Fig 12 Circuit diagram of Cascaded nine levels Inverter for single phase Grid Connected System.



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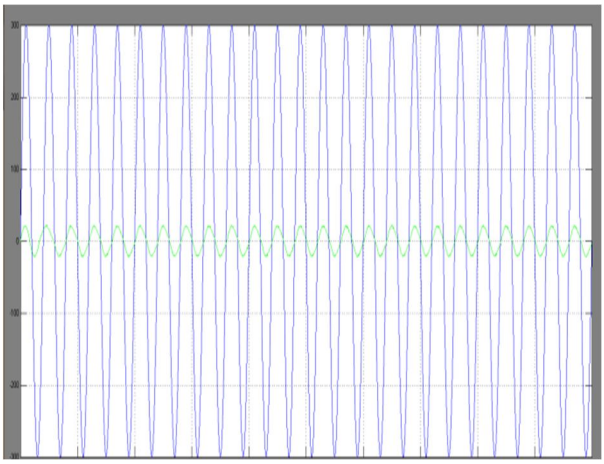

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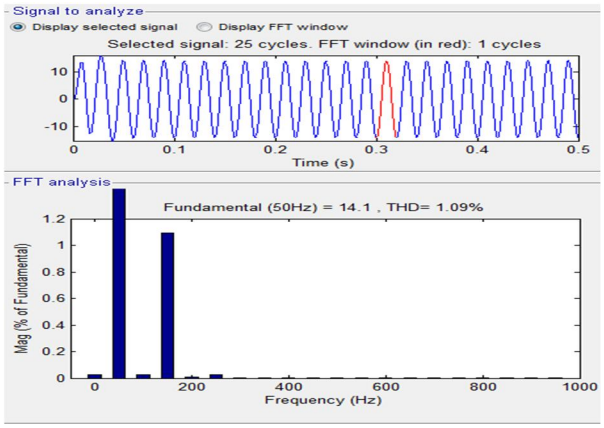

(c)

Fig 13(a) nine level Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c) Harmonic Analysis of Grid Current.

IV. CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes three reference signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel inverter was analyzed in detail. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. The less THD in the nine-level inverter compared with that in the seven, five- and three-level inverters is an attractive solution for grid-connected PV inverters. Control strategy is carried out to synchronies the grid frequency with the inverter frequency and to generate the modulating wave to fire the switches of the inverter.

The harmonic analysis of grid current is carried out for different levels. From the analysis it is clear that as the number of levels increases the %THD decreases. So multilevel inverter is used for grid connected system to inject less harmonic current to the grid.

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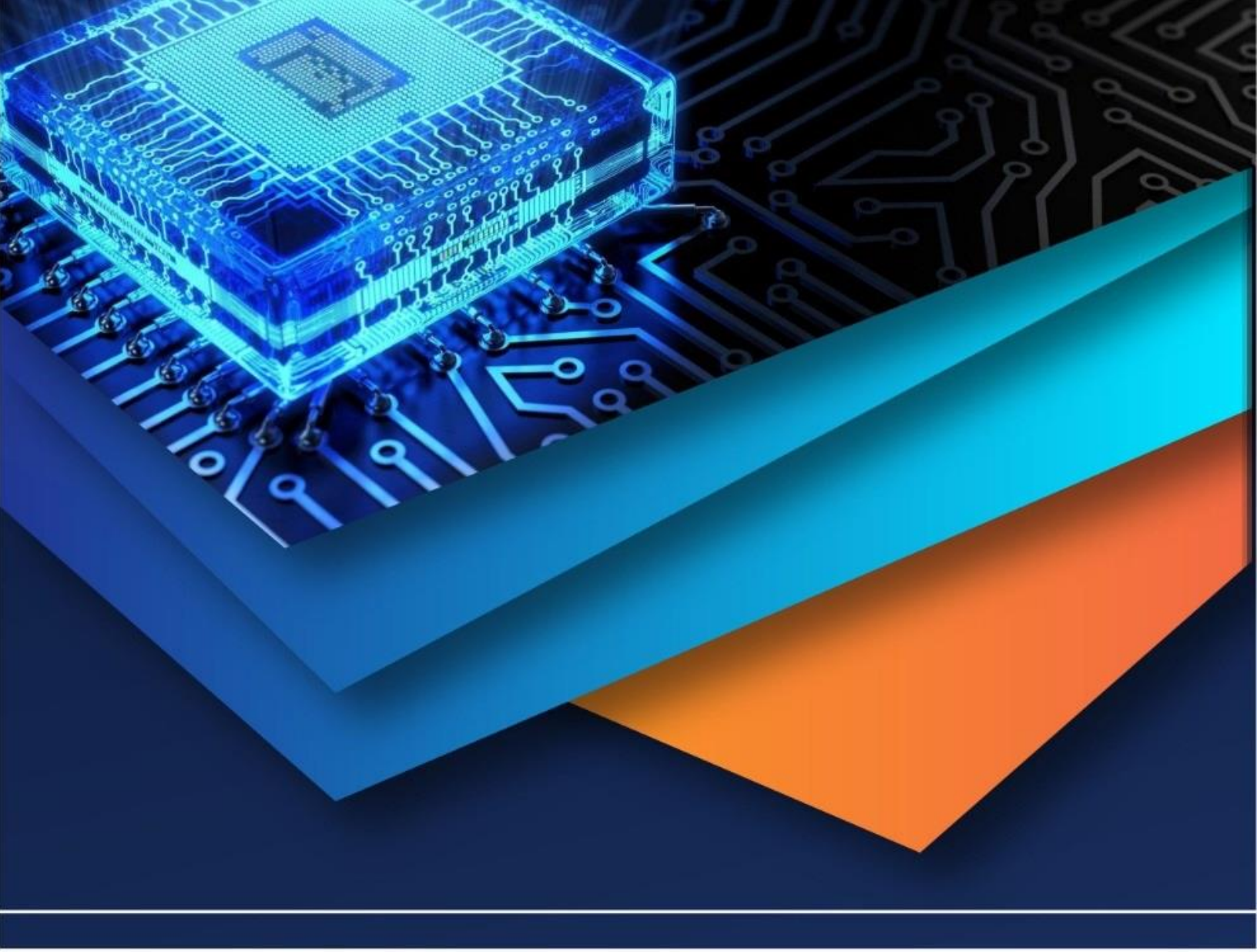

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