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Secondary - Side Phase - Shift - Controlled ZVS Three Level DC/DC Converter Topology

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Abstract: ***This paper presents a soft switching dc/dc converter with secondary - side phase shift control strategy is proposed to improve the conversion efficiency and minimize the primary switch voltage stress to half of the input voltage. The Zero Voltage Switching (ZVS) performance is achieved for both primary and secondary side devices to reduce the switching losses due to secondary side phase shift control scheme. The voltage stress of the primary switches is only half of the input voltage by employing the improved Three Level structure, which makes the low voltage rated power devices available to improve the circuit performance. This paper describes the main operational modes of the proposed converter as well as simulation results based on the MATLAB/SIMULINK software and also compares the switching losses of the proposed converter with and without Zero Voltage Switching scheme.***
Index Terms: DC - DC converter, Secondary - Side Phase - Shift control (SSPS), Zero Voltage Switching (ZVS)

I. INTRODUCTION

In the high input voltage applications, the high-voltage rated switching devices are commonly required to construct the conventional full-bridge dc/dc converters. However, the conduction resistor R_{DS_ON} of the switching devices increases exponentially as the voltage stress rises, which results in the severe conduction losses. Recently, many research contributions have been carried out to make the low-voltage rated power devices available in the high input voltage conversion systems. One of the main concepts is to connect the switches in series to sustain the high voltage stress. In [1], three pairs of series switches are connected in the primary side, which reduces the switch voltage stress to only one-third of the high input voltage.
This topology is further extended to N pairs of series switches [2], where the switch voltage stress is reduced to one Nth of the high input voltage. Unfortunately, the number of the transformer windings as well as the control complexity increases as N goes up. A rectifier is added to the middle pair of the three series switch pairs to realize the voltage auto balance of the series input capacitors [3].
The circulating current is a sum of the reflected output current and transformer primary magnetizing current [10].
In order to reduce the primary switch voltage stress, the conventional three-level structure is widely adopted and discussed in [4]–[6], and the switch voltage stress is reduced to half of the input voltage, which is essential for the high input voltage applications. However, the circulating losses and the voltage spikes on the secondary-side diodes still exist with the conventional phase-shift control scheme. In order to overcome the disadvantages of the conventional phase-shift control scheme, secondary-side phase-shift (SSPS) control strategy is proposed in [7], [8],where the duty cycle of both the primary and secondary active switches keeps 0.5 and the phase-shift angle between the primary and secondary switches is employed as the control freedom to regulate the output voltage. With the SSPS control strategy, the output filter inductor in the conventional phase-shift converter can be removed to simplify the circuit structure. Moreover, the freewheeling current is effectively suppressed and the voltage spikes on the secondary-side switches are eliminated.
An SSPS-controlled ZVS dc/dc converter with reduced switch voltage stress is proposed in this paper. The improved three-level structure is employed in the primary side to reduce the switch voltage stress to half of the input voltage. As a result, the low-voltage rated devices can be used to improve the circuit performance. In addition, due to the SSPS control scheme, ZVS switching is achieved for all the power devices in a wide load range without any auxiliary components. Different from the conventional primary-side phase-shift converters, there is no circulating current at the freewheeling stage, which reduces the conduction losses effectively. And the overshoots on the rectifier are effectively suppressed since the rectifier is clamped to the output voltage.

II. PROPOSED CONVERTER

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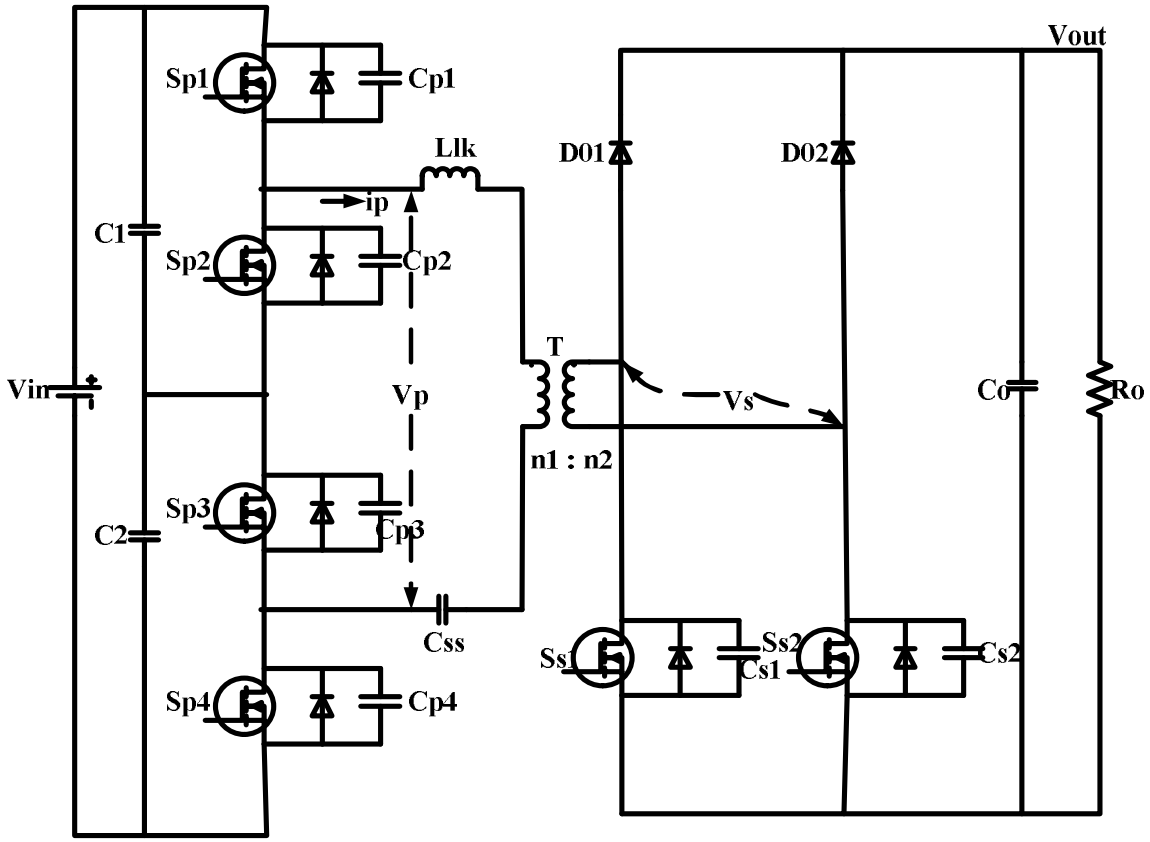

Fig.1: Proposed SSPS ZVS DC/DC Converter

The proposed SSPS-controlled ZVS dc/dc converter for the high input voltage application is shown in Fig. 1, where all of the four primary switches have the constant duty cycle of 0.5. The outer pair of switches S_{p1} and S_{p4} turns ON and OFF simultaneously, while the inner pair of switches S_{p2} and S_{p3} shares the same gate signal. The two pairs of the primary switches operate in the complementary manner. The two secondary-side switches S_{s1} and S_{s2} also act with 0.5 duty cycle complementarily. The phase-shift angle between the primary and secondary active switches is employed to control the output voltage and power. L_{Lk} stands for the transformer leakage inductance, which usually includes an external inductor if the practical leakage inductance is not large enough to realize the expected circuit operation.

The input series capacitors C_1 and C_2 have the same capacitance to clamp the primary switch voltage stress to half of the input voltage. V_P and V_S are the voltages on the primary side and the secondary side of the transformer, respectively. And i_p and i_s are the primary and secondary currents through the transformer with positive direction shown in Fig. 1.

The operations of the proposed converter are elaborated in this section. According to the work conditions of the primary current, the converter has two different modes of operation, namely continuous current mode 1 (CCM1), continuous current mode 2 (CCM2). Considering only half of the input voltage is imposed on the primary side of the transformer, in order to simplify the analysis, the gain G is defined as

$$G = \frac{2NVout}{Vin} \qquad (1)$$

where Vin, Vout, and N are the input voltage, output voltage, and transformer turns ratio n_1 / n_2, respectively.

III. OPERATIONAL MODES OF THE PROPOSED CONVERTER

A. *CCM1 Mode*

The key voltage and current waveforms in the CCM1 Mode are shown in Fig. 2. The corresponding equivalent circuit at every stage is illustrated in Fig. 3. As given in Fig. 2, ϕ is the phase-shift angle between the leading primary switches and the corresponding lagging secondary active switch. β is the time interval during which the primary current returns to zero after the primary active switches turn OFF. $\phi \geq \beta$ is met in the CCM1 mode.

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Mode 1 [θ_0 to θ_1]: During this interval, the primary current i_p flows reversely through S_{p1} and S_{p4}. The power is delivered from L_{Lk} to the input and the secondary side. The output voltage Vout is adversely addressed in the secondary side of the transformer. Due to the negative voltage across the leakage inductor, the current i_p declines rapidly, which is expressed as

$$ip = ip(\theta 0) + \frac{NVout}{Llk}(1/G + 1)(\theta - \theta 0), (\theta_0 \le t < \theta_1). \quad (2)$$

In the CCM1 mode

$$\beta = \theta_1 - \theta_0. \quad (3)$$

Mode 2 [θ_1 to θ_2]: At θ_1, i_p reaches zero and starts increasing linearly due to half of the input voltage across the leakage inductor. As i_p reverses, the secondary-side current is begins to circulate freely through S_{s1} and the antiparallel diode of S_{s2}. The voltage of both sides of the transformer is zero. The power is delivered from V_{in} to L_{Lk}. ip is regulated by

$$ip = ip(\theta 1) + \frac{NVout}{GLlk}(\theta - \theta 1), (\theta_1 \le t \le \theta_2). \quad (4)$$

In the CCM1 mode, i_p keeps increasing at this stage. As a result, the ZVS-on of S_{s2} is achieved naturally. There is not any extra condition to be satisfied for the ZVS-on operation of the secondary-side switches.

Mode 3 [θ_2 to θ_3]: S_{s1} turns OFF at θ_2 and C_{s1} is charged to Vout by is at the end of this stage. i_p is regulated by (4) until θ_3. And the phase angle ϕ is expressed as

$$\phi = \theta_3 - \theta_0. \quad (5)$$

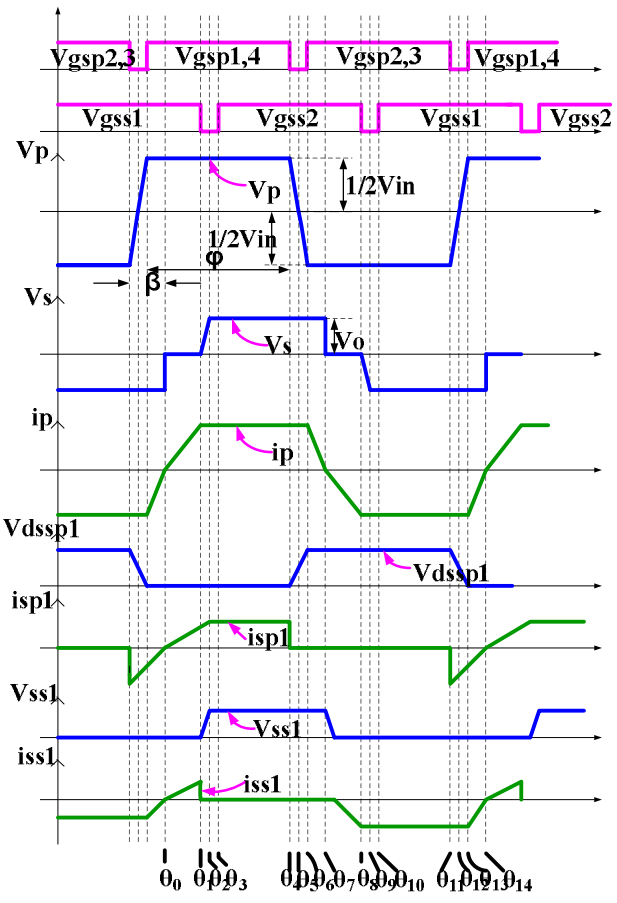

Fig. 2: Waveforms of CCM1 Mode

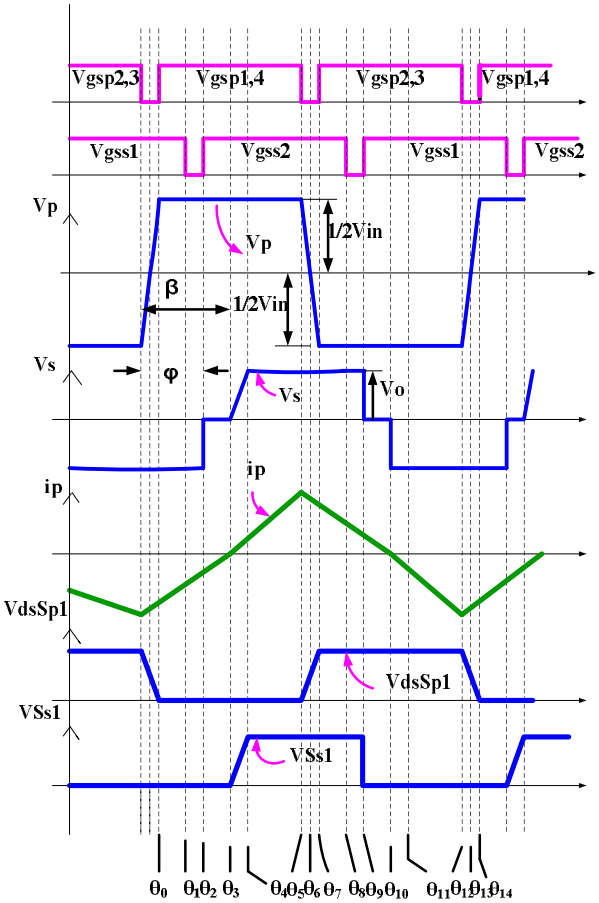

Fig. 3: Waveforms of CCM2 Mode

Mode 4 [θ_3 to θ_4]: When C_{s1} is charged to V_{out} at θ_3, D_{o1} becomes forward-biased i_s flows through D_{o1} and the body diode of S_{s2}, delivering the power from V_{in} to the load. Most of the power is transferred to the load during this stage which is named as the power-transferring stage. The primary current can be obtained as

$$ip = ip(\theta 3) + \frac{NVout}{Llk}(1/G - 1)(\theta - \theta 3), (\theta_3 \le t < \theta_4). \quad (6)$$

In the CCM1 mode i_p keeps constant during this stage, as shown in Fig. 2.

Mode 5 [θ_4 to θ_5]: At the beginning of this interval S_{s2} turns ON with ZVS and begins working in the synchronous rectification

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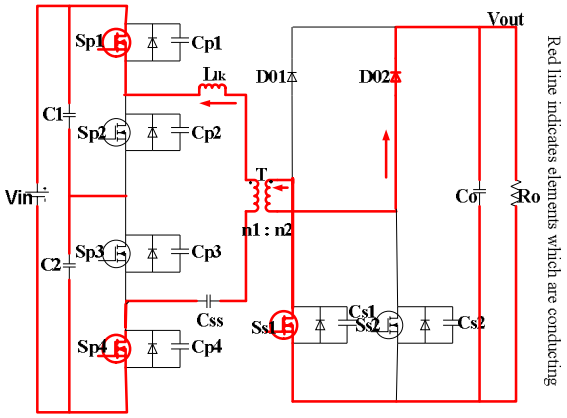
mode.

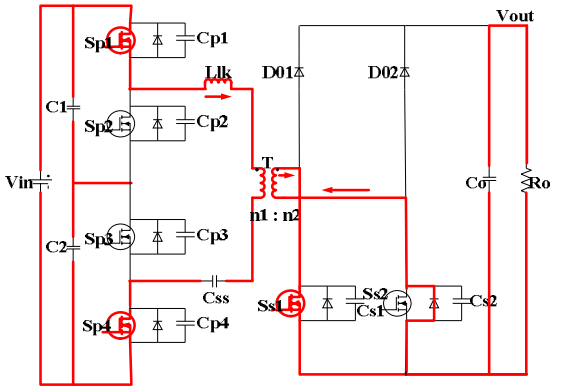
Mode 6 [θ_5 to θ_6]: At θ_5, S_{p1} and S_{p4} turn OFF. ZVS turn-off soft switching performance for S_{p1} and S_{p4} is achieved due to the parallel capacitors C_{p1} and C_{p4}. C_{p1} and C_{p4} are charged, while C_{p2} and C_{p3} are discharged by the primary current. All the parallel capacitors can be charged or discharged completely before S_{p1} and S_{p2} turn ON only if the energy stored in L_{Lk} is large enough.

Mode 7 [θ_6 to θ7]: When C_{p2} and C_{p3} are discharged completely, the antiparallel diodes of S_{p2} and S_{p3} are forward biased, which enables ZVS-on of S_{p2} and S_{p3}. The primary current decreases rapidly due to the negative voltage across L_{Lk}, which is the sum of $1/2V_{in}$ and NV_{out}. At the end of Stage 7, ip becomes negative but has the same absolute value as that at the beginning of Stage 1, which is expressed as

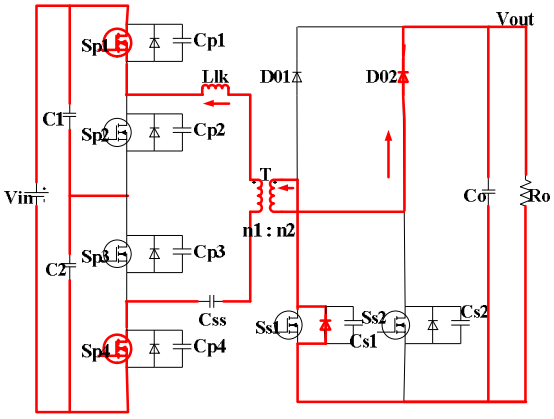
$$i_p(\theta_7) = -i_p(\theta_0). \quad (7)$$



(a)



(b1)



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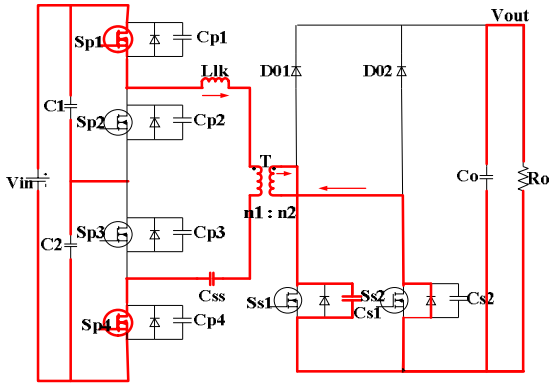

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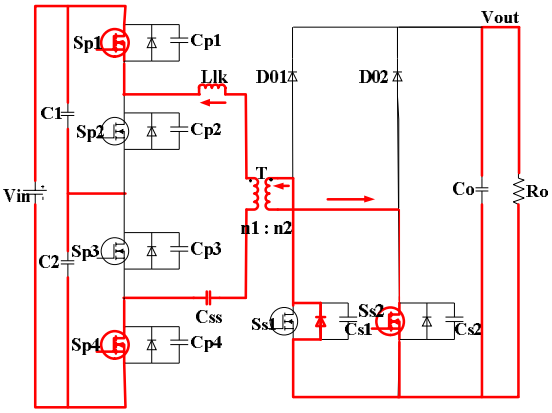

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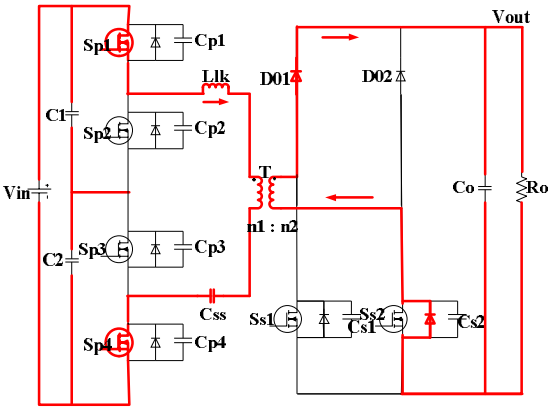

(d1)

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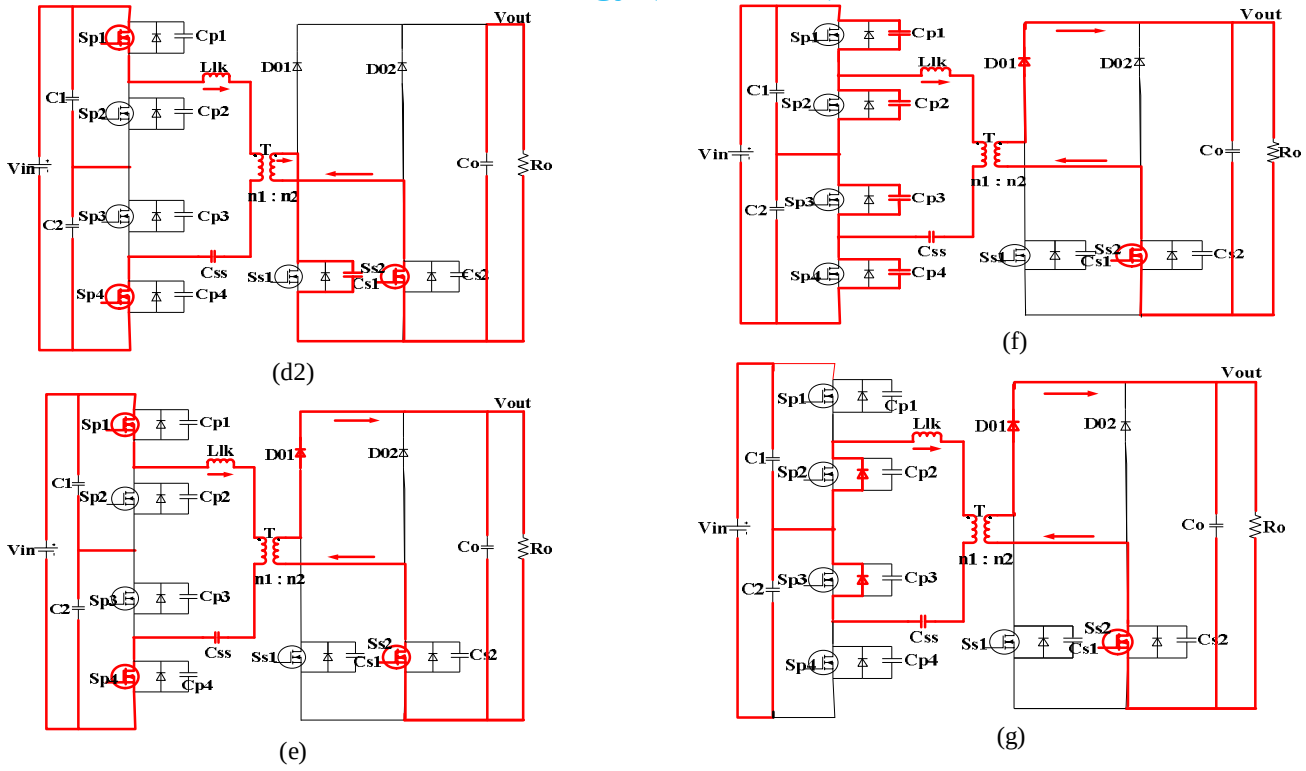

Fig. 3: Equivalent circuits in CCM1 and CCM2.
(a) Mode 1: θ_0 -θ_1. (b1) Mode 2 of CCM1: θ_1 –θ_2. (b2) Mode 2 of CCM2: θ_1 –θ_2. (c1) Mode 3 of CCM1: θ_2 –θ_3 (c2) Mode 3 of CCM2: θ_2 –θ_3. (d1) Mode 4 of CCM1: θ3 –θ_4. (d2) Mode 4 of CCM2: θ_3 –θ_4. (e) Mode 5: θ_4 –θ_5. (f) Mode 6: θ5 –θ_6. (g) Mode 7: θ_6 –θ_7.

B. CCM2 Mode

The above analysis of the CCM1 mode is based on the condition of $\phi \geq \beta$, which means the secondary-side semiconductor devices commutate after i_p returns to zero. If that is not the case, i.e., $\phi < \beta$, the circuit will enter the CCM2 mode. The key waveforms of the CCM2 mode are shown in Fig. 4 and the operational stages are illustrated in Fig. 3.

There are also 14 operational stages in a switching period of CCM2. The power transferring stage and the primary MOSFETs switching stages are similar to the CCM1 Mode, while the main difference between CCM1 and CCM2 can be observed in the secondary - side MOSFETs switching intervals. As a result, the stages 2-5 are analyzed in detail with the description of the other stages omitted.

Mode 2 [θ_1 to θ2]: Before i_p returns zero, S_{s1} turns OFF. The operation of the converter does not change, except that the current through S_{s1} changes to flow through the body diode. i_p is still regulated by (2), while the phase - shift angle is expressed as

$$\phi = \theta_2 - \theta_0. \quad (8)$$

Mode 3 [θ_2 to θ_3]: Before ip declines to zero, there is no current through the body diode of S_{s2}, and the voltage of S_{s2} still equals the output voltage V_{out}. As a result, S_{s2} turns ON with hard switching. Therefore, ZVS is lost for the secondary-side switches in CCM2. After turning ON of S_{s2}, the current through D_{o2} is shunted through S_{s2}. The secondary-side current circulates through S_{s1} and S_{s2} freely, and the secondary winding of the transformer is shorted. Therefore, the output voltage is decoupled from the transformer, and the load is supplied by only the output capacitor.

The primary current at this stage is also regulated by (4).With only half of the input voltage across the leakage inductor, the current falling rate is smaller compared to CCM1 and it takes longer time for ip to decline to zero. In addition, the power of the leakage inductor only returns to the input. As a result, less power is transferred to the load than CCM1 Mode during the intervals prior to the power-transferring stage.

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Mode 4 [θ_3 to θ_4]: As the primary current reverses, the parallel capacitor of S_{s1} is charged by the secondary - side current. And β can be expressed as

$$\beta = \theta_4 - \theta_0 \quad (9)$$

Mode 5 [θ_4 to θ_5]: Most of the power is transferred during this stage with i_p regulated by (6). This mode is the same as Mode 5 of CCM1 except that i_p is zero at the beginning of this stage. That is, $i_p(\theta_4) = 0$. As to the CCM1 mode, i_p larger than zero at the beginning of the power - transferring stage. Assuming G and V_{out} are the same for both the modes, it is clear that less power is transferred to the output terminal in CCM2 than in CCM1 during the power - transferring stage. In addition, as explained in Mode 3 of CCM2 mode, the converter transfers less power before the power - transferring stage. As a whole, less power is transferred in the CCM2 mode than the CCM1 mode during a whole period.

The CCM2 ode is not recommended for the practical applications. The secondary active switch turns ON before the primary current returns to zero. As a result, ZVS - on is lost for the secondary - side switches. And it costs longer time than CCM1 mode for the primary current to return to zero since the inductor voltage is only half of V_{in}. This results in extra power losses due to the secondary - side circulating current through S_{s1} and S_{s2}.

C. Converter Analysis

1) Soft - switching condition:

a) Primary Switches: The ZVS turn - off of the primary switches is obtained due to the parallel capacitors. The larger the parallel capacitors are, the less turn - off losses would be caused. In the steady state operation of CCM1 and CCM2, ZVS turn - on is achieved for all the primary power MOSFETs, which reduces the switching losses greatly. When S_{p1} and S_{p4} turn OFF, the inductor L_{Lk} charges C_{p1} and $C_{p4,}$ and discharges C_{p2} and $C_{p3.}$ As a result, the ZVS turn - on for the switches S_{p2} and S_{p3} can be realized once C_{p2} and C_{p3} are discharged completely. The condition for the ZVS turn - on of another pair of primary switches is the same.

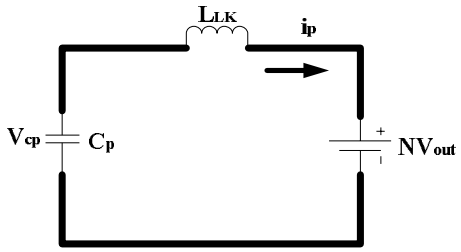

Fig. 5: Primary referred equivalent circuit when primary switches turn OFF.

Fig. 5 shows the primary referred equivalent circuit after a pair of primary switches turn OFF. C_p is equal to one parallel capacitance of the primary switches, assuming the four parallel capacitors are all the sae. That is $C_p = C_{p1} = C_{p2} = C_{p3} = C_{p4.}$ And V_{cp} equals to 0.5 V_{in} when the primary switches turn OFF. Since the output capacitor is relatively large, the output voltage is assumed constant during this short duration.

b) Secondary Switches: The ZVS of the secondary-side switches is achieved naturally in CCM1. No extra condition has to be satisfied for ZVS-on of the secondary-side switches. In CCM2, however, ZVS is lost because the secondary-side switch turns ON before is declines to zero.

2) Voltage stress analysis: Once ignoring the voltage ripple on the input capacitors, the voltage stress of the primary power switches is half of the input voltage, which means the low-voltage rated power devices with superior performance can be employed to reduce the conduction losses. Since there is no filter inductor in the secondary rectifier circuit, the turn-off voltage across the secondary-side switches is clamped by the output voltage, and the voltage spikes on the switches are effectively suppressed. Therefore, the voltage stresses of the secondary-side switches including the MOSFETs and diodes are just the output voltage. The low-voltage rated MOSFETs and diodes could be adopted as the secondary-side power switches, which help the converter accomplish better performance.

IV. SIMULATION RESULTS OF PROPOSED THREE LEVEL DC/DC CONVERTER

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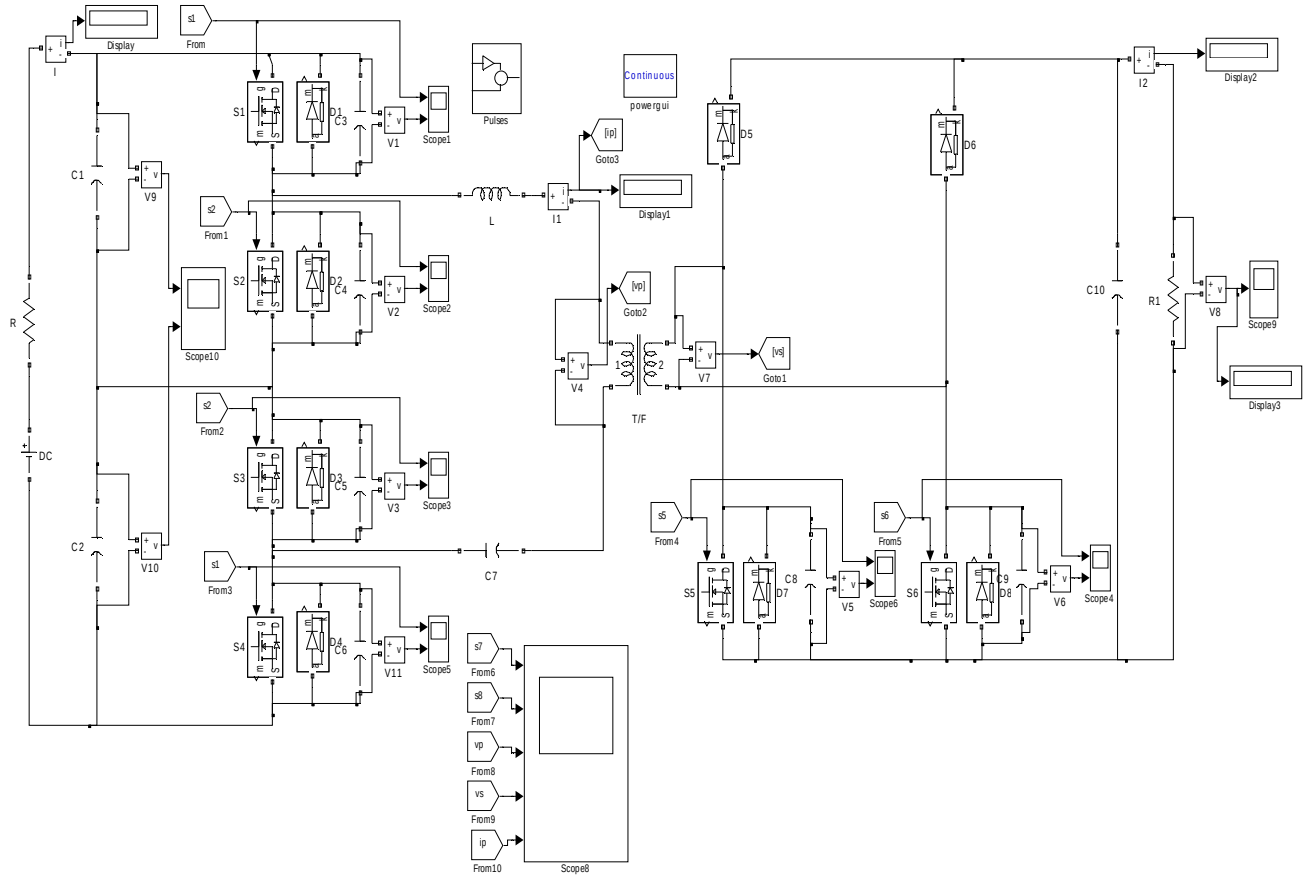

Fig. 6: Simulink diagram of Two to Three-Level DC-DC converter.

Fig.6 Shows the Simulink model of the proposed converter. The proposed converter consists of six switches namely S1, S2, S3, S4, S5 and S6. All the switches are operated with same duty cycle. The parameters used in simulation as shown in table1.
In the proposed converter there are total six switches, all of them are operated under ZVS condition in order to reduce the switching losses. The outer pair of switches (S_1 & S_4) shares the same gate signal where inner pair of switches (S1 & S3) shares the same gate signal. The voltage of transformer primary side is two level and secondary side is three level. The voltage waveforms of the transformer primary and secondary side are as shown in fig. 7.

Table 1

Components	Parameters
V_{in} (input voltage)	200
f_s (switching frequency)	1 kHz
L_{Lk} (primary transformer leakage)	50 µH
C_{p1} - C_{p4}	4.7 nF
C_{s1} - C_{s2}	4.7 nF
C_{ss} (block capacitor)	50 mF
C_o (output capacitor)	5000 µF

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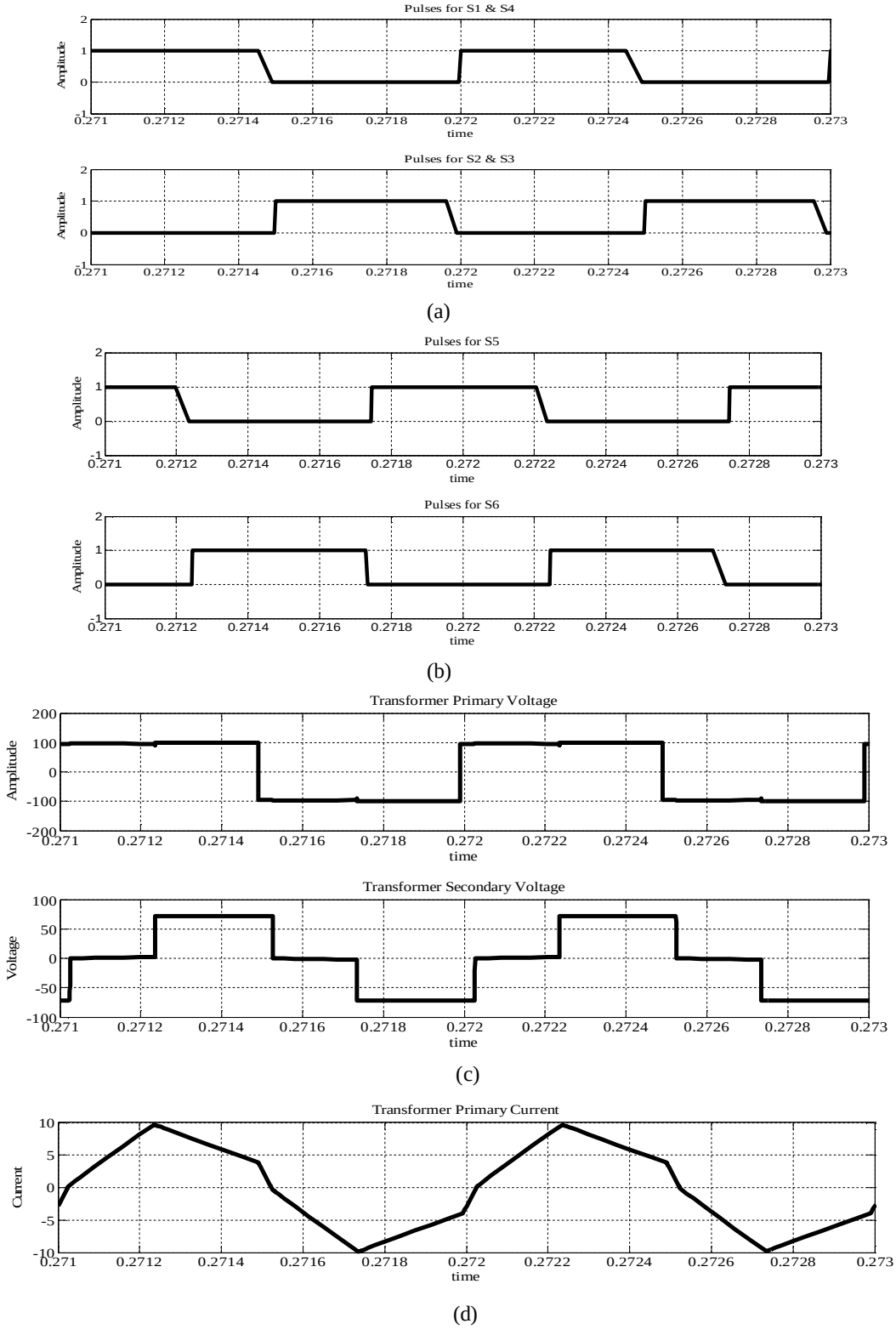

Fig. 7: (a) Pulses for S_1 & S_2 (b) Pulses for S_5 & S_6 (c) Transformer primary & secondary voltage (d) Transformer primary current

Fig. 8 represents soft switching of the proposed converter for S_1 and S_4 switches. Fig.8a shows voltage across S_1, Fig. 8b shows the ZVS for S_1 from off to on & Fig. 8c shows on to off of S_1 under the ZVS.

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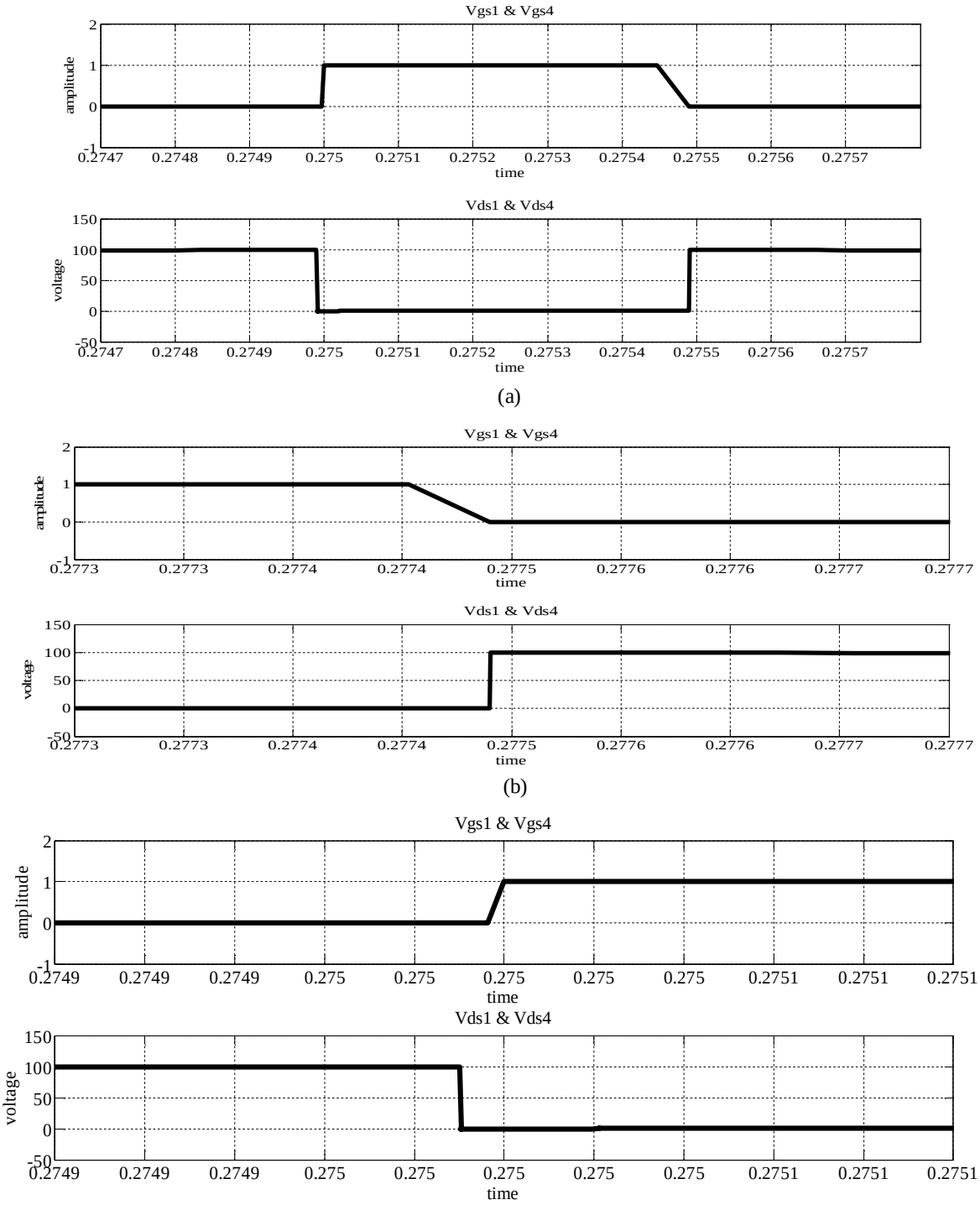

Fig.8: (a) Voltage across switch S_1 (b) ZVS turn off- on S_1 (c) ZVS turn on-off S_1.

Fig. 9 represents soft switching of the proposed converter for S_2 and S_3 switches. Fig.9a shows voltage across S_1, Fig. 9b shows the ZVS for S2 from off to on & Fig. 9c shows on to off of S_2 under the ZVS.

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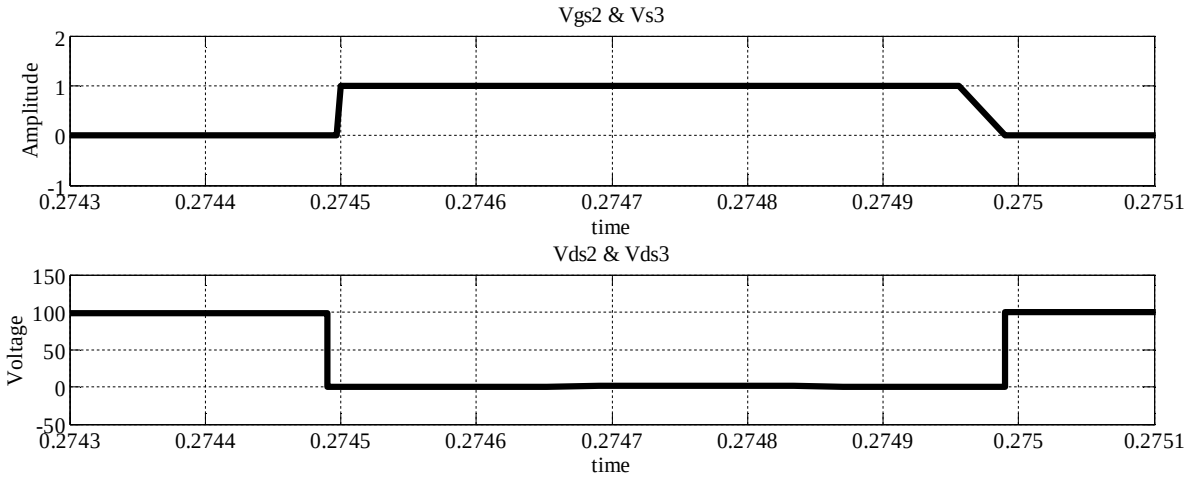
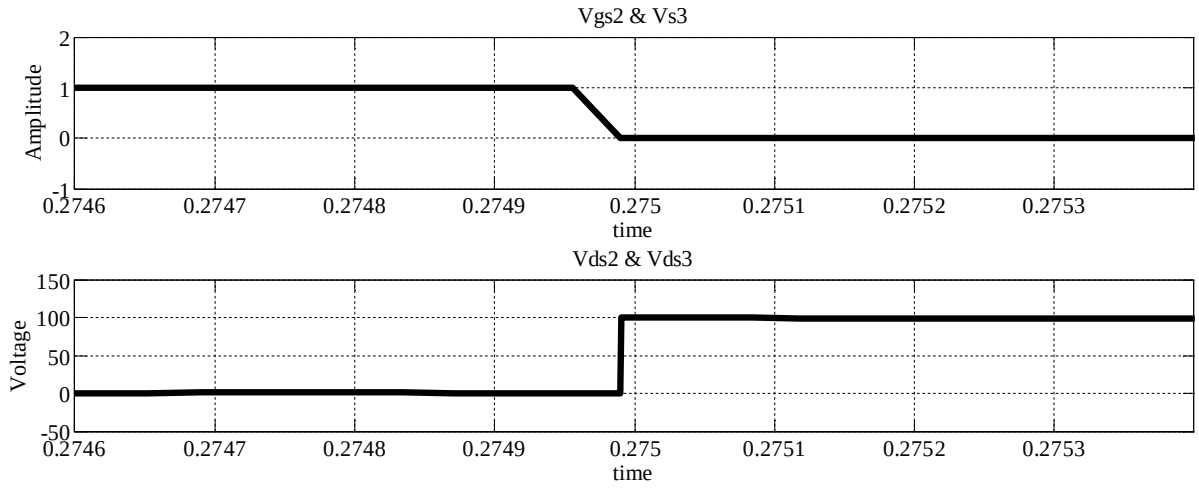


(a)



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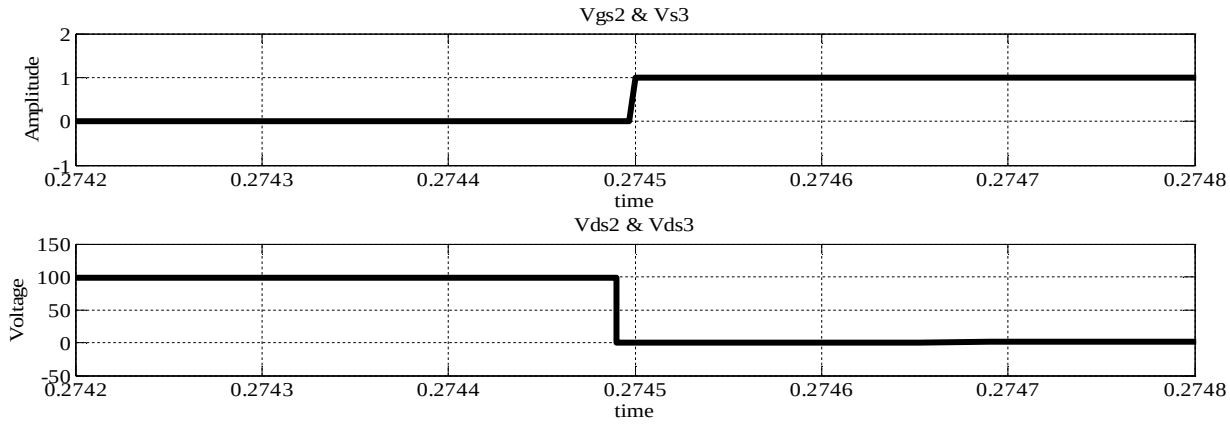

(c)

Fig.9: (a) Voltage across switch S_2 (b) ZVS turn off- on S_2 (c) ZVS turn on-off S_2.

As the Load current increases then the efficiency decreases as shown in table2. Fig. 10 shows graph between efficiency and

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load current, which will also represents the efficiency is high for with soft switching than without soft switching for CCM1 Mode. Fig. 11 shows the rectifier output volatge in CCM1 Mode.

Table 2

S.no	Load Current	Efficiency With Soft Switching	Efficiency Without Soft Switching
1	7.14	89.98	81.27
2	7.458	88.64	79.54
3	7.812	87.73	78.23
4	8.20	87.01	77.42
5	8.64	86.21	75.88
6	9.13	85.43	74.93
7	9.68	84.68	73.34

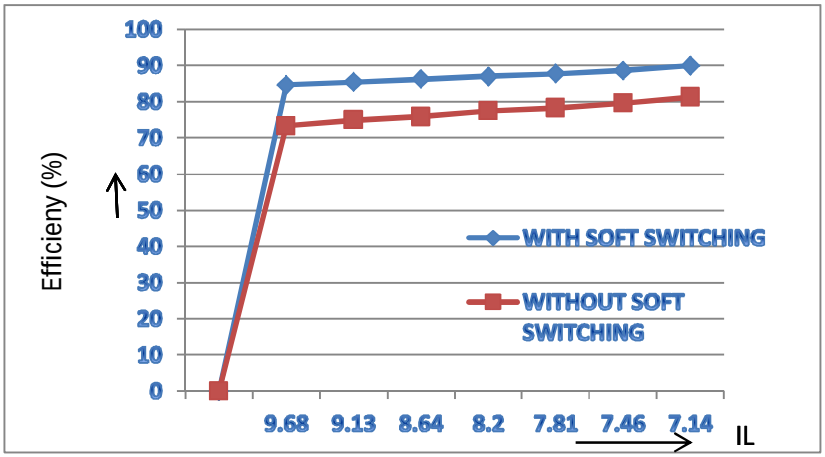

Fig. 10: Load Current vs Efficiency

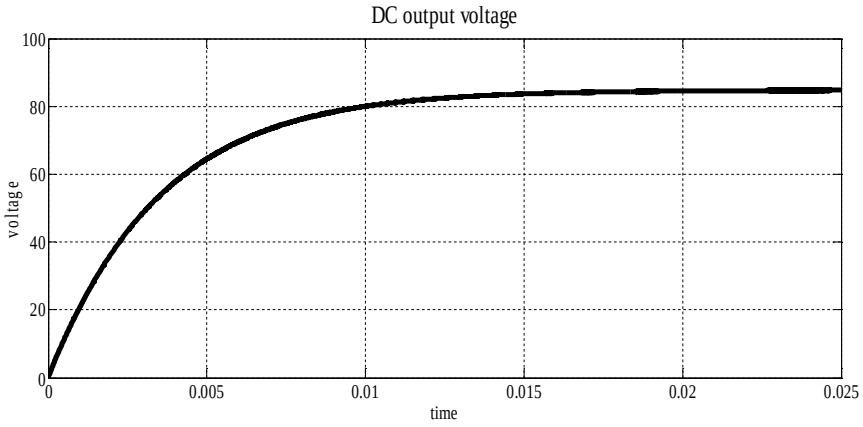

Fig. 11: Rectifier output voltage

V. CONCLUSION

In this paper, a secondary-side phase-shift-controlled ZVS dc/dc converter for high-efficiency has been proposed and analysed. The improved three-level configuration in the primary side halves the primary power devices, which makes it possible to employ low-voltage rated power switches for high input voltage applications. Furthermore, the ZVS can be achieved for all the

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power devices including the primary and secondary switches to effectively reduce the switching losses. And the overshoots on the secondary side devices are effectively suppressed by clamping the rectifier to the output voltage.

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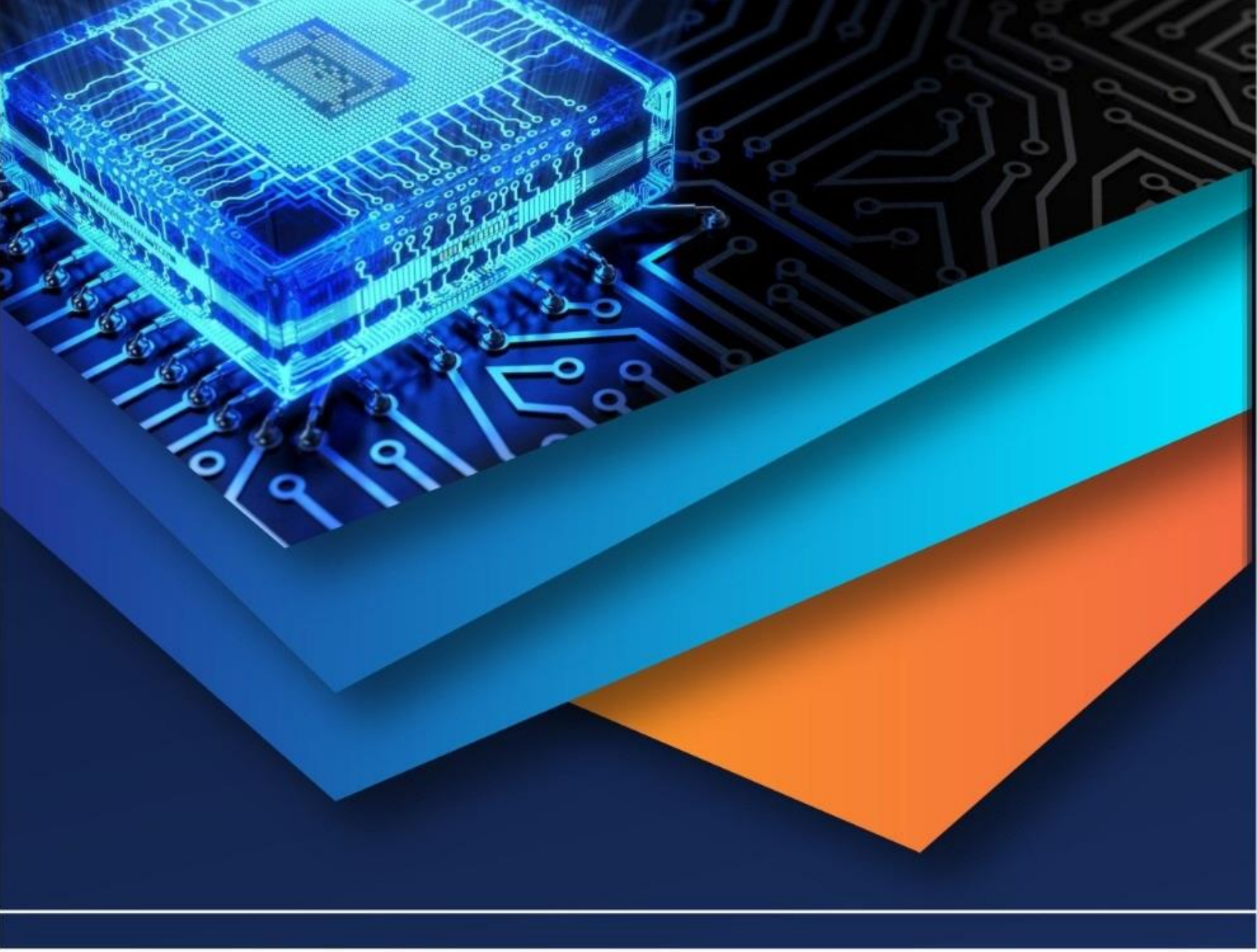

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