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2D-DCT Computations: A Review

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Abstract: In today's scenario, there is large involvement of transformations. These scenarios include digital signal processing and image processing. It is essential in all sectors. Transformation techniques are useful as it makes analysis easier, reliable and relevant. The response to any particular input could have been computed in the time domain, but it takes much more computations and not be as intuitive therefore this signal should convert to the frequency domain. There are various transformations tools used namely FFT, DFT, DCT, DWT, etc. DCT defines a finite sequence of data points regarding a sum of functions oscillating at different frequencies. 1-D DCT is directly extended to form 2-D DCT. 2D-DCT algorithms are computation intensive and involve a large number of multiplication, and addition operations and due to this chip area gets increased and performance gets degrade. Hence it is required to make 2D DCT computations efficient.
Keywords: DSP, DCT, Processors

I. INTRODUCTION

It has been seen that there is continuous growth in customer's demand for high standard information technology due to its quick response. The increase in the use of digital signal processing depends on increase in the use computers. Three domains are used in digital signal processing for a signal representation. These domains are namely time domain/spatial domain, frequency domain, and wavelet domain. A signal can be describing in any one of the domain which represents the necessary characteristics information of the signal, but if we required extra details of the signal then this signal represents in an only time domain is not sufficient hence signal has to represent in the frequency domain. Frequency domain also called spectral analysis in which divides the spectral components of the signal to give a small and meaningful form of signal representation. There are many frequency domain transformations like FFT, DFT, DCT, and DWT. But only DCT having strong 'energy compaction' property DCT is frequently used in signal and image processing. The implementation of a 2D-DCT fast reconfigurability, provide the possibility of swapping in and out designs in the time domain, so that a designer can meet requirements, with a minimum amount of resource. In regular DCT, a 64 multiplications and 56 additions required for 8 point 1-D DCT, and 1024 multiplications and 896 additions required for 8 point 2-D DCT, due to these enormous number of computations there is increase in number of length of the DCT, the number of multiplication and addition operations also increase leading to larger chip area and performance degradation. When a large number of mathematical computations are required, then the primary feature of the 2-D DCT computation is to compute the DCT coefficients. To minimize the complexity of operations as much as possible with maintaining low delays and high-speed throughput is one of the main objectives. More and more embedded systems are using nowadays, for hardware to control and process data by making use of parallelism and flexibility concepts. The need of powerful computation is increasing rapidly. When there is a need of upgradation in the processing power of a computer, the first thing should be considered, the processor's operational frequency. Therefore, it is essential to design such a system with parallelizing tasks or algorithms to boost performance and simultaneously reduce resource footprints using multi-core processing.

II. LITERATURE SURVEY

Mariem Makni [1] this paper proposes the Comparison and Performance Evaluation of FPGA Soft-cores for Embedded Multi-Core Systems. This paper presents a big challenging task for designers to select the most efficient and proper soft-core processor for a respective software application. They compute and compared the performance of existing soft-cores which presents a big challenging task for designers to select the most efficient and proper soft-core for a respective software application. It describes an overview of soft-core processors that have been used in embedded systems. This technology compares different open-source and commercial soft-cores such as open Fire, LEON3, Micro blaze, etc. based on architectural features. They also evaluate the total execution time and area consumption of FPGA affected by the selected soft-core processors using various applications.

The second system designed by Ravi Jani1, Kunjal Mehta [2] Fast Fourier Transform implementation using Microblaze and uclinux, states that in certain multimedia and signal processing application the FPGA's computational capacity proves to be inefficient. To overcome this limitation, the designers have developed the number of methods. Out of that two of the approaches have been implemented. One is a hardware-based approach, and other is a software-based approach. To enhance the performance of System on

Chip the hardware-based approach is resorting to multiprocessor architecture. Another approach which is software -based is useful if the hardware capacity of the FPGA is limited.

F. Cariccia P. Cariccia [3] Multimedia SoC: A Systolic Core for Embedded DCT Evaluation this paper describes that, reconfigurable systolic 2D-DCT architecture has been proposed and hardware implementation results on XILINX Vertex-E FPGA are given. As far as performance is concerned this core can to process 128 XGA (1024 × 768) frames/s running at 110 MHz it is estimated that systolic DCT architectures seem to be well suited for FPGA implementation, especially when high throughput is looked for.

The system proposed by D.W. Trainor, J.P. Heron and R.F. Woods [4] presented a novel FPGA i.e., Xilinx XC6200 series implementation of a 2D (8x8) point DCT. It has shown the development of an appropriate architectural style can produce high-quality circuit designs for respective technology. To produce DCT implementation on a single chip FPGA, they used distributed arithmetic and exploitation of parallelism and pipelining. FPGA operated at 25 frames per second with VGA resolution. This technology was appropriate for processing image data at 25 frames per second.

M. Thiruveni Raguraman, D. Shanthi Saravanan [5] this paper implement FPGA Implementation of Approximate 2D Discrete Cosine Transforms goal to contribute to the efforts of design discrete cosine transform (DCT) is frequently. To reduce the circuit complexity, it is enough to produce equities outputs rather than precious outputs. Numbers of applications like image and video processing required higher dimensional DCT algorithms. For analyzing the accuracy and performance, the approximate 2-D DCT architectures, are coded in Verilog, simulated in Modelsim, synthesized and implemented in virtex E Field Programmable Gate Array kit. For comparative analysis of approximate 2D DCT architectures speed and area are considered.

A bdessalem Ben A bdelali [6] Efficient Binary DCT hardware architecture exploration and implementation on FPGA. This paper describes a huge design exploration of this module to be performed. At first, a detailed study of the Binary-DCT, which is decomposed in a multi-stage architecture, is carried out. Various architectures of the whole 2D-Binary DCT are developed by exploring different Binary-DCT stage hardware implementation solutions. These architectures to be obtained by combining the different implementation solutions of the Binary-DCT stages. The timing of the explored solutions to be determined by taking into account the stages pipeline and the coefficient calculation order. This latter to be fixed in the manner of ensuring the best latency while avoiding data dependency violation.

S.E. Tsai, and S.M. Yang [7] A Fast DCT Algorithm for Watermarking, this paper proposes fast discrete cosine transform (FDCT) algorithm that used the energy compactness and matrix sparseness properties in a frequency domain to achieve efficient computation performance. For a JPEG image of 8×8 block size in a spatial domain, the algorithm separates the 2D DCT into one pair of 1D DCTs with transform computation in only 24 multiplications. The 2D spatial data is a linear combination of the base image which is obtained by the outer product of the column and row vectors of a cosine function. Implementation of the FDCT algorithm shows that embedding a watermarking image of 32×32 block pixel size in a 256×256 digital image can be completed.

Ankita Selokar, A.C. Kailuke [8] FPGA Implementation of Forward 2D-DCT and Inverse 2D-DCT Based On Row-Column Decomposition Method. This paper represents the FPGA implementation of 2D forward DCT and inverse DCT. 2D-DCT to be computed by combining two 1D-DCT pairs that connected by a transpose buffer. Firstly, implemented the forward 1D-DCT row-wise operation that requires addition, subtraction, registers and multipliers, and then column-wise operation. For inverse 1D-DCT they execute 1D-DCT first column-wise and then row-wise. It possesses features and thus well suited for VLSI implementation. It has been used for the computation of either the forward or the inverse 2D DCT. Then synthesized onto a Xilinx14.2 ISE device.

Shahrukh Agha and Farman ullahJan [9] DCT and Motion Estimation. This paper describes a multiprocessor system especially for FFT algorithms based on shared memory multiprocessing system and multistage interconnection. It presents a theoretical analysis for the speeding up FFT algorithm (1D and 2D). Implementation of multiprocessing system is presented in this technology. As compared to a single processor, multiprocessing approaches also appear efficient regarding power at the same throughput at the cost of more area, e.g. as compared to single processors, running multiple processors at low frequency is power efficient in case of 2D DFT and 2D DCT, at a higher frequency. It has also shown that different ways of parallelizations or mapping.

S. Varkeessheeba [10] Performance Evaluation of Various Discrete Cosine Transforms this paper proposes; many DCT algorithms were proposed to achieve high-speed DCT and low power consumption. CORDIC algorithm have been widely used in Software Defined Radio, wireless communications, and medical imaging applications. The algorithm is very much hardware efficient because it performs a combination of shift-add operations and filters the dependence on multipliers. In the Digital Signal Processing, this paper explains the CORDIC algorithm and various DCT performances and compares the performance of various discreet cosine transforms regarding power consumption and accuracy.

Transformations	Power consumption
DCT	1.058 W
1D DCT	13.1 W
2D DCT	2.488
DA based DCT	5.78
CORDIC	0.184

Table1: Power analysis of various transformations

III.CONCLUSIONS

After review from the above-mentioned sources, it seems that many researchers have implemented 2D- DCT for various applications using a single core system on a chip. In today's world, transformation techniques are very beneficial it makes understanding the problem easier in one domain than in another and making analysis reliable. But 2D-DCT demand huge computations which require large memory space and high processing time which is not feasible to overcome these problems. Using multi-core processors, such systems can be integrated on a single FPGA chip, assuming that the soft-core processor provides adequate performance.

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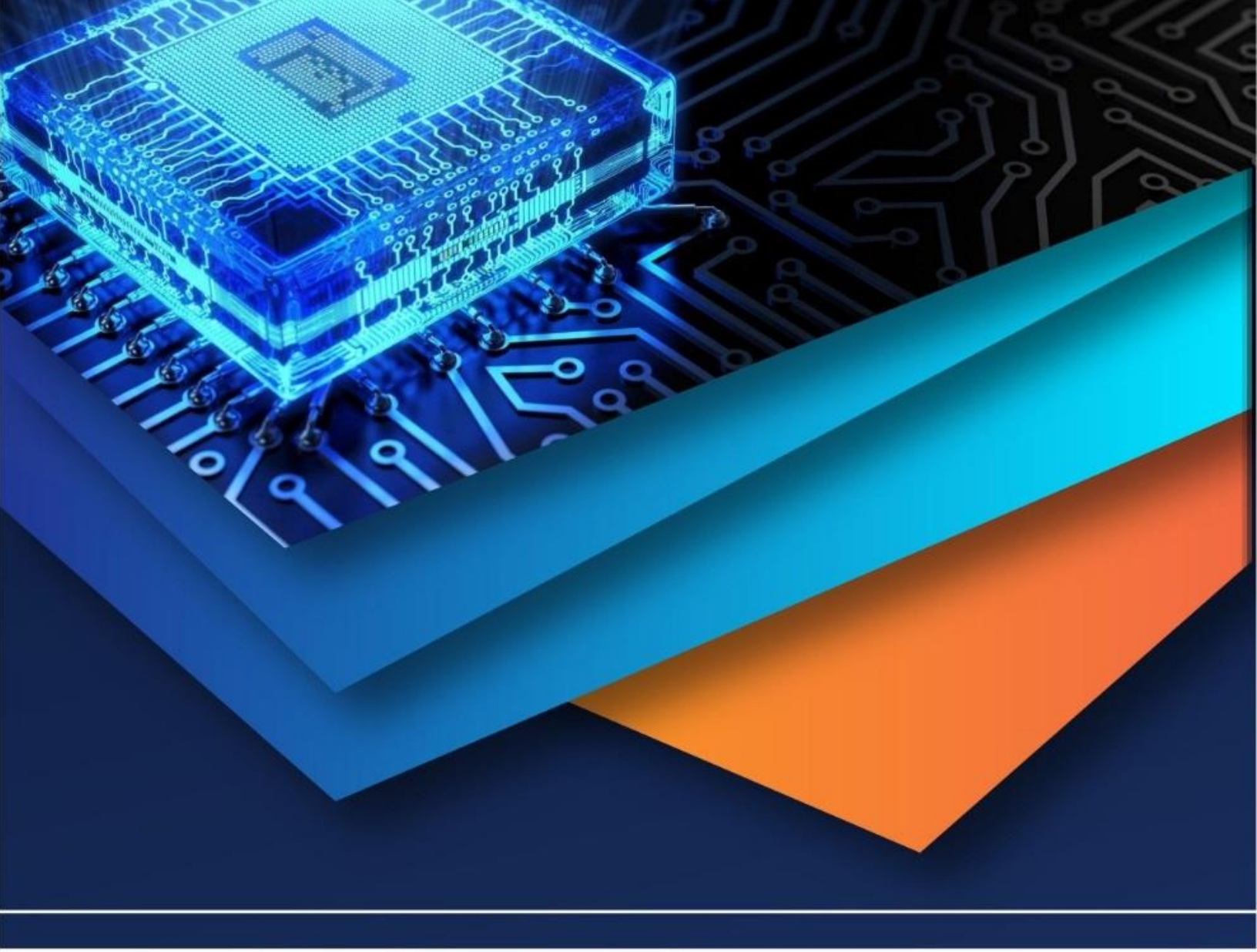

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