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Designing of Parallel to Serial Converter and Flash ADC using Reversible Gate

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Abstract: ***The Reversible Logic maps unique input to the output and ensure one to one mapping. This logic is used in emerging applications like low-power design, quantum computation, optical computing, bioinformatics and nanotechnologies. In communication between devices, the design of Parallel to Serial Converter plays an essential role as data bits in encoded form are transmitted serially rather than in parallel. This work understands and nurtures the necessity of reversible logic for future revolutionary computing and communication technologies. Among the reversible gates designed, Fredkin Gate is considered to be the universal gate which has a quantum cost of 5 and garbage outputs of 6. This work aims at reducing the quantum cost by using DRG4 Gates whose quantum cost is 4 and garbage outputs are 2. Using this reversible logic, the parallel to serial converter is designed to operate at 50MHz. The designs are coded in VHDL using structural modeling. These are synthesized and simulated in Xilinx ISE Design Suite 14.5. The results are compared for various parameters and the proposed design is found to be a better choice of implementing the parallel to serial converter practically due to less quantum cost, area, power dissipation, garbage outputs, etc. As a further extension work, the work is carried out for Analog to Digital Converter for Flash ADC and the proposed design is found to be a better choice to implement in Reversible Logic with less quantum cost, area, power dissipation, garbage outputs, etc.***

I. INTRODUCTION

The ever growing demand of high end computing applications has posed the challenge of continuous technology up gradation. The up gradation in technology has enabled the complex applications like Cloud computing, Real-time transitions on huge databases, Biotechnological computations a reality. Technological advancements in terms of higher operational frequency and miniaturization of chip in recent years have generated sufficient computing power to enable this growth. As predicted by Gordon Moore in 1960, popularly known as Moore's law, the transistor count in a chip will be double every one and half year on the average. Transistor growth is shown by Gordon Moore in figure 1.1. ITRS (International Technology Roadmap for Semiconductors) has also drawn a road-map of required feature size in future at atomic level in 2050. Shrinking in feature size resulted in a number of implementation and operational difficulties like heat dissipation, requirement of very thin laser beam, clock distribution etc.

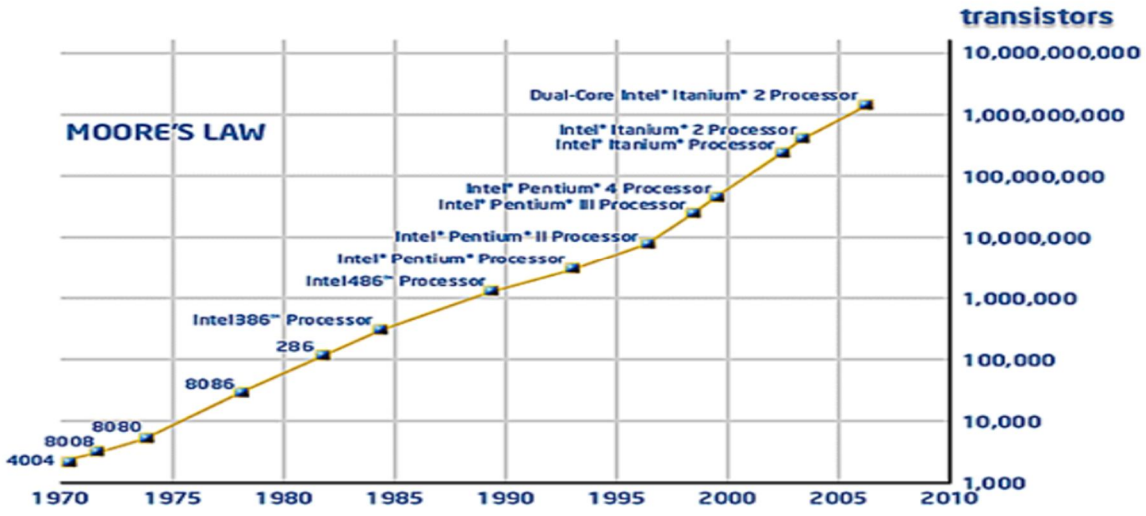

Figure 1: Moore Law's Graph for Transistors

Current technologies are finding it difficult to continue with the required level of growth. Alternative technologies are emerging to take place so that the growth momentum can be continued. Reversible computing is one of the computing system in which new generation computing system can be designed. Because of its basic nature of reversibility, it retains the old information and reduces dissipation of heat in its operation.

II. LITERATURE SURVEY

Reversible computing is emerging as a potential development platform to replace conventional logic. Here represents previous work on reversible logic.

A. *Reversible Logic Gates*

Right from the stored program architecture given by John Von Neumann in 1949, heat dissipation per computation of bit is being estimated. R. Landauer [1961] pointed out that the irreversible erasure of a bit of information consumes power and dissipates heat. While reversible designs avoid this aspect of power dissipation. Destruction of bits causes heat dissipation as per Landauer Principle. Bannett in 1973 proposed a turning machine for loss-less computation by making it reversible. The development of reversible gates and circuits started after Toffoli proposed reversible logic gates in 1977. A number of gates have been proposed thereafter. The same has been described two categories namely basic gates and generalized gates.

Two constraints for reversible logic synthesis are:

1) Feedback is not allowed

2) Fan-out is not allowed (i.e., fan-out = 1).

A gate with k inputs and k outputs is called a k*k gate. Several reversible gates have been proposed over the last decades.

B. *Reversible Circuit Design*

Toffoli, Fredkin and Peres have given their reversible gates in 1980's; these gates are used to implement the Boolean functions. Network of reversible gates to implement the specific Boolean function is called reversible circuits. Formally a combinational reversible circuit is an acyclic combinational logic circuit in which all gates are reversible and interconnected without explicit fan-out's and loops.

III. OBJECTIVES

A. Multiple Comparative Analyses of Reversible Gates for Designing Logic Circuits

B. Designing parallel to serial converter using DRG4 gate

C. Designing of ADC convertor using DRG4_ gate

IV. FREDKIN GATE

The Fredkin gate (also CSWAP gate) is a computational circuit suitable for reversible computing, invented by Edward Fredkin. It is *universal*, which means that any logical or arithmetic operation can be constructed entirely of Fredkin gates. The Fredkin gate is a circuit or device with three inputs and three outputs that transmits the first bit unchanged and swaps the last two bits if, and only if, the first bit is 1.

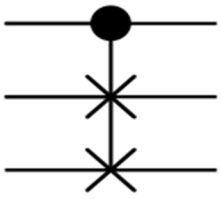

Fig No. 2 Circuit representation of Fredkin gate

The basic Fredkin gate is a controlled swap gate that maps three inputs (C, I_1, I_2) onto three outputs (C, O_1, O_2). The C input is mapped directly to the C output. If $C = 0$, no swap is performed; I_1 maps to O_1, and I_2 maps to O_2. Otherwise, the two outputs are swapped so that I_1 maps to O_2, and I_2 maps to O_1. It is easy to see that this circuit is reversible, i.e., "undoes" itself when run backwards. A generalized $n \times n$ Fredkin gate passes its first n-2 inputs unchanged to the corresponding outputs, and swaps its last two outputs if and only if the first n-2 inputs are all 1. The Fredkin gate is the reversible three-bit gate that swaps the last two bits if, and only if, the first bit is 1.

A. Reversible Logic based Parallel to Serial Converter Design

The three bit counter is constructed with the help of three toggle flip-flops. A variety of counter circuits of various types of complexities are viable in IC form. The design of Reversible T-Latch is carried out the combination of Peres Gate and Feynman Gate as shown in figure 2.5.

The higher order design of 32-bit Parallel to Serial Bit conversion is performed in this work by using DRG4 Gate. The 32-bit multiplexer is designed as shown in figure 2.4.

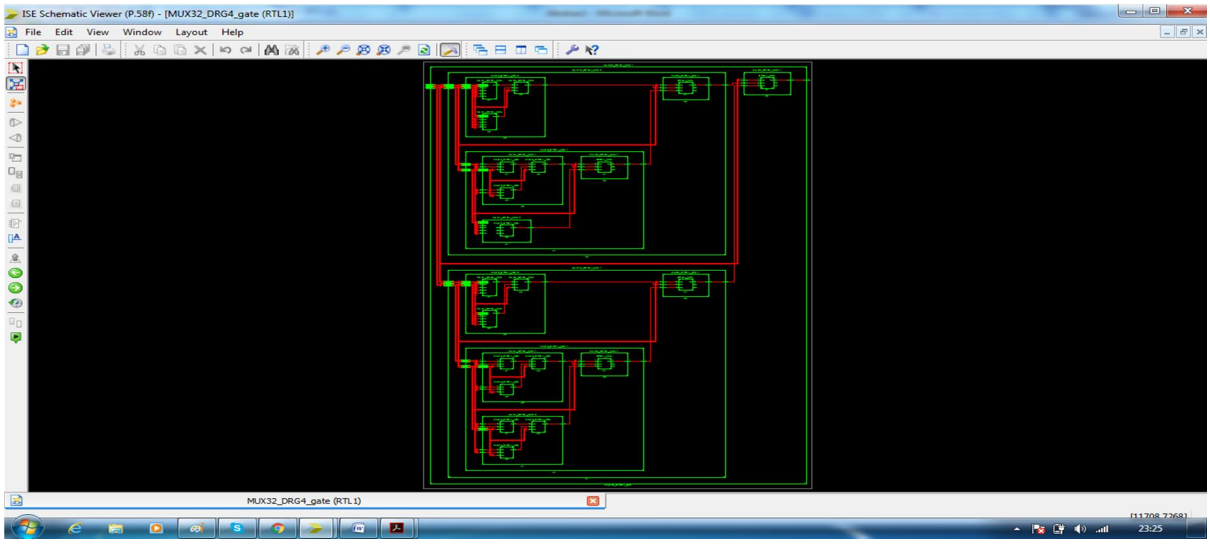

Figure 3: Design of 32-Bit Multiplexer using DRG4 Gate

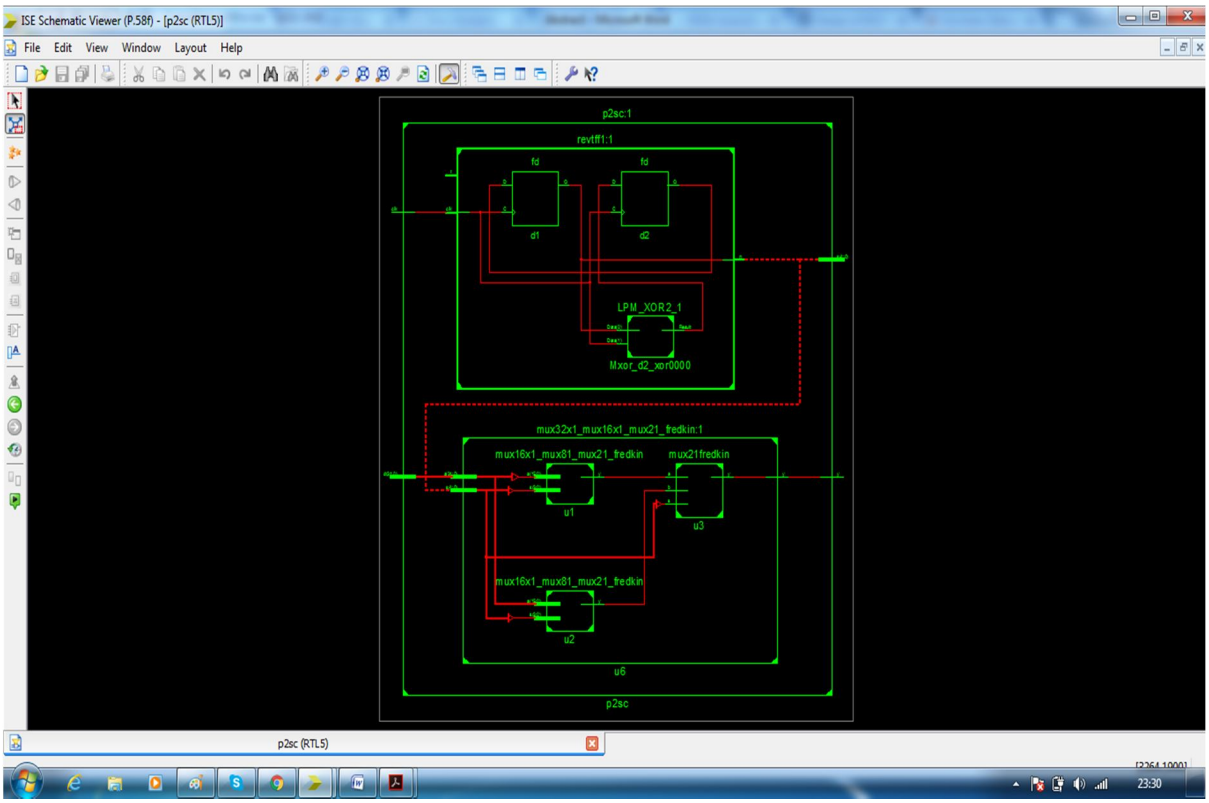

Figure 4: Design of Parallel to Serial Converter using Reversible T-Latches and DRG4 Gate based 32x1 Multiplexer.

The design of finally implemented parallel to serial converter using the reversible logic based on Fredkin Gate, Feynman Gate, and Peres Gate is shown in figure 2.5.

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V. SYNTHESIS RESULTS

The synthesis results include Design Summary, RTL Schematic, Technology Schematic, FPGA Floorplan and Routing and Power Analysis Report for Parallel to Serial Converter using DRG4 Gate as shown in figures 5 to 13.

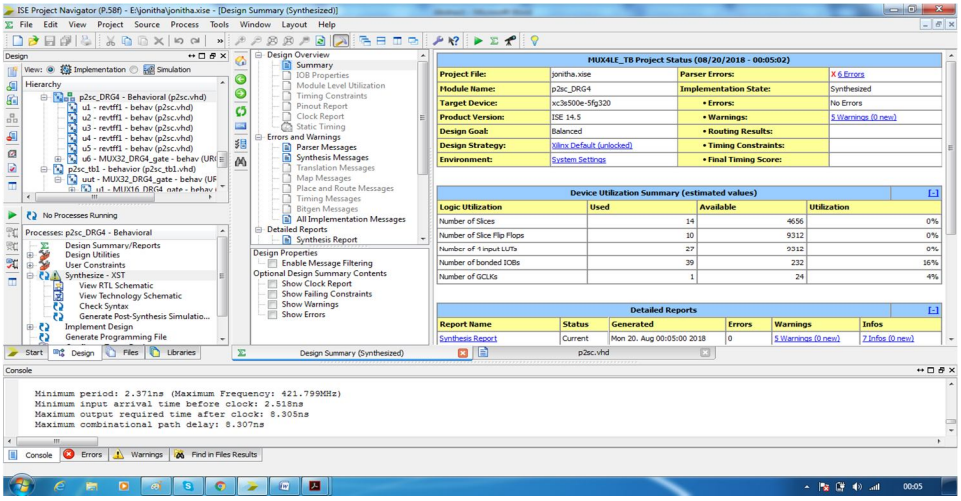


Figure 5: Design Summary of Parallel to serial converter using DRG4 gate

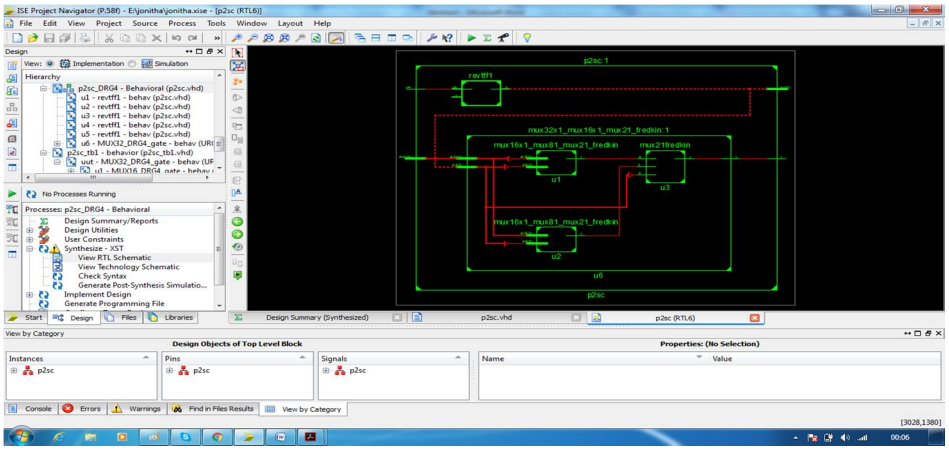


Figure 6: RTL Schematic of Parallel to Serial Converter using DRG4 gate

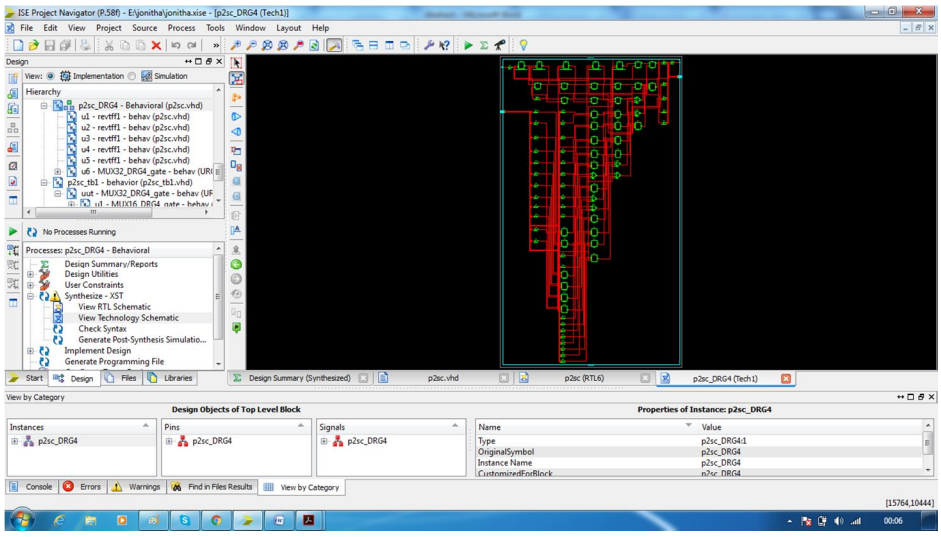


Figure 7: Technology Schematic of Parallel to Serial Converter using DRG4 gate

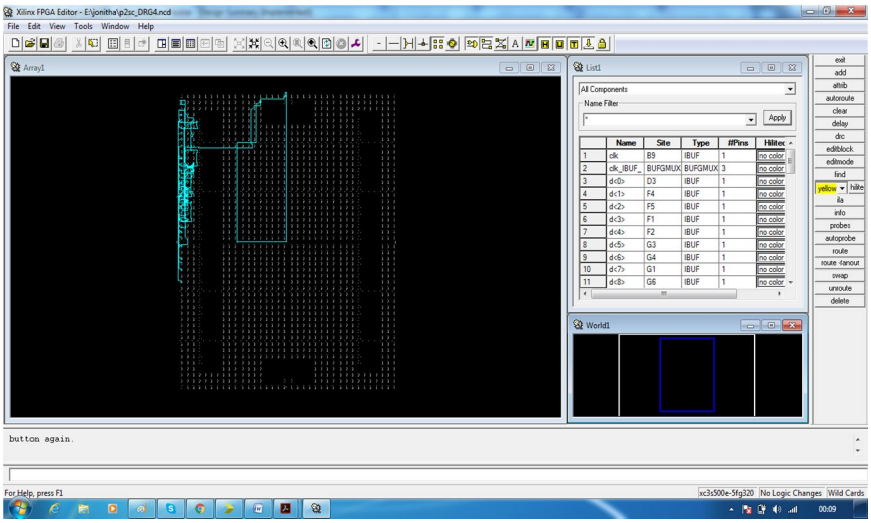


Figure 8: Floor plan and Routed Design of Parallel to Serial Converter using DRG4 gate

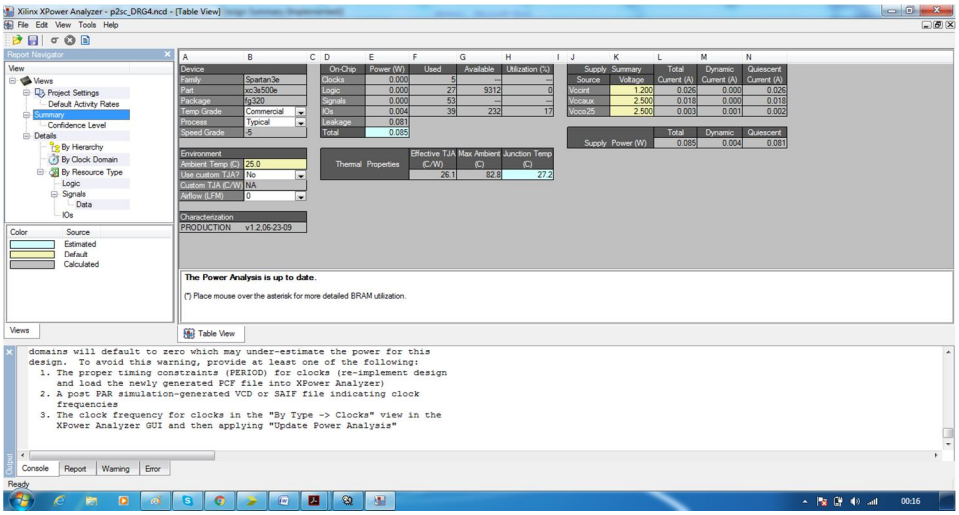


Figure 9: Power Report Summary of Parallel to Serial Converter using DRG4 gate

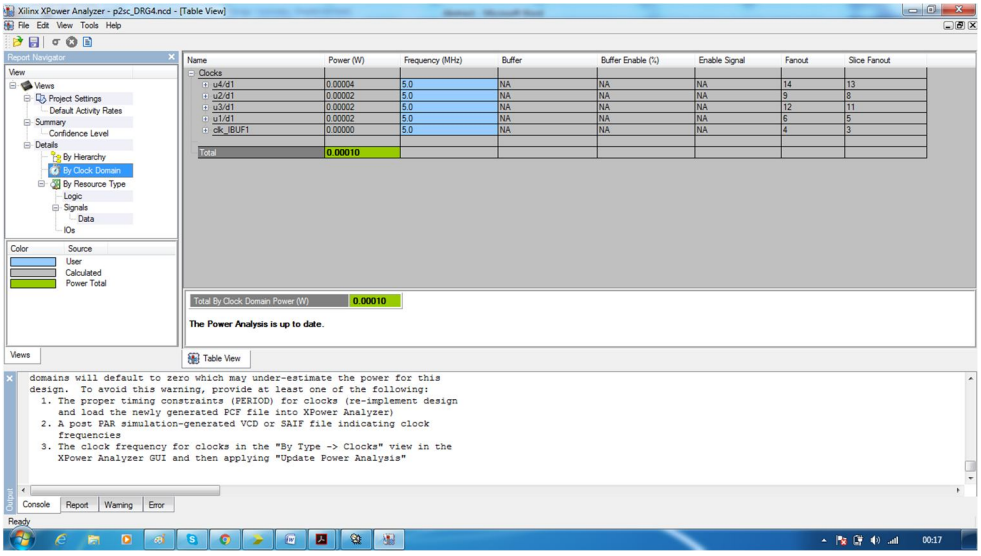


Figure 10: Clock domain Power of Parallel to Serial Converter using DRG4 gate

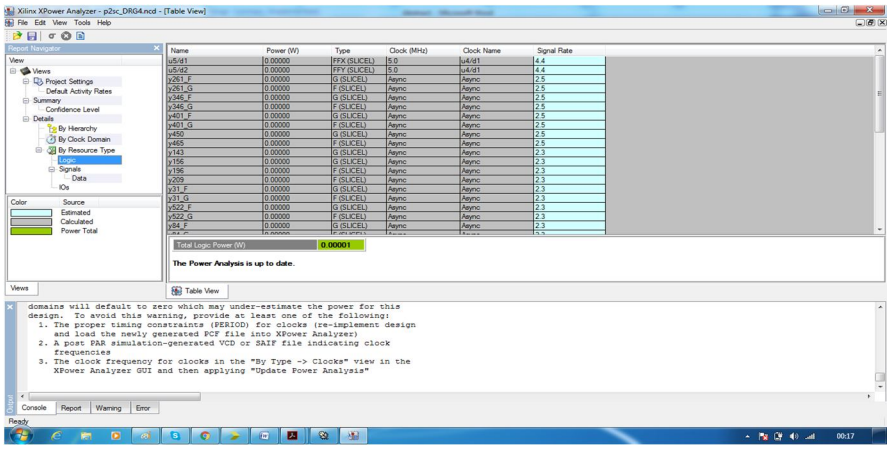


Figure 11: Logic Power of Parallel to Serial Converter using DRG4 gate

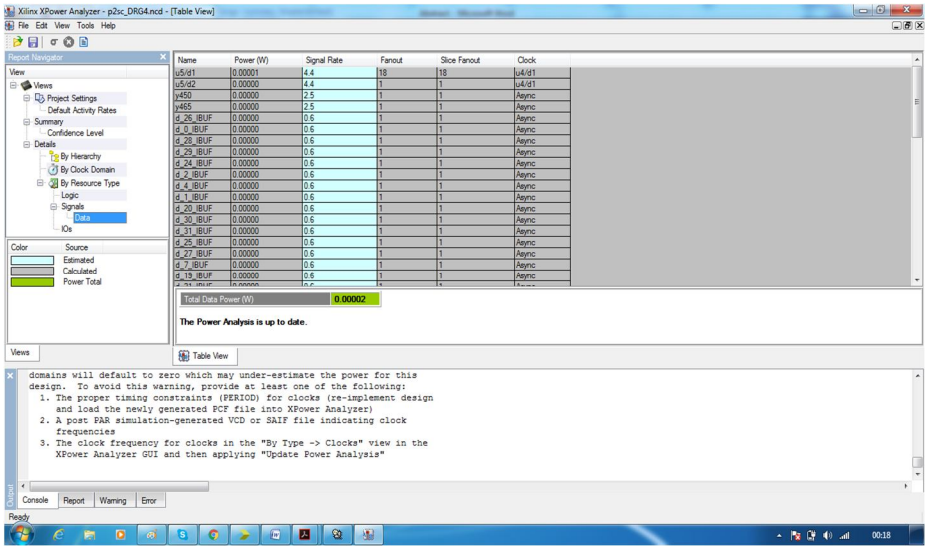


Figure 12: Data Power of Parallel to Serial Converter using DRG4 gate

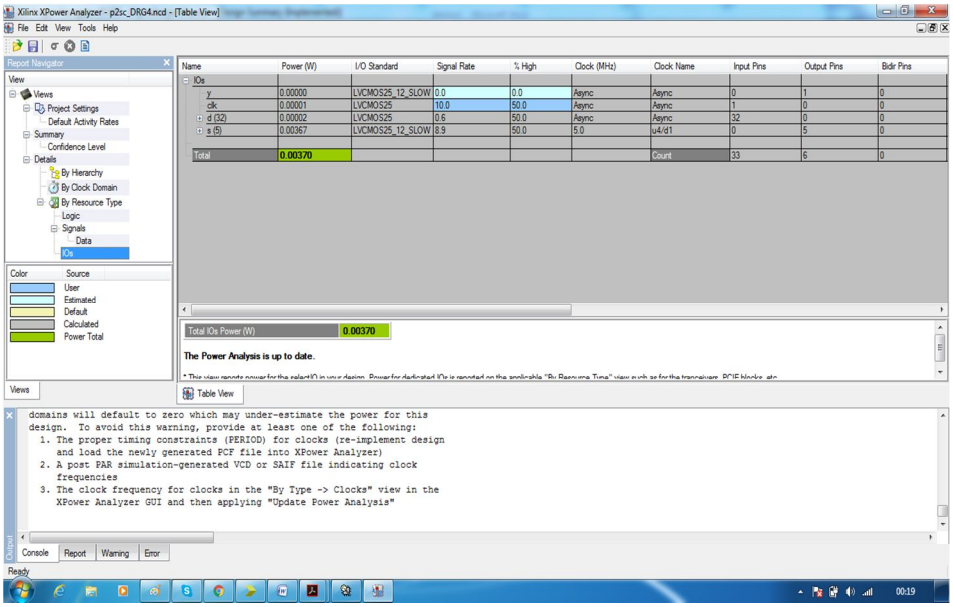


Figure 13: I/Os Power of Parallel to Serial Converter using DRG4 gate

The synthesis results include Design Summary, RTL Schematic, Technology Schematic, FPGA Floor plan and Routing and Power Analysis Report for Parallel to Serial Converter using Fredkin Gate as shown in figures 14 to 22.

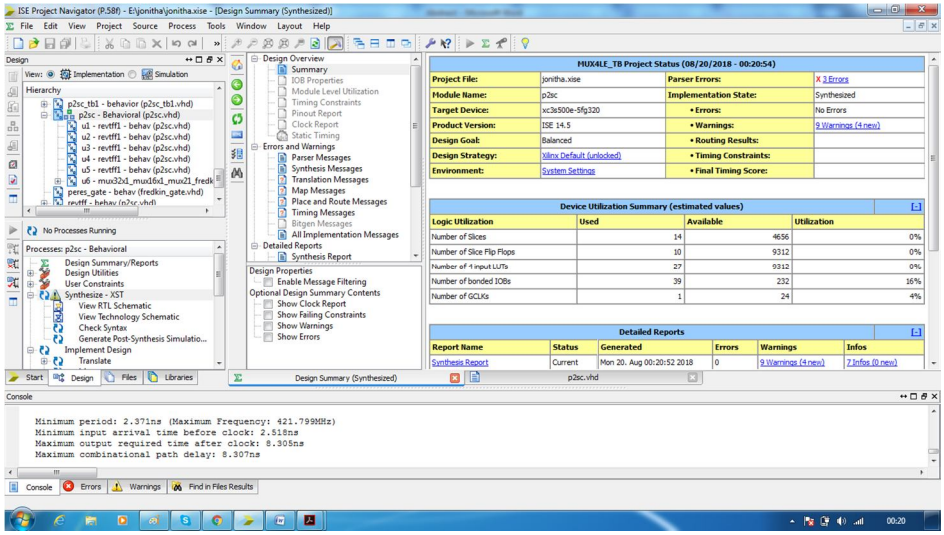


Figure 14: Design Summary of Parallel to Serial Converter using Fredkin Gate

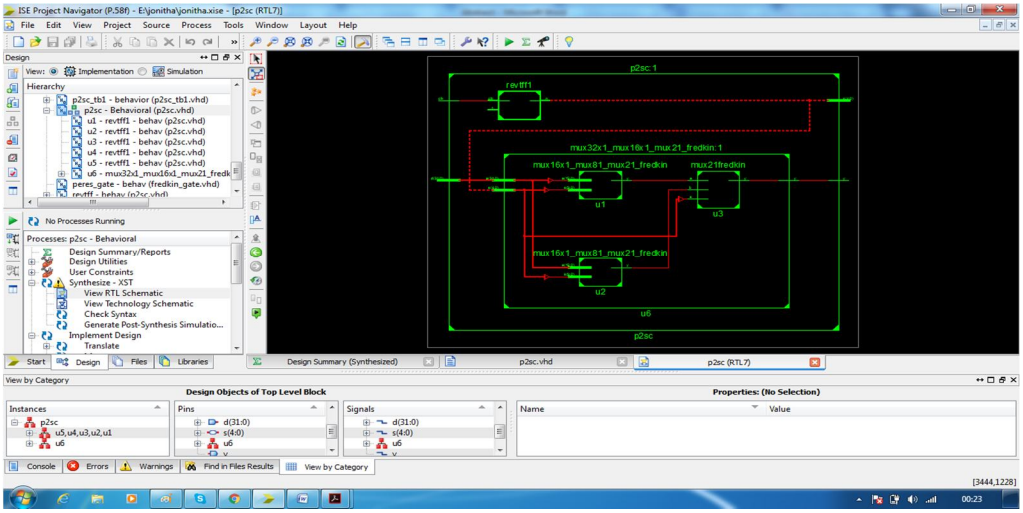


Figure 15: RTL Schematic of Parallel to Serial Converter using Fredkin gate

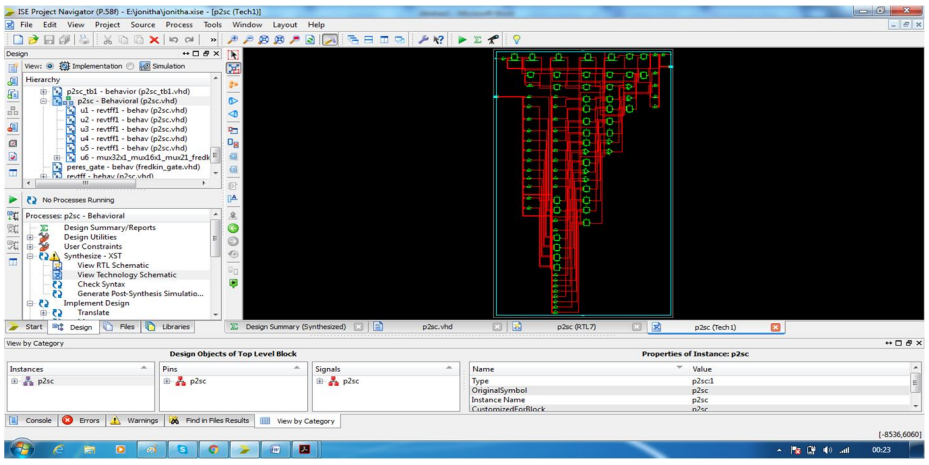


Figure 16: Technology Schematic of Parallel to Serial Converter using Fredkin gate

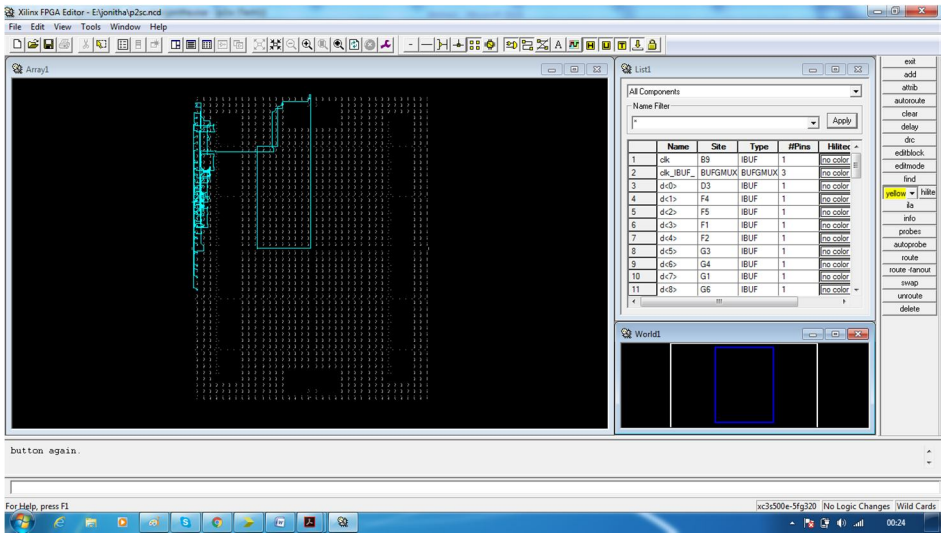


Figure 17: Floor plan and Routed Design of Parallel to Serial Converter using Fredkin Gate

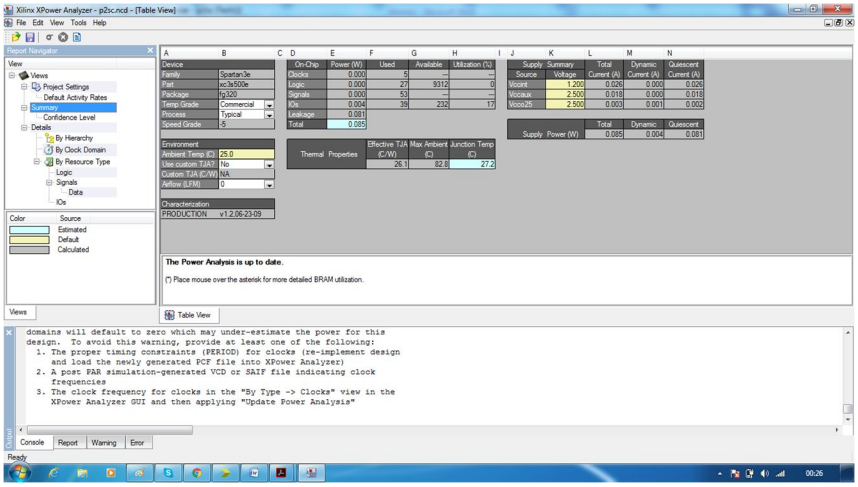


Figure 18: Power Report Summary of Parallel to Serial Converter using Fredkin Gate

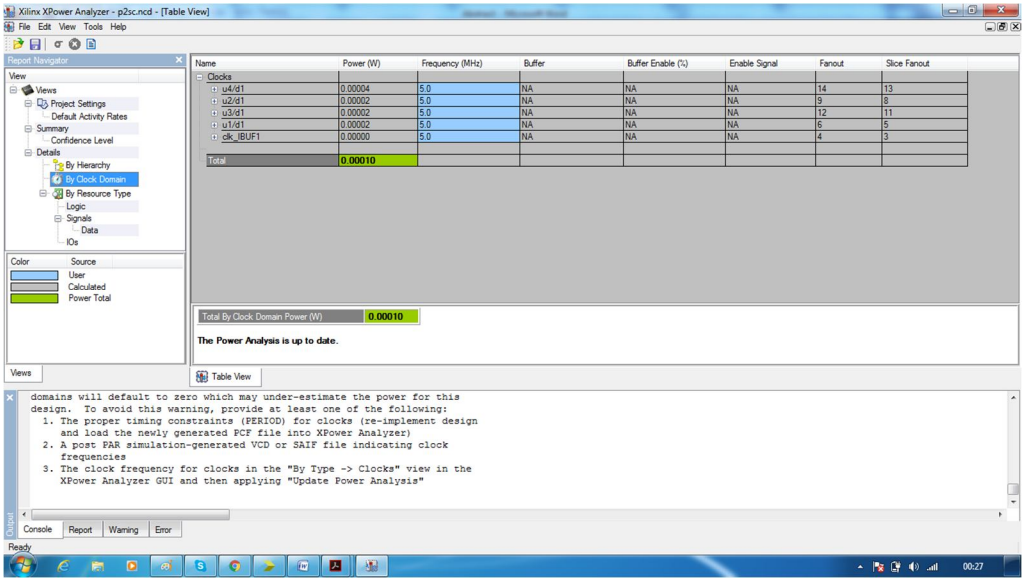


Figure 19: Clock Domain Power of Parallel to Serial Converter using Fredkin Gate

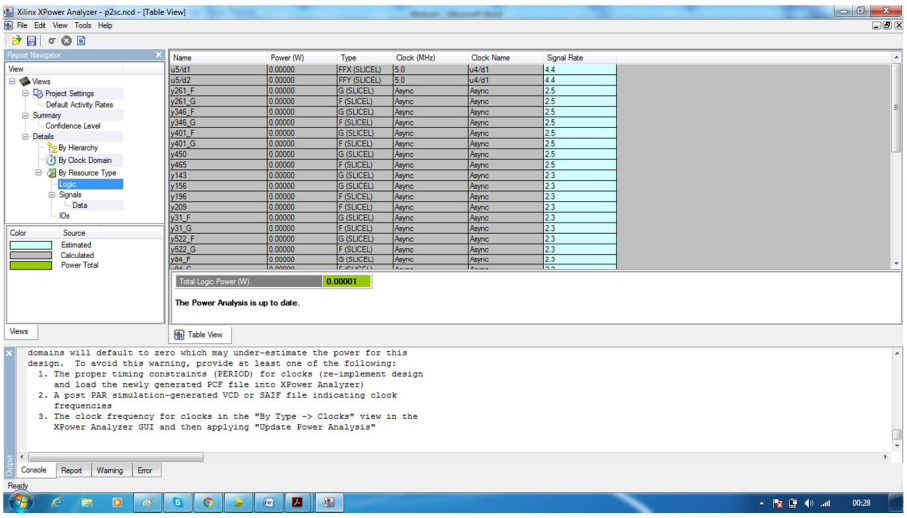


Figure 20: Logic Power of Parallel to Serial Converter using Fredkin Gate

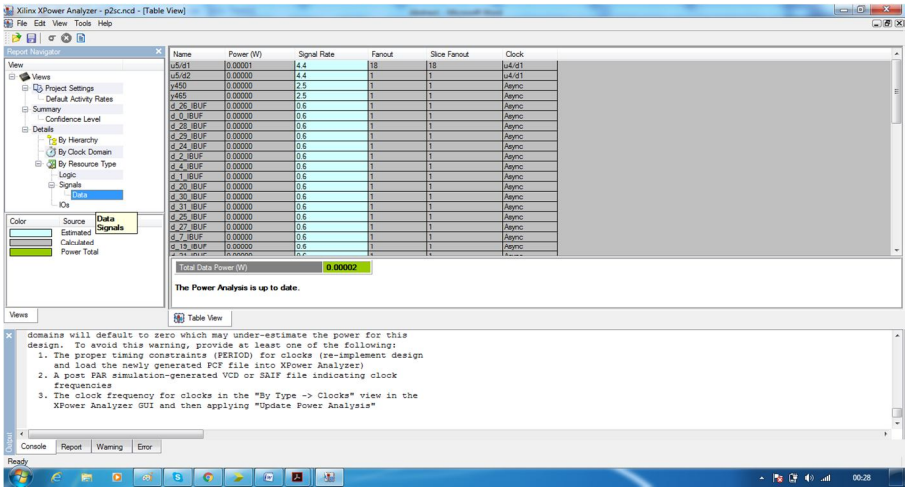


Figure 21 Signal Power of Parallel to Serial Converter using Fredkin Gate

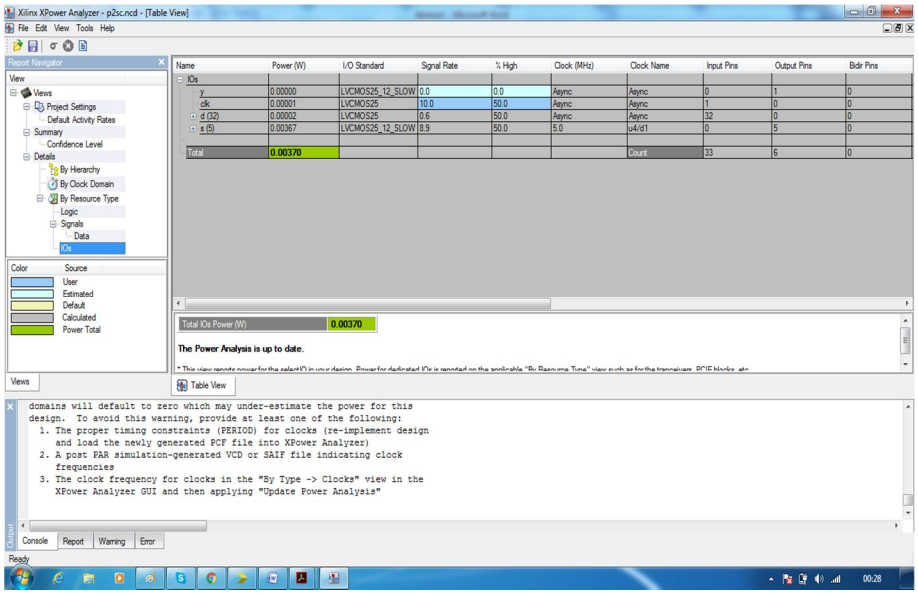


Figure 22: I/Os Power of Parallel to Serial Converter using Fredkin Gate

VI. INTRODUCTION TO ADC

An ADC converts a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal and is chosen to match the bandwidth and required SNR of the signal to be digitized. If an ADC operates at a sampling rate greater than twice the bandwidth of the signal, then per the Nyquist–Shannon sampling theorem, perfect reconstruction is possible. The presence of quantization error limits the SNR of even an ideal ADC. However, if the SNR of the ADC exceeds that of the input signal, its effects may be neglected resulting in an essentially perfect digital representation of the analog input signal.

A. Resolution

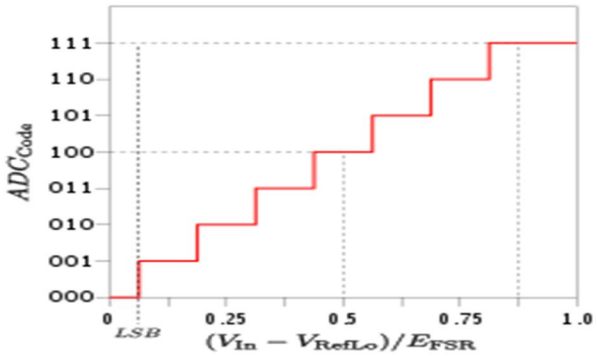


Fig. 23 An 8-level ADC coding scheme

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The resolution determines the magnitude of the quantization error and therefore determines the maximum possible average signal-to-noise ratio for an ideal ADC without the use of oversampling.

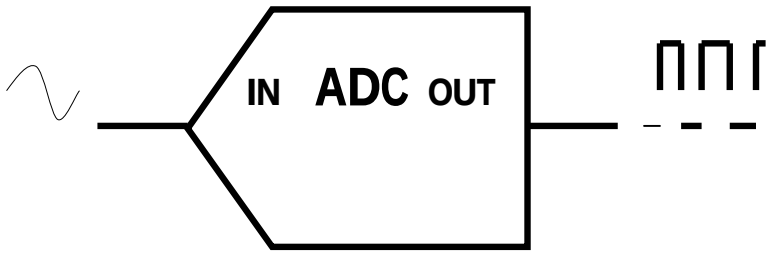
B. Quantization Error

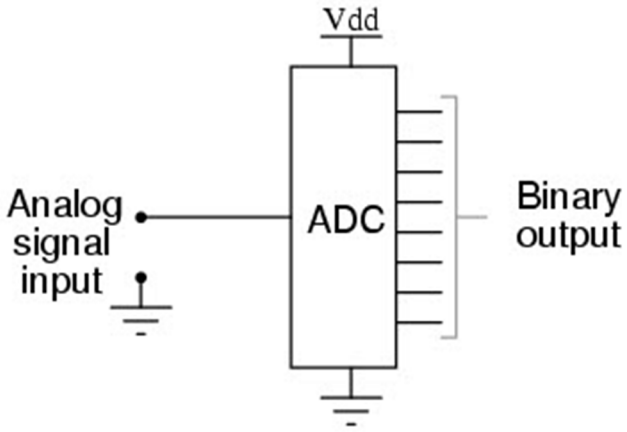
Quantization error is the noise introduced by quantization in an ideal ADC. It is a rounding error between the analog input voltage to the ADC and the output digitized value. The noise is non-linear and signal-dependent. In an ideal analog-to-digital converter, where the quantization error is uniformly distributed between −1/2 LSB and +1/2 LSB, and the signal has a uniform distribution covering all quantization levels, the Signal-to-quantization-noise ratio (SQNR) can be calculated from Where Q is the number of quantization bits.

C. Accuracy

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity are intrinsic to any analog-to-digital conversion. These errors are measured in a unit called the least significant bit (LSB). In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

D. Electronic Symbol





VII. SIMULATION RESULTS OF ADC CONVERTOR

The synthesis results include Design Summary, RTL Schematic, Technology Schematic, FPGA Floorplan and Routing and Power Analysis Report for Parallel to Serial Converter using DRG4 Gate as shown in figures 24 to 31

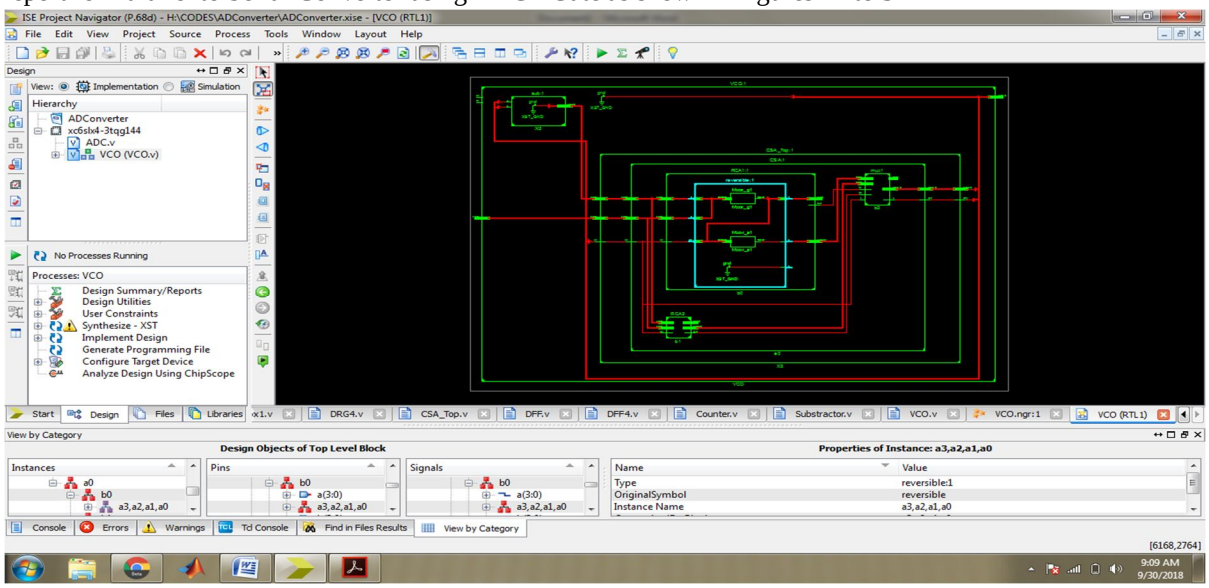


Fig 24: ADC DRG4_Gate Circuit

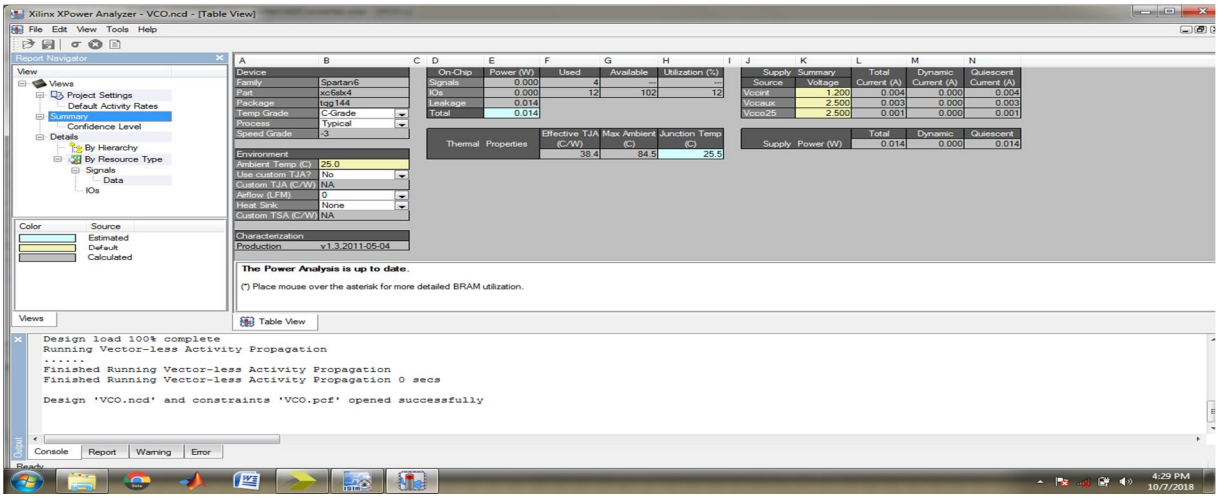


Fig 25 Values of VCO

VCO Project Status (10/07/2018 - 16:29:35)			
Project File:	ADConverter.xise	**Parser Errors:**	No Errors
Module Name:	VCO	**Implementation State:**	Placed and Routed
Target Device:	xc6slx4-3tqg144	**•Errors:**	No Errors
Product Version:	ISE 14.6	**•Warnings:**	25 Warnings (11 new)
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	4,800	0%	
Number of Slice LUTs	0	2,400	0%	
Number of occupied Slices	0	600	0%	
Number of MUXCYs used	0	1,200	0%	
Number of LUT Flip Flop pairs used	0			
Number of bonded IOBs	12	102	11%	
Number of RAMB16BWERs	0	12	0%	
Number of RAMB8BWERs	0	24	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	

Fig 26: Values of ADC convertor

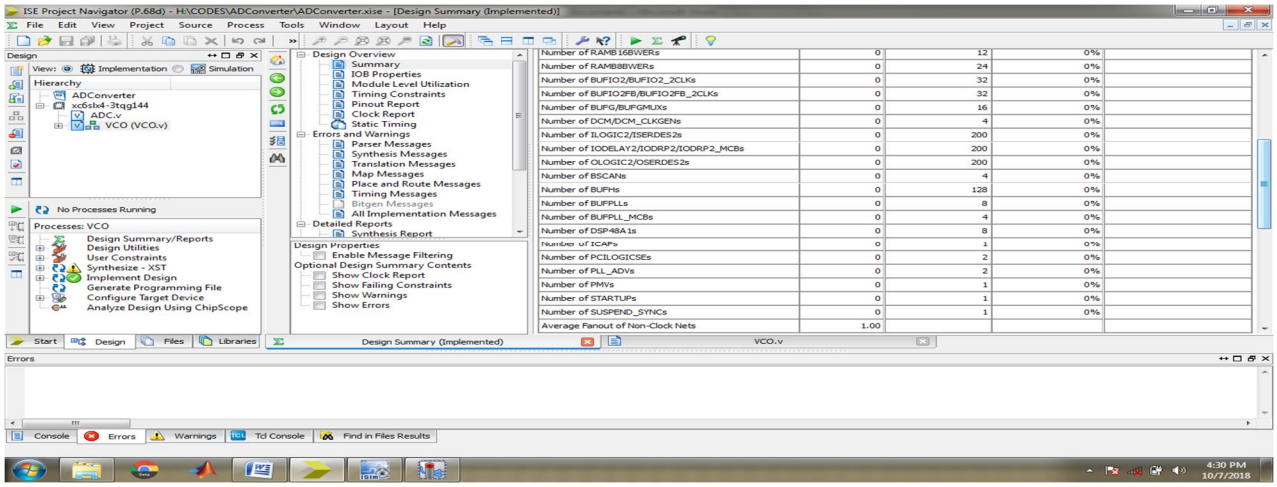


Fig 27: Values of ADC convertor Design Summary Values

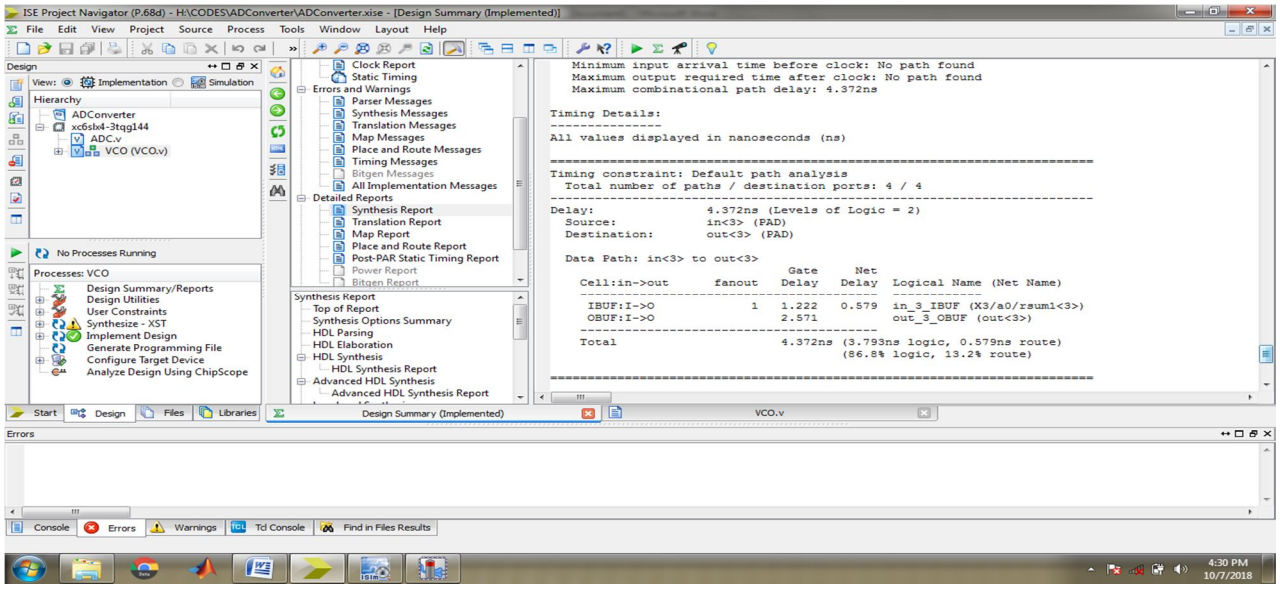


Fig 28 Summary of ADC convertor

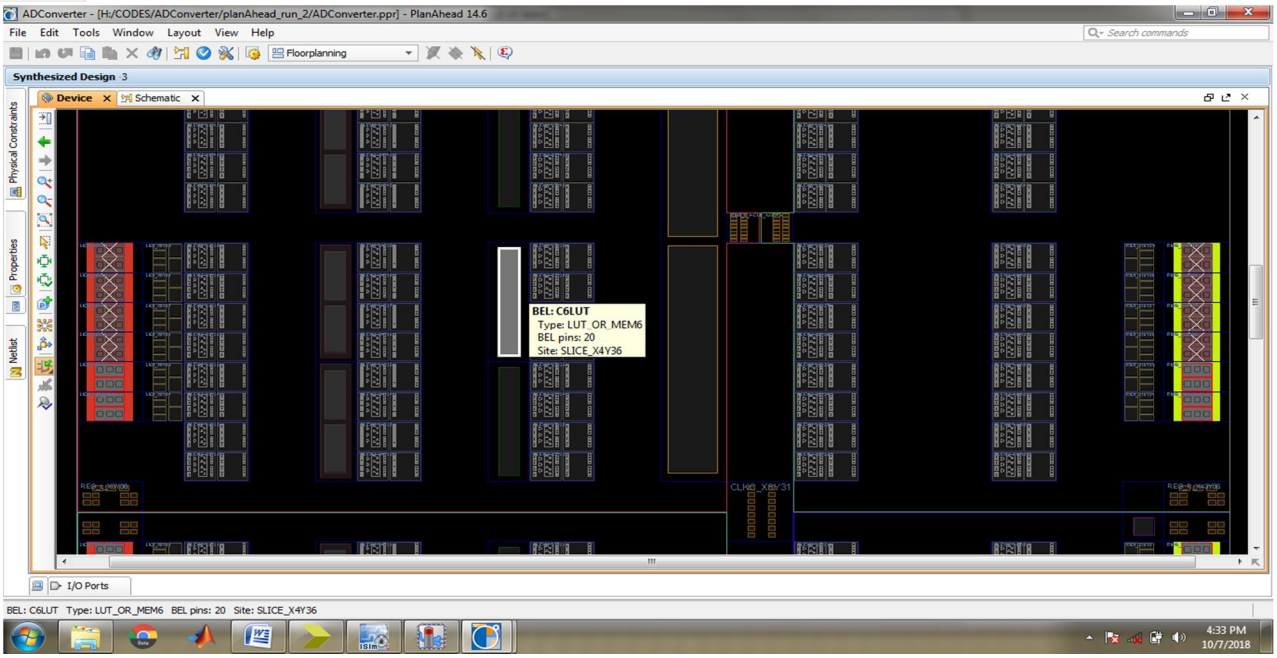


Fig 29 Outputs of ADC convertor

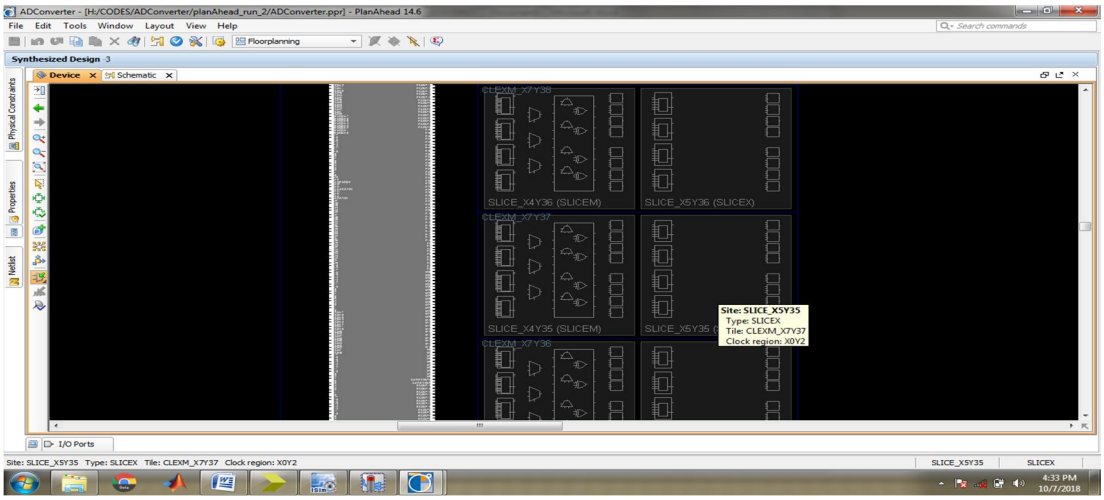


Fig 30 Output of ADC convertor

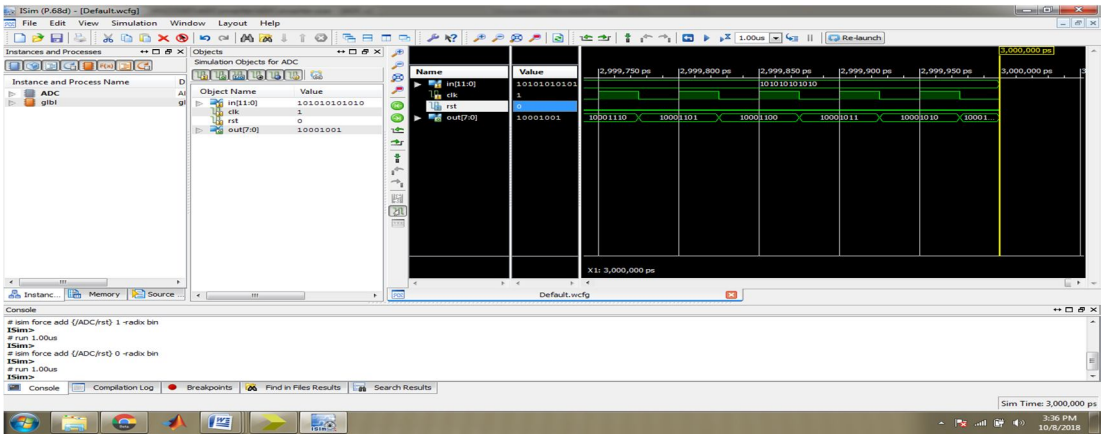


Fig 31 ADC DRG4_gate Circuit simulation results

VIII. CONCLUSIONS

With the advancement of technology, there has been more and more need for the gigabit rate link for storage application, data communication, computer networks and etc. To meet with the high processing multi-gigabit speeds and system performance, it becomes necessary to have prompt and efficient high-speed inter-connects. Traditional parallel link has been used in circuits for a long time, which let the data be sent over multiple channels simultaneously. A Serial Data link is preferred for long distance communication. This work verifies the design of parallel to serial converter using reversible logic gates like Fredkin Gate, Peres Gate, Feynman Gate and DRG4 Gates. The designs are coded in VHDL using structural modelling. These are synthesized and simulated in Xilinx ISE Design Suite 14.5. The results are compared for various parameters and the proposed design i.e., by using DRG4 gate is found to be a better choice of implementing the parallel to serial converter practically due to less quantum cost, area, power dissipation, garbage outputs, etc. As it reduces the quantum cost by 15% and Garbage outputs by 5%. Further as an application, the designs are developed for Flash Analog to Digital Converter for which the proposed design proved to be better choice of implementation using Reversible Logic with an improvement of design in terms of quantum cost and garbage outputs.

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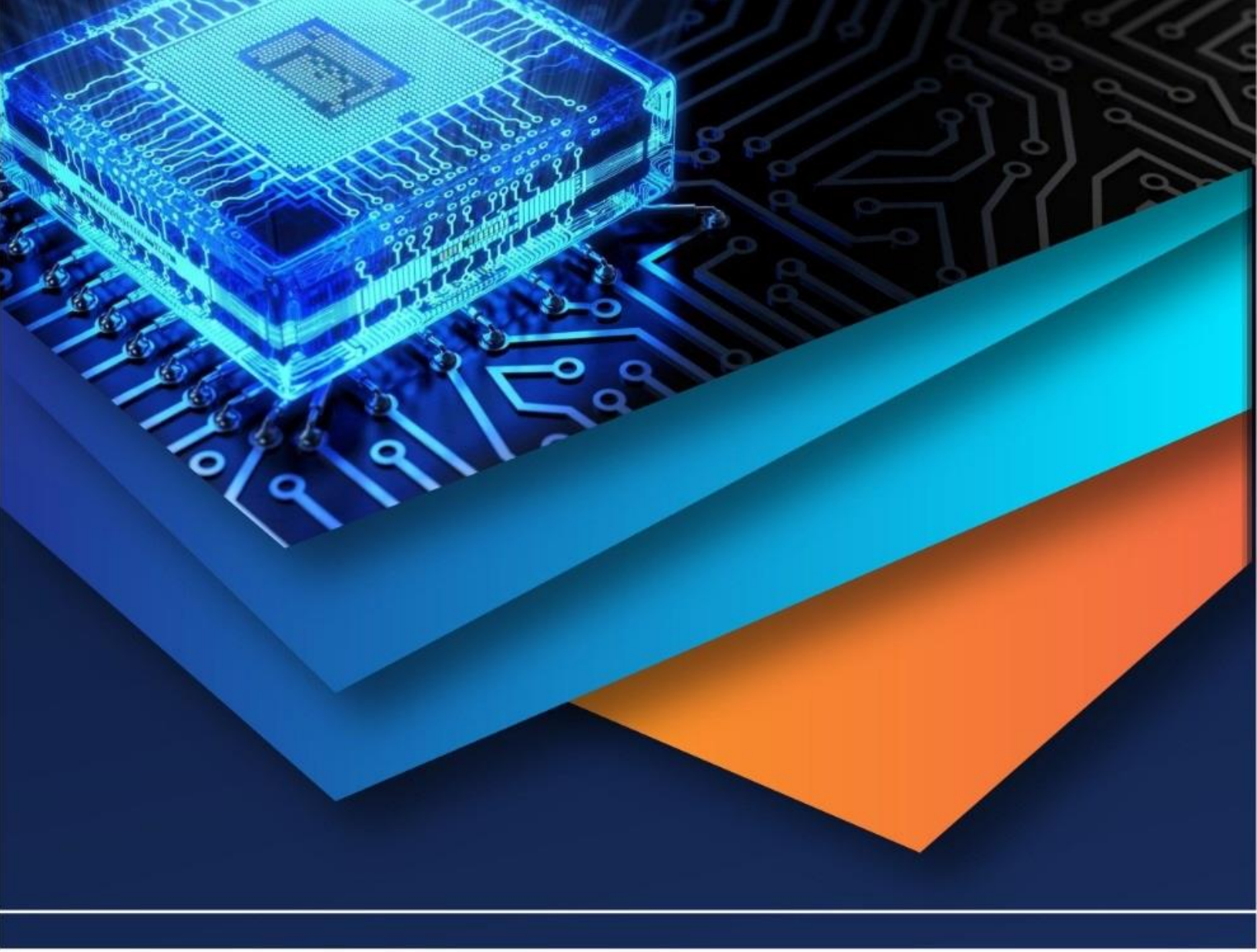

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