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Analysis and Minimization of THD by 7L- Neutral Point Clamped Converter and its Modulation Strategy

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Abstract: ***This thesis aims to extend the knowledge about the performance of multilevel inverter through harmonic analysis. Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses, and stresses in the bearings of a motor. Several multilevel converter topologies have been developed; i) diode clamped, ii) flying capacitors, and cascaded or H-bridge. Referring to the literature reviews, the cascaded multilevel inverter (CMI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility. The H-bridge inverter eliminates the excessively large number of (i) bulky transformers required by conventional multilevel inverters, (ii) clamping diodes required by multilevel diode-clamped inverters, , and (iii) flying capacitors required by multilevel flying-capacitor inverter. As a preliminary study the thesis examined and compared the most common multilevel topologies found in the published literature. Starting from the essential requirements, the different approaches to the construction of multilevel inverter are explained and compared. In particular, aspects of total harmonic distortion (THD) and modulation which are required or desirable for multilevel converters are discussed. Sine-triangle carrier modulation is identified as the most promising technique to pursue for both technical and pedagogical reasons. Since multilevel inverter is considered to be suitable for medium & high power applications, the thesis examined & compared the harmonic analysis of 7-level multilevel inverter through analysis and simulation.***

Keywords: Voltage source, Level changer, Trigger circuit, Bridge circuit

I. INTRODUCTION

Nowadays, there have been major advancements in power electronics. Power electronics have moved along with new developments with such things in control power systems the digital signal processors being used. So basically a new advancement which is given by the power electronic is an inverter. A device that inverts dc power in to ac power at desired output voltage and frequency is called an inverter. Inverter circuit can be very complex so that objective of this paper is to present some of inner working of inverters. Inverter produce an ac output waveform from dc source including applications such as adjustable speed drives, uninterruptible power supply, flexible ac transmission system. Inverter has some typologies which are dividing in two distinct categories. Voltage source inverter and current source inverter.

A. Multilevel Inverter

Multilevel converters are predominantly utilized to composite a desired single- or three-phase voltage wave shape. The desirable multi-staircase end product or output voltage is squeeze out by combining various dc voltage sources. Solar cells, fuel cells, batteries and ultra-capacitors are the most communal non parasitic sources used. One essential application of multilevel converters is concentrated on medium and high-power transmutation. A multilevel inverter is a power electronic device which has potential to generate desired cyclonical voltage amplitude at the output using multiple lower level DC voltages as an input.

1) *Concept of Multilevel Inverter:* First prefer the case of a two-level inverter. A two-level Inverter generates two dissimilar voltages for the load i.e. assume we are implement ***Vdc*** as an input to a two level inverter then it will generate + ***Vdc***/2 and – ***Vdc***/2 on output. In order to frame an AC voltage, these two newly inaugurated voltages are usually altered. For switching essentially PWM is used,. Although this method of initiating AC is adequate but it has few imperfection as it creates harmonic misrepresentation in the output voltage along with a high dv/dt as correlated to that of a multilevel inverter. Useuly this

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arrangement works still in minor operation it generate complication particularly those where low misrepresentation in the output voltage is recommended.

B. *Multilevel Inverter Topology*

There are few properties of multilevel inverters available. The inequality present in the structure of switching and the source of incoming voltage to the multilevel inverters. The most commonly used multilevel inverter topologies are:

1) Cascaded H-bridge multilevel inverters
2) Diode Clamped multilevel inverters
3) Flying Capacitor multilevel inverter

C. *Advantages of Flying Capacitor Multilevel Inverters*

Static var generation is the best application of Capacitor Clamped Multilevel inverter

1) For balancing capacitors' voltage levels, phase redundancies are available.
2) We can control reactive and real power flow.

D. *Disadvantages of Flying Capacitor Multilevel Inverters*

1) Voltage control is complex for all the capacitors
2) Complex startup
3) Switching adequacy is poor
4) Capacitors are costly than diode.

II. EXPERIMENTAL WORK

Block Diagram

The developed system performs in the basis of the blocks as shown in fig 1.

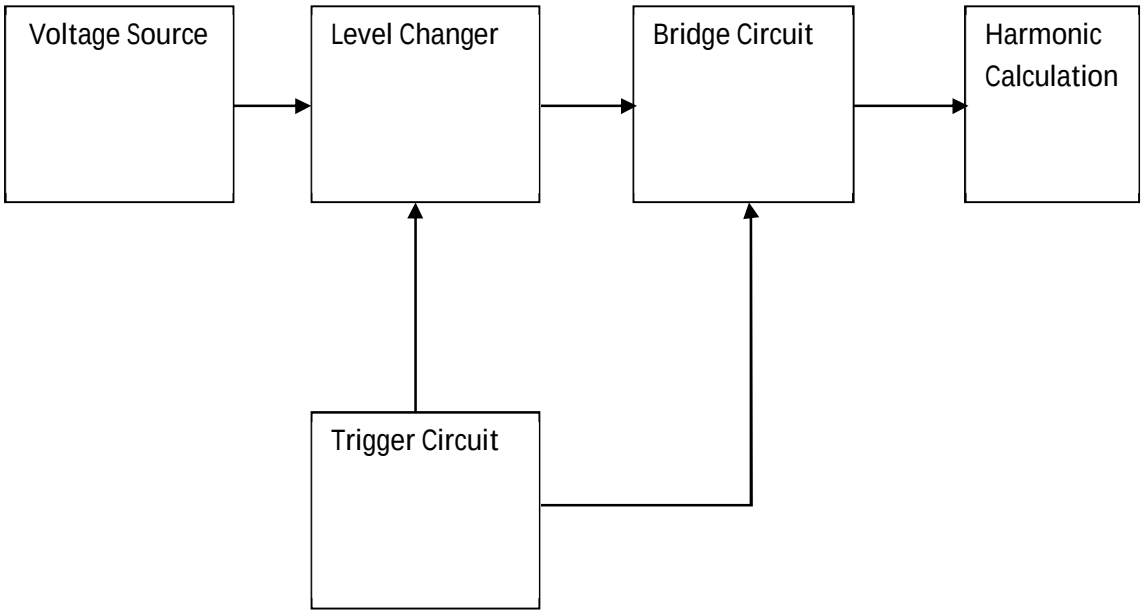

Fig.1: Block Diagram of Proposed Methodology of Cascaded inverter

A. *Derivation Of The Proposed 7l-Npc Inverter*

First, the input DC voltage is described as VDC. The DC-link exists of two series-fetched capacitors (C1, C2) in NPC inverter whose voltages are graded at half of DC voltage (VDC/2). . In case of 3-stage NPC inverter, clamping diode, D1 and D4 clamped the DC bus voltage into three voltage level, $+V_{dc}/2$, 0 and Diode, D4 equality out the voltage equally distributed between S_{4in} and S_{4out}, with S_{4in} blocking the voltage across C_1 and S_{4out} blocking the voltage across C_2.The 7-level NPC multilevel inverter consists of 1 source 6 subsystem models and switch system as illustrated in Figure 2.

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B. Source Subsystem

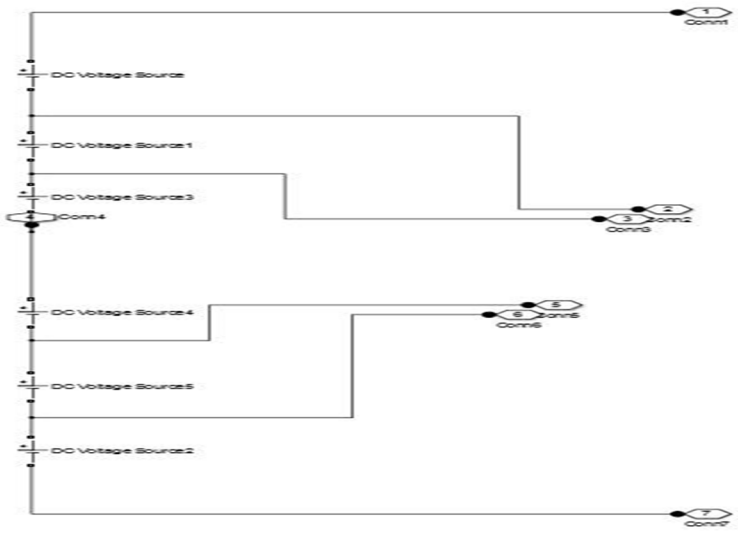

Fig. 2: Subsystem of Source

The clamping diodes are connected in such a way that it blocks the reverse voltage of the capacitor as shown in fig 4.13. Two capacitors have been used to divide the DC link voltage into three voltage level i.e. +Vdc, 0V and –Vdc, thus the name of 3-level. Same as in 7-level it reverse the 7 voltage level.Here one point is common point and the 6 DC voltage sources are equally distributed both side of neutral point. In this work, twelve triggering signals are needed for the 7-level NPC inverter. These signals should be synchronized with the AC supply voltage. Since the Matlab/Simulink does not have such triggering block set, a new triggering block has been designed and developed using the blockset obtained from Simulink Toolbox. Also, the gate signals sequence and duration of conduction angle of the IGBTs have been determined.

C. Pulse Generation Subsystem

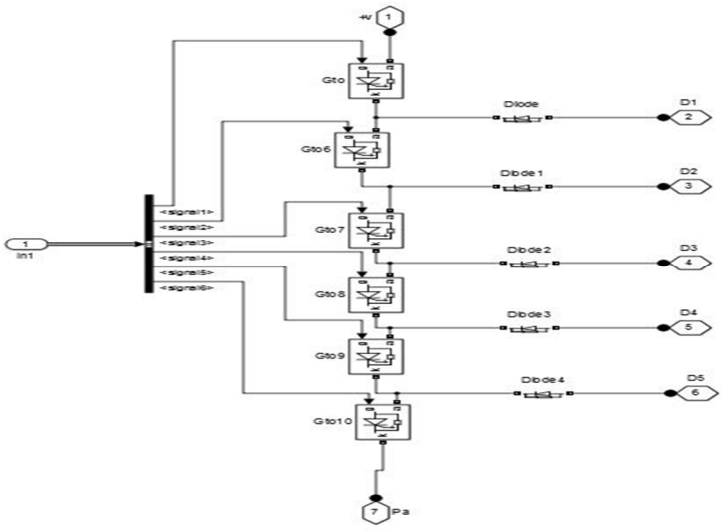

Fig. 3: Subsystem of Pulse Generation

Here Pulse generator is given the value with phase shift so as to control the neutral clamped inverter to produced desired output level of voltage at the output. The pulse generator block generates square wave pulse at un-varying intervals. The block wave shape parameter amplitude, pulse width, period and phase delay conclude the shape of the output wave shape. If a level changer block is in a resettable subsystem that hits a reset trigger. The block output resets to its initial condition. In our subsystem we are using 6 pulse generators as shown in figure 3.

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D. Switch Subsystem

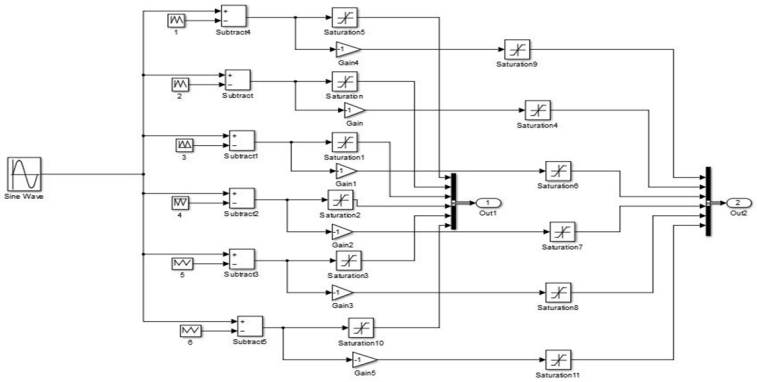

Fig. 4: Subsystem of Switch

If action subsystem block is a subsystem block preconfigured as a starting point for creating a subsystem whose execution is enabled by an external block than it evaluates a logical expression and depending on its result of evaluation.Here the subsystem of switch is given in figure 4.

E. Operating Principles Of 7l-Npc Inverter

Working is based on convention neutral point clamped converter. NPC inverter has 36 switching states to produce 7 output level +3,+2,+1,0,-1,-2 and -3. When switches (T1, T2) or (T3, T4) are switched on, the inverter is producing +2 or - 2 output stages. Similarly, for the switching states which produce +1 or -1 levels, (T1, T3) or (T2, T4) are turned on. In this way +3 and -3 level is also generate. Here input voltage is 100V and the phase voltage is 200V. By the simulink model after burn the program in MATLAB following result is produced.

III. SIMULATION RESULTS

A low harmonics content of a proposed 7-level NPC inverter simulation model has been successfully designed and developed. Previously a low harmonic content of a proposed 3level, 5 level and seven level cascaded multilevel inverter model is also designed and a mitigated 5 level cascaded multilevel model is designed and correlate with the 5 level cascaded model in our methodology. The entire model has been constructed in MATLAB to obtained results from the simulation. The voltage THD values of the proposed inverter are lower than that of the same inverter using different modulation techniques. The models show that the results obtained corresponded to each others. The waveforms have the same shapes and values. The analyses have been conducted only for the 7-level NPC inverter. Here the fundamental voltage is more. No need to use to more filter it automatically reduces the harmonics.

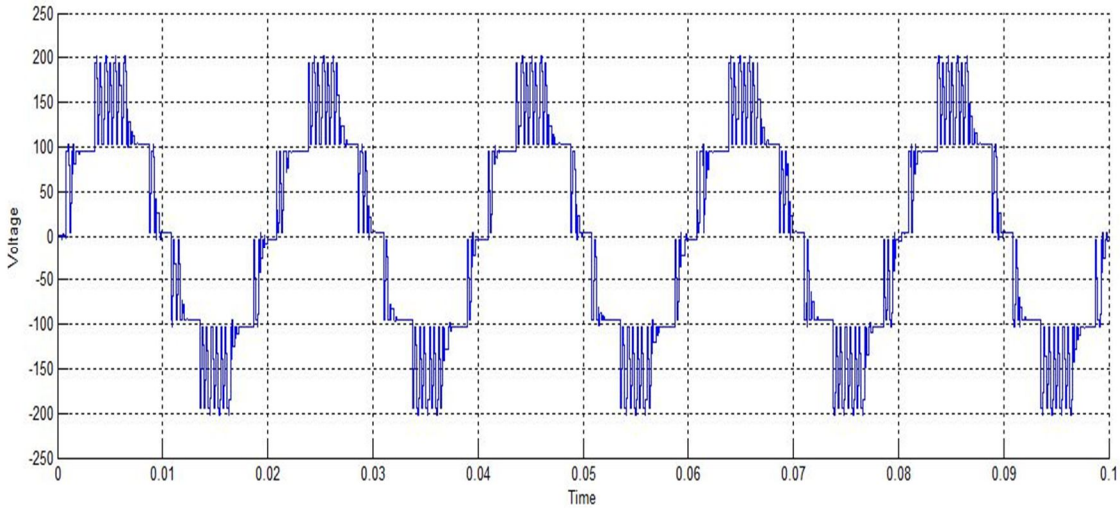

Fig.5: Output of 7 Level NPC Multilevel Inverter

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In fig 5 output waveform of 7NPC multilevel inverter is shown. Here voltage is vary with respect to time and generate 7 level.

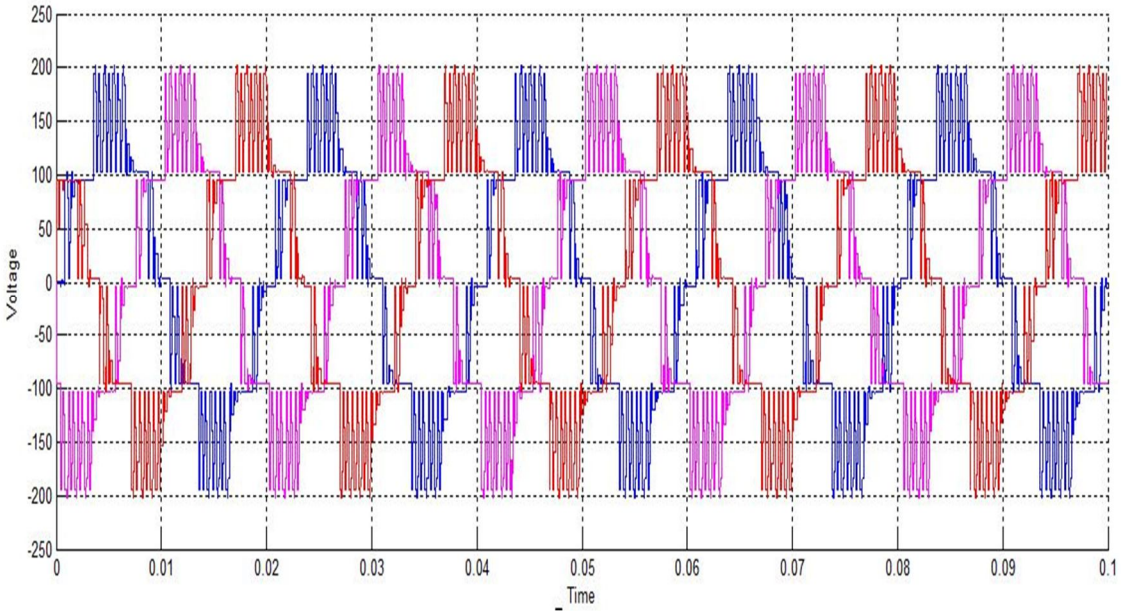

Fig. 6: Simulation signal Analysis of 7 Level NPC Inverter

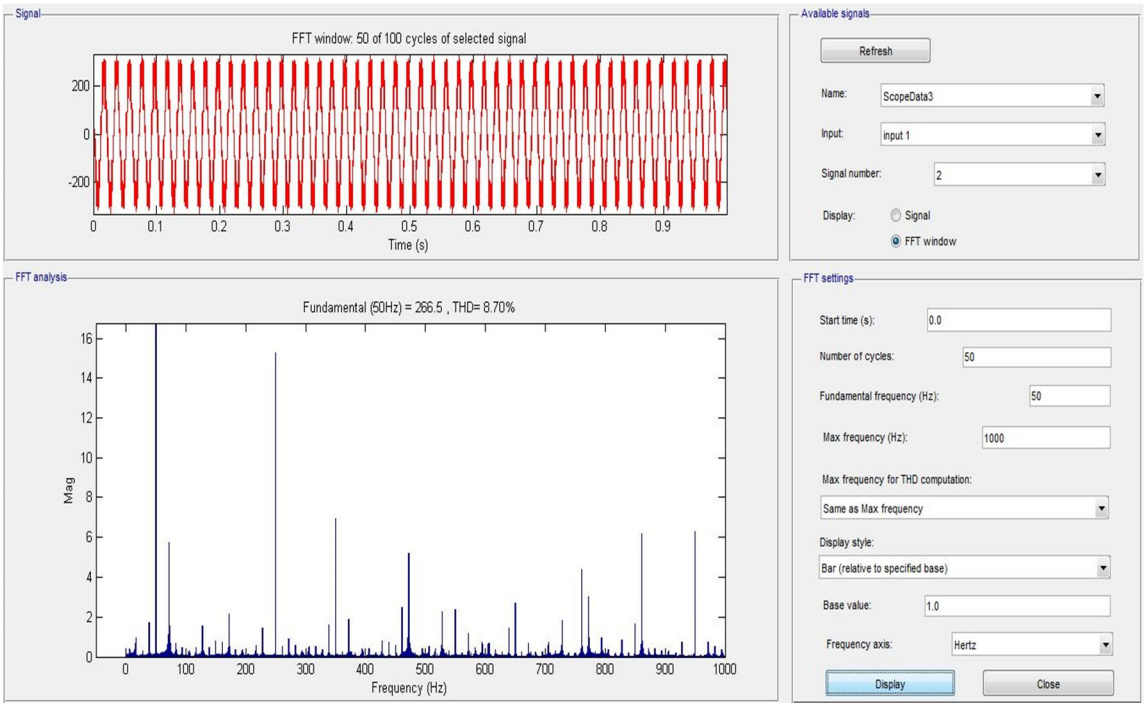

Fig. 7: FFT Analysis of Phase Voltage 7 Level NPC Inverter

TABLE 1: THD % of 7 levels NPC Multilevel Inverter

Simulation of 7-Level NPC Inverter			
THD (%)	Line Voltage	Phase voltage	Line Current
	12.20	8.70	6.15

He the fundamental frequency are 154.1 Hz and THD% is 12.20% for line voltage, 266.5 Hz for phase voltage and THD% is 8.70%, 264.1 Hz for line current and THD% is 6.15%. This result is already shown in figure 5, figure 6 and figure 7.

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IV. CONCLUSION

This thesis presents a brief summary of multilevel inverter circuit topologies (3- level, 5-level and 7-level) and their analysis. Each MLI has its own benefits and limitations and for any one particular application, one topology will be more appropriate than the others. Often, topologies are selection placed on what has gone previous, even if that topology may not be the best choice for the application. The advantages of the body of research and familiarity within the engineering community may outweigh other technical disadvantages. Multilevel converters can achieve a productive increase in complete switch frequency through the erasure of the shortest order switch frequency concepts. As discussed in introduction, in the middle of the multilevel converter topologies, the Cascaded Multilevel Converter is the most promising alternative for industry utilization. There are various modulation methods for multi level inverters. But carrier based modulation method is simple and effective. The PWM output spectra were calculated from basic operation simulated using MATLAB. The simulation results for three-level, five-level and seven-level cascaded inverters are presented in chapter-4. Their harmonic analysis is also discussed. THD of the three cascaded multi-level inverters have been calculated at different modulation index. Their speed and torque are compared. We have observed that the performance of the induction motor drive improves with increase in voltage level of the inverter. The simulation results show that the Cascaded Multilevel Converter in different level has a satisfactory execution. To verify the simulation conclusion, a Cascaded Multilevel Converter, using separated DC point of supply is used. Both simulation and exploratory results are in nearby agreement. Correlated to typical PWM switching schemes, multilevel topology of switching will lead to lower switching losses. As a result, using fundamental frequency switching course of action will move towards to increased efficiency. This paper discuss about performance characteristics of various multilevel technique.Comparison of THD level component is also tabulated which shows by increasing no of level THD reduced to a great extent and it also show that it is minimum for 7 level using PWM scheme.

REFERENCES

[1] Ayoub Kavousi, Behrooz Vahidi, Reza Salehi, Mohammad azem Bakhshizadeh, Naeem Farokhnia and S.Hamid Fathi,(april 2012) “Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters”, IEEE Transactions on power electronics, vol. 27, no. 4, pp1689-1696.
[2] Damoun Ahmadi, KeZou, Cong Li, Yi Huang and Jin Wang,(october 2011) “A Universal Selective Harmonic Elimination Method for High-Power Inverters”, IEEE Transactions on power electronics, vol. 26, no. 10,pp2743-2752,.
[3] FaeteFilho, Leon M. Tolbert, Yue Cao and BurakOzpineci,(september/October 2011) “Real-Time Selective Harmonic Minimization for Multilevel Inverters Connected to Solar Panels Using Artificial Neural Network Angle Generation”,IEEE Transactions on industry applications, vol. 47, no. 5, pp2117-2124.
[4] Hossein Sepahvand, Jingsheng Liao and Mehdi Ferdowsi,(november 2011) “Investigation on Capacitor Voltage Regulation in Cascaded H-Bridge Multilevel Converters With Fundamental Frequency Switching”, IEEE Transactions on industrial electronics, vol. 58, no. 11,pp5102-5111.
[5] Jason R. Wells, XinGengPatrick L. Chapman Philip T. Kreinand Brett M. Nee,(january 2007) “Modulation-Based Harmonic Elimination”, IEEE Transactions on power electronics, vol. 22, no. 1,pp336-340.
[6] J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L. G. Franquelo, P. W. Wheeler and M. A. Aguirre,(june 2012)”Selective Harmonic Mitigation Technique for Cascaded H-Bridge Converters with Non-Equal DC Link Voltages”, IEEE Transactions on power electronics,pp1-9.
[7] John N. Chiasson, Leon M. Tolbert, Keith J. McKenzieand Zhong Du,(march 2004) “A Unified Approach to Solving the Harmonic Elimination Equations in Multilevel Converters”,IEEE Transactions on power electronics, vol. 19, no. 2, pp478-500.
[8] A. Maheswari, S. Mahendran, Dr. I. Gnanambal (August 2012), “Implementation of Fundamental Frequency Switching Scheme on Multi –Level Cascaded H-Bridge Inverter Fed Three Phase Induction Motor Drive” Wulfenia journal,Klangfurt, Austria, Vol 19, No. 8, pp10-24.
[9] L. M. Tolbert, “A Multilevel Modular Capacitor Clamped DC-DC Converter,” in Proc. 41st IAS, 2006, pp. 966–973.K.
[10] Mouton, H.T.,2002“Natural Balancing of Three-Level Neutral-Point-Clamped PWM Inverters IEEE Transaction on Industrial Electronics, Volume 49, Issue 5, October
[11] [10] Nguyen, T.H., P.K.W. Chan, Y. Shrivastava and S.Y.R. Hui, 2005. “A Three-Dimensional Space Vector Modulation Scheme for Three-Level Three-Wired Neutral Point Clamped Converters”, IEEE 36th Power Electronics Specialists Conference 2005. pp. 2307-2314.
[12] Panagis, P., F. Stergiopoulos, P. Marabes, and S. Manias, 2008. “Comparison of State of theArt Multilevel Inverters”, IEEE Power Electronics Specialists Conference 2008, 15-19 June2008, pp. 4296-4301.
[13] Peng, F.Z., 2000. “A Generalized Multilevel Inverter Topology with Self Voltage Balancing”,IEEE Industry Applications Conference 2000, Rome, Italy, Volume 3, 8-12 October 2000, pp.2024-2031.
[14] Rashid, M.H., 2001. Power Electronics: Circuits, Devices and Applications. New Jersey: Prentice Hall, 2001.

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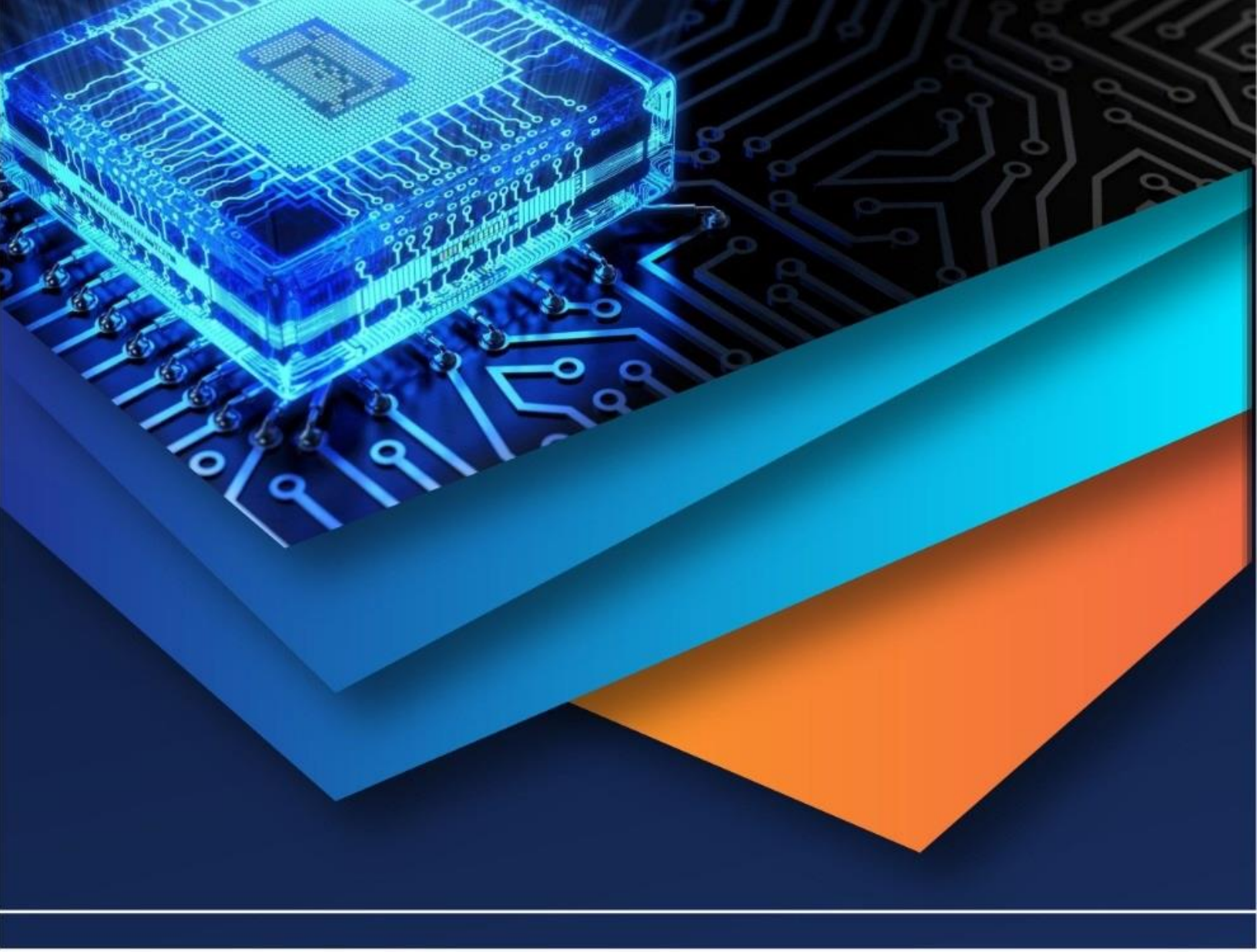

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