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Technology (IJRASET) Analysis of Self Checking Additional Adder Circuit in Combinational Circuits

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Abstract— Digital computers perform variety of information tasks; among the functions encountered are the various arithmetic operations. The most basic arithmetic operation is the addition and subtraction of two or more binary digits. In processors adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar operations. The basic building block of many complex computational systems is the full adder. VLSI integrates a large system into a single chip. Self checking scheme is becoming an important design technique to full fill the requirements of modern computer systems with full reliability. The main aim of this paper is to provide the output of ripple carry adder without any error even when any one of the full adder is fault. The proposed system is built using VHDL, simulated using Xilinx ISE 12.1 and implemented using Spartan-3E FPGA and ALTERA Universal kit. This will fit the specified functional requirements and finds a solution to overcome the problem of fault in any one full adder.

Keywords—Full adder, self-checking, modified adder, modified subtractor, combinational circuit, multiplexer.

I. INTRODUCTION

For any large combinational circuit there are generally two approaches to design. Taking simpler circuits and replicates them or designs the complex circuit as a complex device. Both the circuits allow spending less time to design and more time for signals to propagate through the transistors. So attempt to replace portions of the circuit that are too slow and faulty. It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that Cin = 0).

The layout of a ripple-carry adder is simple, which allows for fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic. In a 32-bit ripple-carry adder, there are 32 full adders, so the critical path (worst case) delay is 2 (from input to carry in first adder) + 31 * 3 (for carry propagation in later adders) = 95 gatedelays. The general equation for the worst-case delay for an n-bit carry-ripple adder is

$$T_{CRA}(n) = T_{HA} + (n-1).T_C + T_S$$

= $T_{FA} + (n-1).T_C$

$$= 6D + (n-1)Tc = (n+2).2D$$
 --(1)

The delay from bit position 0 to the carry-out is a little different:

$$T_{CRA[0:C_{out}]} = T_{HA} + n.T_{C} = 3D + n.2D - (2)$$

The carry-in must travel through n carry-generator blocks to have an effect on the carry-out

$$T_{CRA[C_0:C_{out}]}(n) = n..T_C = n.2D - (3)$$

A design with alternating carry polarities and optimized AND-OR-Invert gates can be about twice as fast. To reduce the computation time, engineers devised faster ways to add two binary numbers by using carry-look ahead adders. They work by creating two signals (P and G) for each bit position, based on whether a carry is propagated through from a less significant bit position (at least one input is a '1'), generated in that bit position (both inputs are '1'), or killed in that bit position (both inputs are '0'). In most cases, P is simply the sum output of a half adder and G is the carry output of the same adder. After P and G are generated the carries for every bit position are created. Some advanced carry-look ahead architectures are the Manchester carry chain, Brent–Kung adder, and the Kogge–Stone adder. For all the adder circuit the combination of half adder and full adder has been used.

Some other multi-bit adder architectures break the adder into blocks. It is possible to vary the length of these blocks based on the propagation delay of the circuits to optimize computation time. These block based adders include the carry-skip (or carry-

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bypass) adder which will determine P and G values for each block rather than each bit, and the carry select adder which pregenerates the sum and carry values for either possible carry input (0 or 1) to the block, using multiplexers to select the appropriate result when the carry bit is known.

Other adder designs include the carry-select adder, conditional sum adder, carry-skip adder, and carry-complete adder.

II. EXISTING SYSTEM

A. One Bit Full Adder

A one-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs a, b and cin and two outputs S and Cout [3] as illustrated in Fig. 1.Expressions for S and Cout are given in (1) and (2)



Fig1.A full adder block

 $S = a \oplus b \oplus cin-(1)$ Cout=a.b+b.cin+cin .a-- (2)

B. Full Subtractor

A one-bit full subtractor is a combinational circuit that performs subtraction of three bits. It has three inputs are X, Y and Z and the two outputs are D (difference) and B (borrow) as illustrated in Fig.2. Expressions for D and B are given in (1) and (2)

X		D
Y 7	Full subtractor	В

Fig 2.A full subtractor block

$$D = X \oplus Y \oplus Z$$
$$B = \overline{X} \cdot (Y \oplus Z) + Y \cdot Z$$

C. Multiplexer

A multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has *n* select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector.



Fig3.A One Bit Multiplexer

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D. Four Bit Ripple Carry Adder

A simple ripple carry adder (RCA) is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain. Fig. 2 shows the interconnection of four full adder (FA) circuits to provide a four bit ripple carry adder.



Fig4. A Four bit ripple carry adder

Notice from Fig. 2 that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits a0 and b0 in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits S0 - S3. The main problem with this type of adder is the delays needed to produce the carry out signal and the most significant bit. These delays increase with the increase in the number of bits to be added.

E. Four Bit Ripple Borrow Subtractor

A ripple-borrow subtract or can be composed of a cascade of full subtractor. Two binary numbers A and B are subtracted from right to left, creating a difference and a borrow at the outputs of each full subtract or for each bit position. Fig. 5 shows the interconnection of four full subtractor (FS) circuits to provide a four bit ripple borrow subtractor.



Fig5.A Four bit ripple borrow subtractor

III. PROPOSED SYSTEM

The proposed system provides the modified structure of the four bit ripple carry adder, four bit borrow subtractor and four bit 2's complement borrow subtractor. The working principle and operation of the proposed system is similar as it before expect the number of adder and multiplexer increases in both the adder and subtractor. These is because the fault any full adder/subtractor is replaced with another adder /subtractor circuit. With this we can able to rectify the fault easily



Fig6.A Modified Four bit ripple carry adder

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Fig 7.A Modified Four bit ripple borrow subtractor



Fig 8.A Modified Four bit ripple borrow subtractor (2's complement)

IV. SIMULATION RESULTS AND PERFORMANCE COMPARISON

Even though the number of adder and mux in the modified binary adder and Subtractor architecture increases, any fault in one of the full adder can be replaced with another adder circuit. With this modified structure, we can able to rectify the fault easily. Fig shows the simulation result for 4-bit ripple carry adder done with the help of Xilinx12.1 and implemented in Spartan 3E FPGA board.



Fig 9.simulation of 4-bit ripple carry adder

Fig shows the timing details for 4 bit ripple carry adder done with the help of Xilinx12.1.

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elay:	8.959ns	(Levels o	f Logic	: = 6)
Source:	b<0> (PAI	D)		
Destination:	cout (PAI	D)		
Data Path: b<0> t	o cout			
		Gate	Net	
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)
IBUF: I->0	2	1.106	0.532	b 0 IBUF (b 0 IBUF)
LUT3:10->0	2	0.612	0.449	a1/cout1 (c<0>)
LUT3: I1->0	2	0.612	0.449	a2/cout1 (c<1>)
LUT3: I1->0	2	0.612	0.449	a3/cout1 (c<2>)
LUT3: 11->0	1	0.612	0.357	a4/cout1 (cout OBUF)
OPHE.T NO		2 1 6 0		CONT OPUE (CONT)

Fig 10.Timing details of 4-bit ripple carry adder

Fig shows the simulation result for 4-bit ripple borrow subtractor done with the help of Xilinx12.1 and implemented in Spartan 3E FPGA board.



Fig 11.simulation of 4-bit ripple borrow subtractor

Fig shows the timing details for 4 bit ripple borrow subtractor done with the help of Xilinx12.1.

Delay:	9.208ns	(Levels o	f Logic	= 6)
Source:	bin (PAD)			
Destination:	bout (PAI	0)		
Data Path: bin to	bout			
		Gate	Net	
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)
IBUF:I->0	2	1.106	0.532	bin_IBUF (bin_IBUF)
LUT3:10->0	2	0.612	0.532	a1/bout1 (c<0>)
LUT3:10->0	2	0.612	0.532	a2/bout1 (c<1>)
LUT3:10->0	2	0.612	0.532	a3/bout1 (c<2>)
LUT3:10->0	1	0.612	0.357	a4/bout1 (bout OBUF)
OBUF: I->O		3.169		bout_OBUF (bout)
Total		9.208ns	(6.723	ns logic, 2.485ns route)
			(73.0%	logic, 27.0% route)

Fig 12.Timing details of 4-bit ripple carry adder

Fig shows the simulation result for modified 4-bit ripple carry adder done with the help of Xilinx12.1 and implemented in Spartan 3E FPGA board.

									Ī
Name	Value	mlum	1,999,994 ps	1,999,995 ps	1,999,996 ps	1,999,997 ps	1,999,998 ps	1,999,999 ps	1
▶ 臂 b[3:0]	0101				0101				T
l <mark>e</mark> cin	0								
🕨 🙀 cond[4:0]	10000				10000			-	2
🕨 😽 Sum[3:0]	1111				1111				2
Cout	0								
🕨 🧏 ca[4:0]	00000				00000				2
▶ 🎇 s[4:0]	11111			-	11111				1
🕨 👹 f[9:0]	1001100000				1001100000				2
▶ 💐 sel1[4:0]	10000				10000				2
🕨 👹 sel[2:0]	111	-			111				2
▶ 👹 sel2[3:0]	0000				0000				2
🕨 👹 text[110:0]	ADDERS 1,2,3,4				ADDERS 1,2,3,4				2
🕨 👹 text1[110:0]	GOOD CONDITION				GOOD CONDITION				2
		-		·					-

Fig 13.simulation of modified4-bit ripple carry adder

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Fig shows the timing details for modified 4 bit ripple carry adder done with the help of Xilinx12.1.

elay:	8.304ns	(Levels o	of Logic	: = 6)
Source:	b<1> (PA	D)		
Destination:	Cout (PA	D)		
Data Path: b<1> t	o Cout			
		Gate	Net	
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)
IBUF:I->0	5	1.106	0.690	b 1 IBUF (b 1 IBUF)
LUT4:10->0	1	0.612	0.000	Cout31 (Cout3)
MUXF5:I1->0	3	0.278	0.481	Cout3 f5 (Cout bdd8)
LUT3:12->0	1	0.612	0.387	Cout SWO (N6)
LUT4:12->0	1	0.612	0.357	Cout (Cout OBUF)
OBUF:I->0		3.169		Cout_OBUF (Cout)

Fig 14.Timing details of modified 4-bit ripple carry adder

Fig shows the simulation result for 4 bit ripple borrow subtractor done with the help of Xilinx12.1 and implemented in Spartan 3E FPGA board.

Name	Value	 1,999,994 ps	1,999,995 ps	1,999,996 ps	1,999,997 ps	1,999,998 ps	1,999,999 ps	2
▶ <table-of-contents> a[3:0]</table-of-contents>	1111	 		1111				5
b[3:0]	0000			0000				5
1 bin	0							
▶ 🎬 cond[4:0]	01000			01000				5
Dif[3:0]	1111			1111				Ĵ.
Le Bor	1							1
▶ 🍕 ca[4:0]	00000			00000				2
▶ 🍕 s[4:0]	11111			11111				5
▶ ₩ 1[9:0]	1010100000			1010100000				Ĵ.
sel1[4:0]	01111			01111				b.
▶ 🌃 sel[2:0]	000			000				5
sel2[3:0]	0001			0001				Ċ.
 text[110:0] 	RACTOR 2,3,4,5			RACTOR 2,3,4,5				b.
 text1[110:0] 	GOOD CONDITION			GOOD CONDITION	1			Ĵ.

Fig 15.simulation of modified 4-bit ripple borrow subtractor

Fig shows the timing details for modified 4 bit ripple borrow subtractor done with the help of Xilinx12.1.

Delay:	8.328ns	(Levels o:	f Logic	: = 6)
Source:	bin (PAD))		
Destination:	Dif<1> ()	PAD)		
Data Path: bin t	Dif<1>			
		Gate	Net	
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)
IBUF: I->0	5	1.106	0.690	bin IBUF (bin IBUF)
LUT4:10->0	1	0.612	0.000	Dif<1>112 (Dif<1>111)
MUXF5:10->0	2	0.278	0.532	Dif<1>11 f5 (Dif<1> bdd0)
LUT4:10->0	1	0.612	0.360	Dif<1>160 SW0 (N6)
LUT4:13->0	1	0.612	0.357	Dif<1>160 (Dif 1 OBUF)
OBUF: I->O		3.169		Dif_1_OBUF (Dif<1>)
Total		8.328ns	(6.389	ns logic, 1.939ns route)
			(76.7%	logic, 23.3% route)

Fig 16.Timing details of modified 4-bit ripple borrow subtractor

Fig shows the simulation result for modified 4-bit ripple borrow subtractor 2's complement done with the help of Xilinx12.1 and implemented in Spartan 3E FPGA board.

-								
Name	Value	 1,999,994 ps	1,999,995 ps	1,999,996 ps	1,999,997 ps	1,999,998 ps	1,999,999 ps	2,
🕨 🎽 a[3:0]	1111			1111				Г
▶ 🎽 b[3:0]	0000			0000				2
l <mark>e</mark> bin	0							
▶ 🎽 cond[4:0]	01000			01000		-		2
Dif[3:0]	1111			1111				1
Bor	1							1
▶ 🍢 ca[4:0]	00000			00000				2
▶ 🍢 s[4:0]	11111			11111				1
▶ 🍢 f[9:0]	1010100000			1010100000				2
▶ 🌃 sel1[4:0]	01111			01111				1
▶ 🍯 sel[2:0]	000			000				2
▶ <table-of-contents> sel2[3:0]</table-of-contents>	0001			0001				1
▶ <table-of-contents> text[110:0]</table-of-contents>	RACTOR 2,3,4,5			RACTOR 2,3,4,5				1
▶ 📢 text1[110:0]	GOOD CONDITION			GOOD CONDITION				2

Fig 17.simulation of modified 4-bit ripple borrow subtractor

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Fig shows the timing details for modified 4 bit ripple borrow subtractor 2's complement done with the help of Xilinx12.1.

Delay:	8.328ns	(Levels o	f Logic	: = 6)
Source:	bin (PAD))		
Destination:	Dif<1> (1	PAD)		
Data Path: bin t	o Dif<1>			
		Gate	Net	
Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)
IBUF: I->0	5	1.106	0.690	bin IBUF (bin IBUF)
LUT4:10->0	1	0.612	0.000	Dif<1>112 (Dif<1>111)
MUXF5:10->0	2	0.278	0.532	Dif<1>11 f5 (Dif<1> bdd0)
LUT4:10->0	1	0.612	0.360	Dif<1>160 SW0 (N6)
LUT4:13->0	1	0.612	0.357	Dif<1>160 (Dif 1 OBUF)
OBUF: I->O		3.169		Dif_1_OBUF (Dif<1>)
Total		8.328ns	(6.389	ns logic, 1.939ns route)
			(76.7%	logic, 23.3% route)

Fig 18. Timing details of modified	4-bit ripple borrow subtractor
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Adder / Subtractor	Delay	Auto Correction
4 bit adder	8.959ns	No
4 bit Subtractor	9.208ns	No
Modified 4 bit adder	8.304ns	Yes
Modified 4 bit Subtractor	8.328ns	Yes

TABLE1. COMPARISON OF ADDER AND SUBTRACTOR

V. CONCLUSION

The proposed full adder/subtractor system has been simulated and results are compared with existing full adder/subtractor system in terms of performance and delay. This proposed adder/subtractor system is having improvement in both of these aspects. The system is designed in auto correction format which is done with the help of extra one full adder/subtractor and multiplexer.

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