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A Highly Linear CMOS LNA

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Abstract: In this work, a highly linear Cascode CMOS LNA is presented. Linearity issues in RF receiver frontend are discussed, followed by an analysis of the specifications and requirements of a LNA through consideration of multi-standard LNA. Device non-linear characteristics cause linearity problems in the RF front-end system. To solve this problem, Post linearization technique for inductively degenerated (L-deg) common source Cascode Low Noise Amplifier is presented, which improves linearity performance with small gain loss and current consumption as consequence. The LNA presented has 1.0GHz – 3.2GHz frequency range designed using TSMC 0.18 μ m CMOS process. The linearized LNA achieves an IIP3 of +5.0 dBm, with P-1dB of -14 dBm, 13.8 dB gain (max), NF 2.03dB and power utilization of 19.4 mW at 1.8 volt power supply.

Keywords: Low noise amplifier (LNA), complementary metal oxide semiconductor (CMOS), nonlinearity, third-order input intercept point (IIP3), third-order intermodulation distortion (IMD3)

I. INTRODUCTION

Communication technology is moving toward a major milestone. The tremendous growth of the wireless industry, global access to the internet, and the ever growing demand for high speed data communication are spurring us toward fast developments in communication technology. Today's Smart phone have need of GSM for cellular communications, Wi-Fi/WLAN for internet connectivity, Bluetooth for short range connectivity and data transfer between itself and another phone, and GPS for navigation. The challenge is to find a way to integrate all these radios in these multi-radio platforms for cost-effective solutions; a reduction in the number of front-end receivers per device is the way to go. RF designers are strained to develop new methodologies that allow the design of such novel products.

A unique component of any RF receiver is in the front-end low-noise amplifier (LNA) that interacts with the incoming signal. Due to the possible large interference signals at the input of the low-noise amplifier (LNA), it has to provide high linearity, thus preventing the inter modulation tones created by the interference signal from corrupting the carrier signal [1]. This linearity improvement should not be at the expense of gain or noise figure (NF). This demands the use of linearization techniques implemented with minimal current overhead.

The linearity of CMOS is gets worse as the process scales down [2], which has motivated several linearization techniques [3]. Negative feedback techniques to obtain linearity cannot be easily used at RF frequencies due to stability reasons and, hence, demanding different linearization techniques.

The LNA in [4] and [5] is linearized using the fact that third-order derivative of dc transfer characteristics of MOSFET, which is responsible for third-order nonlinearity, changes from positive to negative in the moderate inversion region. Thus, a MOSFET biased at the crossover point attains best linearity, but the region over which this linearity boost can be obtained is very narrow and the bias point is bound to change due to process variations leading to a very sensitive and limited improvement.

The major drawback of this technique is that the transistor has to be biased at the "sweet spot," hence, limiting the trans conductance of the input stage leading to reduced gain and increased NF.

Until now, the most efficient reported linearization method for CMOS LNA is the derivative superposition technique [1], [6] which nulls the negative 3rd order derivative of the dc transfer characteristic (g_{m3}) of the main amplifier by paralleling the auxiliary amplifier biased near the weak inversion region with the positive g_{m3} .

Despite the outstanding improvements in the linearity, the DS method have difficulties in controlling the quality factor (Q) of the input matching network which plays a key role for low noise optimization [7], [8]. Other drawback with the DS method is that it is valid only at low frequencies at which the effect of circuit reactance is negligible [9].

In this paper, we present a post-linearization technique for the Cascode CS LNA with the concept of IMD sinking [10]. In the proposed method, the IMD3 can be partially cancelled by the additional folded diode with a parallel RC circuit. In addition, it will be not at the expense of gain, NF and current consumption, which is suitable for the high-frequency and high-linearity Cascode CS LNAs.

II. PROPOSED LOW NOISE AMPLIFIER

The circuit of proposed inductively degenerated (L-deg) common source Cascode Low Noise Amplifier (LNA) is as shown in the Fig. 1

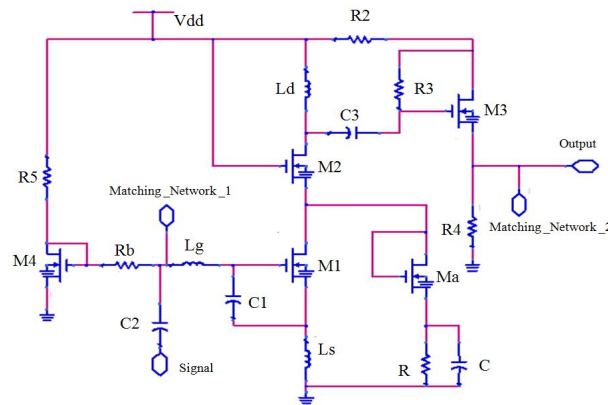


Fig. 1 Complete Schematic of proposed L-deg common source CascodeLNA

The schematic of Cascode LNA shown in Fig. 1 comprises of input matching inductors L_s and L_g along with Capacitor C_1 and C_2 . Capacitor C_1 is connected to increase the effective C_{gs} of MOSFET M1 so that it can match to wide frequency spectrum. The real part of the input impedance is adjusted using the source inductor L_s , while the imaginary part is removed at resonance using the inductor L_g . M1 is the main amplifying device whereas M2 is responsible to have high reverse isolation and to compliment stability [11].

Adding M2 increases Noise in the circuit but still it can be neglected foreseeing the advantages. Inductor L_d provides the necessary sufficient gain so that signal can get amplified. Capacitor C_3 couples the signal to next stage. MOSFET M3 is connected as Source follower/buffer so that it acts as unity gain amplifier and aids in matching output impedance. This is done to match the impedances of test equipment or mixer which is connected after LNA. Resistor R_b is a high value resistance forms a part of DC bias to keep MOSFET M1 is saturation region. It is connected so as to make the ac signal to enter into amplifying device only and not in other paths.

LNA biasing is done with the help of constant current source which is provided by current mirror [11]. T-match network is used for matching purpose in the circuit. M_a is an auxiliary transistor with a parallel RC circuit as an intermodulation distortion (IMD) sinker [10].

The L-deg CS LNA topology is also called as Simultaneous Noise and Input matching topology (SNIM) as this topology takes care of two things as matching of input impedance and minimizing the amount of noise in the circuit as there is no added physical resistor [16].

Only one Inductor can prove to be sufficient to have an input match condition (connected to source) but an extra Inductor is added at the gate terminal. This is done so as to compliment the input impedance matching by adding an extra degree of freedom in the value of L_s [17]. Another objective of adding L_g is, most of DC and AC currents flow from L_s , hence it is somewhat incapable in providing the required impedance for a stable system. A common source input stage offers the possibility to achieve the best noise performance by increasing their input quality factor Q . However, it degrades the linearity and increases the sensitivity of the input matching [12]. Its minimum noise factor including channel thermal noise and induced gate noise is given by:

$$F_{min} = 1 + 1.41 \frac{\gamma}{\alpha} \left(\frac{\omega_o}{\omega_T} \right) \quad \dots (1)$$

Where, ω_o is the operating frequency, $\omega_T = g_m / C_{gs}$ is the unity current gain frequency of the MOSFET, and α , γ and δ are process dependent parameters.

Input Quality Factor of inductively degenerated Structure is as follows [16]:

$$Q_{in} = \frac{1}{\omega C R}$$

$$\begin{aligned}
 &= \frac{1}{\omega C_{gs}(R_s + g_m L_s / C_{gs})} \\
 &= \frac{1}{\omega(C_{gs} R_s + g_m L_s)} \\
 &= \frac{1}{2\omega C_{gs} R_s} \dots (2)
 \end{aligned}$$

A lower Q_{match} results in a wider BW. Due to the relatively high Q of CS-LNAs' matching network, the CS-LNA cannot meet UWB matching requirements without advanced design techniques [13], [14].

III. PROPOSED LINEARIZATION METHOD

Frontend nonlinearity originates from two major sources as [3]: (i) g_m non-linearity and (ii) g_{ds} non-linearity. This work deals with g_m linearization technique. Linearization is mainly done to minimize the power of image signal. If LNA is not linear enough, the power of image signal might be similar to that of main signal which would make the main signal indistinguishable. In other words, the Minimum detectable Signal of the system is dominated by the image signal generated due to cross terms present in the non-linear devices [9].

To improve the linearity of the Cascode CS LNA, several linearization methods have been proposed [1][2][15], which are usually evaluated with the IIP3. To suppress the nonlinearity of the amplifier, the third-order derivative coefficient has to be close to zero [3].

In this paper, we present a post-linearization technique for the Cascode CS LNA with the idea of IMD sinking [10]. In the proposed method, the IMD3 can be partially cancelled by the supplementary folded diode with a parallel RC circuit. In addition, there is not so much expense of gain and current consumption, which is appropriate for the high-frequency and high-linearity Cascode CS LNAs.

Similar to the derivative superposition (DS) method, the post-distortion (PD) technique also utilizes an auxiliary transistor's nonlinearity to cancel that of the main device, but it is more sophisticated in two aspects [3]:

- 1) The auxiliary transistor is connected to the output of main device instead of directly to the input, minimizing the impact on input matching.
- 2) All transistors operate in saturation, resulting in more robust distortion cancellation.

A. Concept Of Post Distortion Technique

The conceptual view of proposed linearization technique is as shown in the Fig. 2.

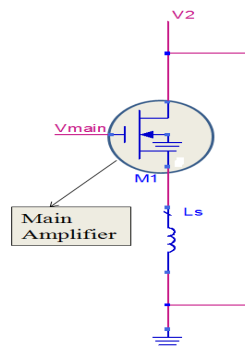


Fig. 2 Proposed linearization circuit

Here M1 is a main amplifying device and Ma is auxiliary transistor with a parallel RC circuit as intermodulation distortion (IMD) sinker. We utilize the diode (Ma) and resistor (R) as shown in Fig. 2 to generate the i_{Ma} , and choose the proper size of the diode and resistor for linearity optimization. It should be noted that the IIP3 is independent of varying capacitance (C), because the C is for ac ground [10].

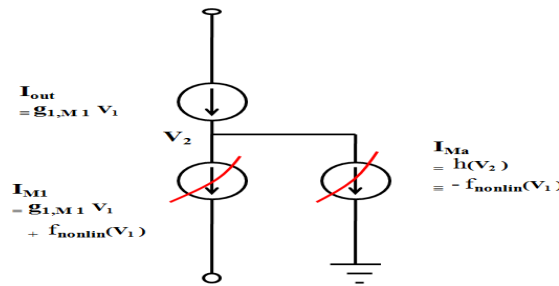


Fig. 3 Conceptual view of the proposed linearization technique

The auxiliary transistor Ma taps voltage V_2 and replicates the nonlinear drain current of the main transistor M1, partially cancelling both second and third order distortion terms [3]. The nonlinear drain currents of M1 and Ma can be modeled as:

$$i_{M1} = g_{1,M1} V_1 + g_{2,M1} V_1^2 + g_{3,M1} V_1^3 \dots (3)$$

$$i_{Ma} = g_{1,Ma} V_2 + g_{2,Ma} V_2^2 + g_{3,Ma} V_2^3 \dots (4)$$

Suppose V_1 is related to V_2 by

$$V_2 = -b_1 V_1 - b_2 V_1^2 - b_3 V_1^3 \dots (5)$$

Where $b_1 - b_3$ are generally frequencies dependent and can be extracted from simulation.

The two nonlinear currents i_{M1} and i_{Ma} sum at node V_2 , yielding i_{out} [3]:

$$\begin{aligned} i_{out} &= i_{M1} + i_{Ma} \\ &= (g_{1,M1} - b_1 g_{1,Ma}) V_1 \\ &\quad + (g_{2,M1} - b_1^2 g_{2,Ma} - b_2 g_{1,Ma}) V_1^2 \\ &\quad + (g_{3,M1} - b_1^3 g_{3,Ma} - b_3 g_{1,Ma} \\ &\quad \quad - 2g_{2,Ma} b_1 b_2) V_1^3 \dots (6) \end{aligned}$$

Note that in the PD method, both the main and auxiliary transistors drive in saturation with the same $g_{1,2,3}$ polarity. Hence, Ma partially cancels the linear term as well [10]; however, it does not substantially degrade the gain/NF because Ma is designed to be more nonlinear than i_{M1} .

It is observed that the proposed linearization technique can introduce the degree of freedom $g_{2,Ma,HB}$ and $g_{3,Ma,HB}$, which partially cancels the second-order and third-order distortion terms. Besides, the second-order nonlinearity also contributes to third-order intermodulation (IM3) product. Thus, the proposed technique uses the diode (Ma) and resistor (R) to decide the magnitude and phase of second- and third-order nonlinearity contribution to IM3 product [10] [15]. The composite 2nd-order coefficient has the opposite phase with respect to the composite 3th-order coefficient. It can partially cancel the contribution from 2nd-order nonlinearity to IM3 product, resulting in a small IM3 product at the output [10]. Thus, the linearity can be effectively improved.

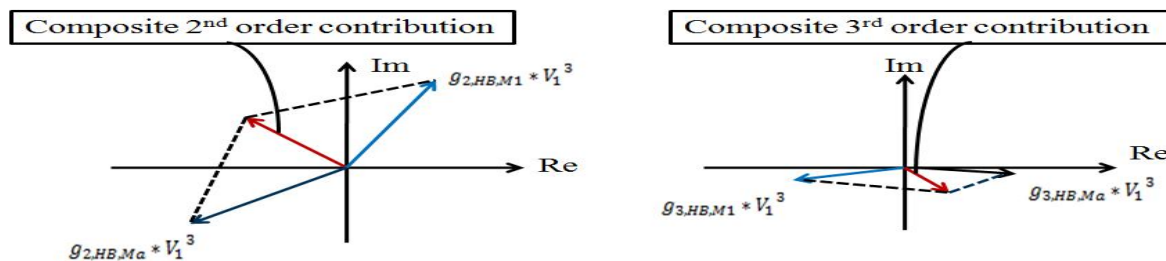


Fig. 4 Vector diagram of the proposed technique for the IM3 products

It is observed that proper choice of the diode and resistor size can increase the linearity of LNA. It should be noted that the resistor (R) provides the voltage drop required to control the voltage across the diode [10].

IV. RESULTS AND GRAPHS OF CS LNA

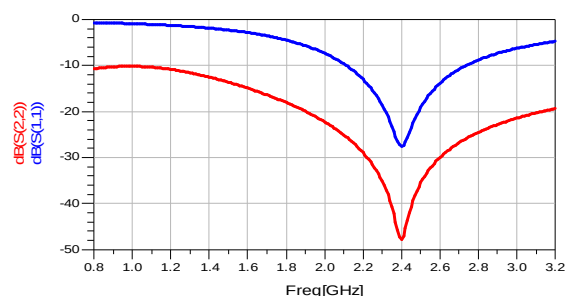


Fig.5 Input and output reflection coefficient of LNA

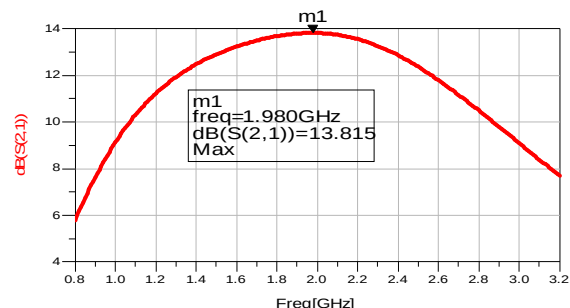


Fig. 6 Gain of LNA

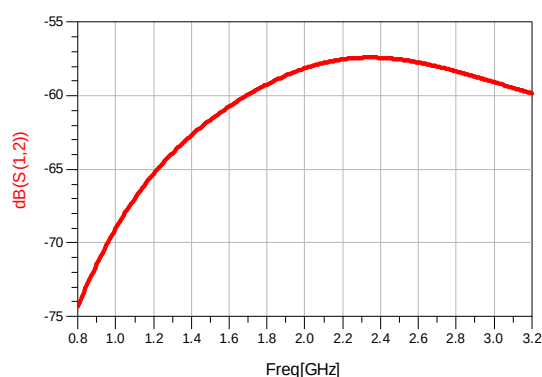


Fig. 7 Reverse Isolation of LNA

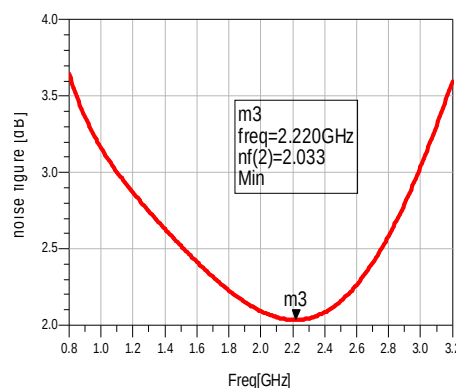


Fig. 8 Noise Figure of LNA

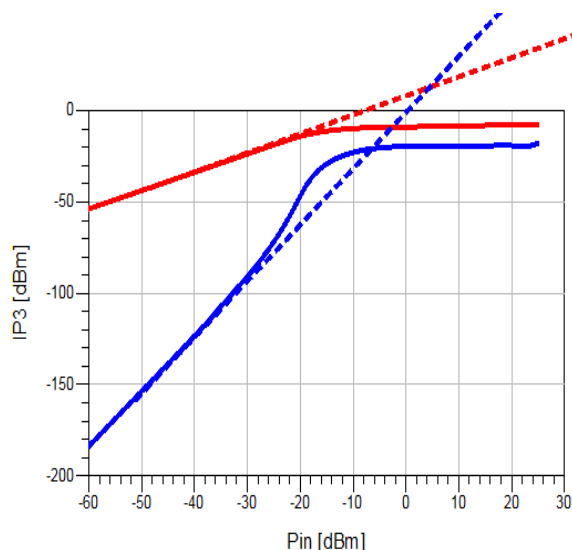


Fig. 9 IIP3 of LNA

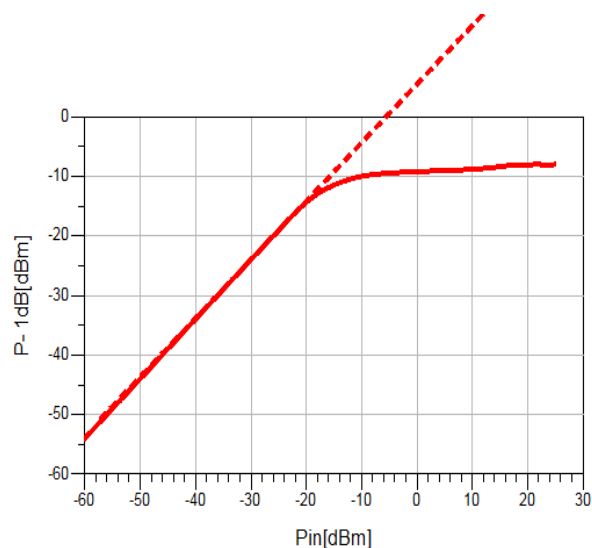


Fig. 10 "1-dB" compression point of LNA

The simulations and analysis of LNA circuit are carried out using Agilent's ADS tool. The technology schematic is developed with the help of TSMC 0.18 μ m CMOS process. The analysis is done at 1.8 V supply voltage. Harmonic Balance analysis is performed at a frequency of 2 GHz with a frequency spacing of 10MHz between the two tones.

V. CONCLUSION

In this paper, we have shown how the post linearization technique can be used to improve the linearity of a common source low noise amplifier. The proposed technique adopts an additional folded diode with a parallel RC circuit as an intermodulation distortion (IMD) sinker [10]. LNA biasing is done with the help of constant current source which is provided by current mirror, which is used to overcome the effect of PVT variations. The measured results of LNA with linearization circuit show that it can improve linearity performance with small gain loss and current consumption penalty. Linearized LNA achieves 2.03 dB minimum noise figure along with maximum gain of 13.8 dB which is sufficient enough to amplify weak incoming signal. The Power consumption is 19.4 mW at 1.8 volt power supply for linearized LNA.

Harmonic balance analysis is performed at 2 GHz frequency having 10MHz spacing between the two tones. 1-dB compression point for linearized LNA has a value of -14 dBm which is high enough to handle strong signal.

Linearized LNA achieves IIP3 of +5 dBm sufficient enough to decrease amplitude of third order intermodulations at the output.

VI. ACKNOWLEDGMENT

The authors would like to thank Taiwan Semiconductor Manufacturing Corporation, Limited (TSMC), for providing us the 0.18 μ m CMOS process PDK, due to which we were able to carry out research work.

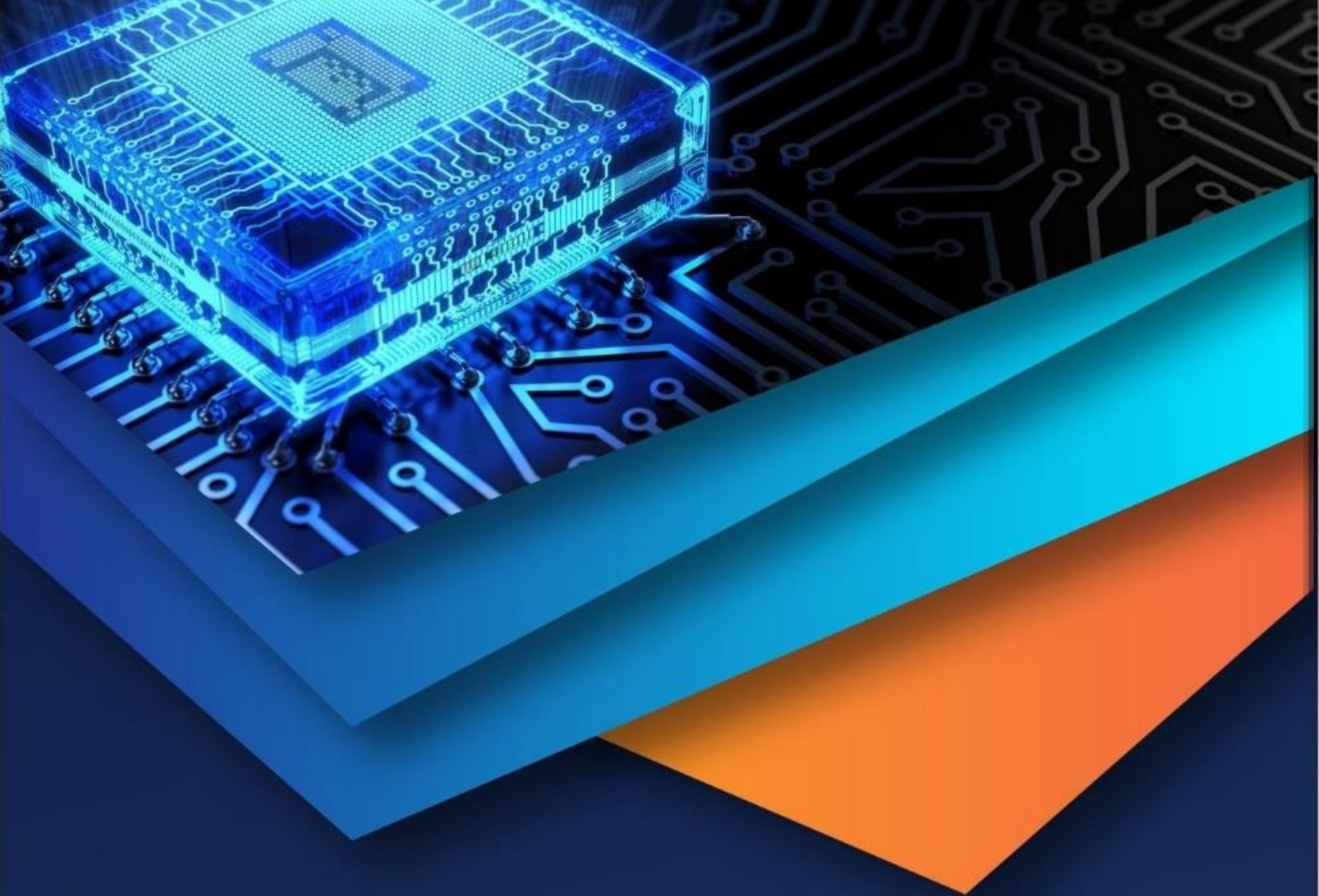
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Table 1: Comparison with others works

Reference	Frequency (GHZ)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Technology	Topology
[01]	0.9 – 2.4	10	2.85	15.6	21.1	0.35 μ m	CS LNA
[18]	0.1 – 6.5	14	4.2	+1	12	0.13 μ m	CS LNA
[19]	0.1 – 6.5	19	3	+1.0	11.7	0.13 μ m	Common gate
[20]	0.8 – 2.1	14.5	2.6	+16	17.4	0.13 μ m	Common gate
[21]	0.2 – 5.2	15.6	>0	<3.5	14	0.65 μ m	CG-CS Differential LNA
[22]	0.002 – 2.3	21	1.4	-1.5	18	90nm	Differential CMOS LNA
[23]	0.5 – 8.2	25	1.9 – 2.6	-4.0	41.85	90nm	Resistive feedback
[24]	0.5 – 7.0	21	2.9	-10.5	12	90nm	L-deg CS LNA
[25]	0.04 – 7.0	8.6	4.2 – 6.2	+3	9.0	0.18 μ m	Three stage distributed amplifier
This Work	1.0 – 3.2	13.8	2.08	+5.0	19.4	0.18 μ m	L-deg CS LNA



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