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DDS based Digital Frequency Transmission Design for Wireless Communication

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Abstract: ***The aim of this study is to model and design an efficient wireless system that should be easy to integrate with other technologies or infrastructures at a low cost. The input data is converted digitally using ADC and sent to FSK transmitter through FPGA. Verilog HDL has been used to implement the required functions of the FPGA. SIMULINK/MODELSIM software has been used to model and simulate Frequency-Shift Keying (FSK) Transmitter/ Receiver suitable for short-range communications. A two-tone FSK signal is generated, passed through a noisy channel, down converted to baseband and passed to FM detector to restore the original transmitted bit stream. The behavioral HDL design has been interfaced to the SIMULINK/MODELSIM model and the overall performance has been verified.***
Keywords: **SOPC Builder, transmission system, modulation, Demodulation**

I. INRODUCTION

Wireless communication is one of the fastest growing fields owing to its length and breadth of applications. Deep space communication is one such field where the use of wireless systems is indispensable. The most important issue in space communication is power and happens to be one of the major driving forces in the quest for low power wireless systems. We focus on the design of a low power FSK receiver intended specifically for deep space communications that involves an orbiter and a lander.

The receiver is designed and modeled in MATLAB and SIMULINK. We simulate the receiver and test it for data rates of 10kbps, 1kbps and 100bps. We design an FSK transmitted signal and test the receiver for such conditions.

We port the SIMULINK model to a XILINX hardware model using the system generation
features and block sets of SIMULINK.

The block set contains various building blocks for digital signal processing, communication and math operations. We simulate the XILINX model in SIMULINK and synthesize the model to a VIRTEX-2 FPGA using XILINX's optimized logi COREs. Then we perform static timing analysis and power analysis of the synthesized design. A control system is designed and developed in VHDL to take care of symbol and timing detection of the receiver. The system is tested, synthesized to XILINX hardware and interfaced to the receiver.

Digital modulation is the process by which digital symbols are transformed into waveforms that are compatible with the characteristics of the channel. In the case of baseband modulation these waveforms are pulses, but in the case of band pass modulation, the desired information signal is modulated to a sinusoid called a carrier wave. FSK modulation is a class of band pass modulation in which the frequency of the carrier varies in accordance with the information signal.

This paper constructs a modulation-demodulation model of digital frequency transmission system with DSP Builder based on FPGA/SOPC technique, simulates the waveforms with Simulink, creates VHDL text files supported by Modelsim software. After synthesis and compiling, corresponding program files pof and sof are created and downloaded to FPGA .

II. THE DESIGN OF MODULATION-DEMODULATION SIGNAL

Based on the principle of high frequency signal transmission system, the new-style DDS(Direct Digital Synthesizer) replaces VCO(analog Voltage Controlled Oscillator) to build ASK,FSK,PSK models, implements frequency switch quickly. The phase keeps continuous while frequency changes and digital modulation about frequency, phase and amplitude is implemented with Simulink/Modelsim and function module and IP core in DSP Builder.

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A. Frequency shift keying (FSK)

Frequency Shift Keying (FSK) system is a class of wireless systems that is very popular today and has widespread applications. An FSK system carries its information in the instantaneous frequency of the received signal. For e.g. a binary FSK system which transmits the symbols 0 and 1 have one frequency corresponding to the symbol 0 and another frequency to the symbol 1.

FSK systems are broadly classified into Coherent and Non-coherent systems. A coherent system requires carrier or phase synchronization at the receiver end in order to detect the signals whereas non coherent detection does not require any sort of synchronization. Consequently the design of non coherent systems is much simpler when compared to

coherent systems making them more popular when power is an important concern. But non coherent systems have a BER performance of 3db less than the traditional coherent receiver at a BER of 10E-5.

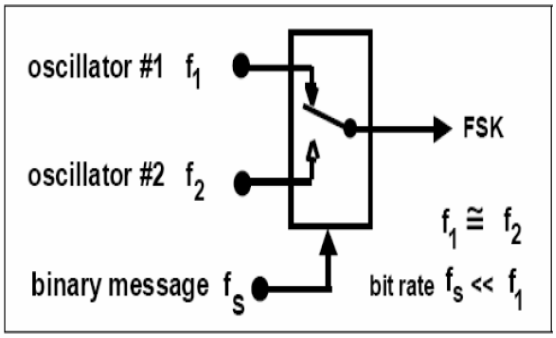

Fig1. An FSK transmitter

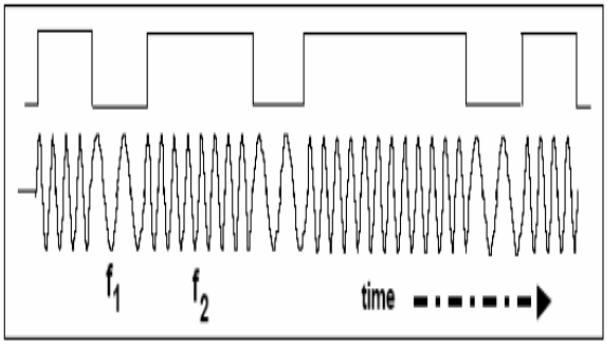

Fig2. An FSK waveform , derived from a binary message

B. The Design of 2FSK Modulation Model

Direct frequency modulation method is used to design 2FSK modulation model. The input of DDS module frequency word is controlled by digital baseband signal, the phase of accumulator is selected by multiplexer. By selecting different frequency word, the output of frequency is controlled by phase increment change and modulated frequency waveform with continuous phase is created, show as figure But in application, output data need to convert from digital to analog signal, then produce analog output signal through low-pass filter.

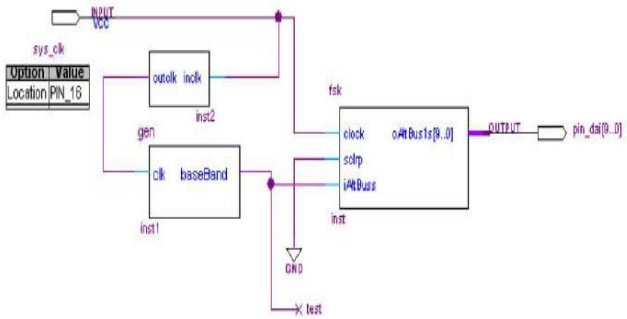

Fig3. Principle diagram of 2FSK modulation system

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III. FSK TRANSMITTER/RECEIVER SIMULINK IMPLEMENTATION

A detailed description of the simulated FSK transceiver model is given in this section

A. FSK Transmitter Model

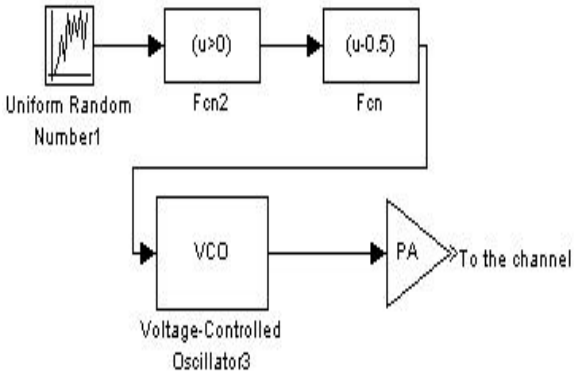

Fig4. Modeling FSK transmitter

A uniform random number generator is employed to output a random bit stream of 0 and 1's with a specific data rate. The input voltage to the Voltage Controlled Oscillator (VCO) is shifted either to □ 0.5 instead of 0 or 1. This is implemented in order to get an equal frequency shift for the both tones by multiplying this input value by the sensitivity of the VCO. The power amplifier (PA) is modeled to be a non-linear unit since it exhibits a higher efficiency of 60% for some of the power efficient modulation techniques as the FSK [6]. This can be explained, as the FSK waveforms have no abrupt phase change and exhibit a constant envelope. Therefore the FSK signals can therefore be amplified by means of nonlinear PAs with no spectral regrowth

B. FSK Receiver Model

Direct-conversion *homodyne* receiver is modeled as shown in Fig.8. The low-noise amplifier (LNA) represents the first gain stage in the receiver path and its noise figure is added directly to that of the system. A small signal non-linearity, compression, saturation, slew rate limiting, and two types of noise (white and flicker) are modeled within the (LNA) unit as shown in Fig.

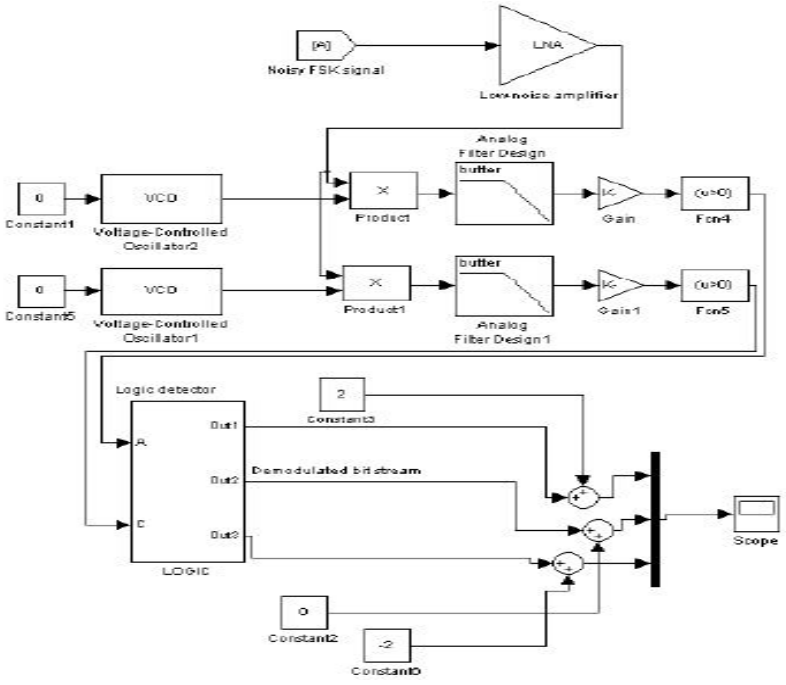

Fig5.Modeling FSK direct-conversion receiver

C. Xinlinx Implementation Of The Receiver

The receiver model developed in SIMULINK is useful to validate the functionality of the receiver design at a system level. In order to get a power estimate of the receiver, the SIMULINK model has to be reduced to hardware. As mentioned before, SIMULINK's XILINX block set allows us to develop a XILINX hardware model of the receiver using the
XILINX building blocks. This process basically reduces to translation of the SIMULINK model to a XILINX model provided a one to one correspondence exists between each and every block. The hardware model is developed and tested in SIMULINK and the system generator tools of XILINX is used to synthesize the model by generating .bit file targeted to a particular XILINX FPGA. A .bit file contains all the configuration information defining all the internal logic and interconnections in the FPGA.
The System Generator in XILINX is a very convenient method for electronic designs to be created, tested, and translated into hardware for XILINX FPGAs. The tool extends SIMULINK to support bit and cycle accurate system level simulation, and automatic code generation for XILINX FPGAs. System Generator co-simulation interfaces extend SIMULINK to incorporate FPGA hardware and HDL simulation into the system-level environment as naturally as other library blocks. System Generator presents a high level and abstract view of the design, but also exposes key features in the underlying silicon, making it possible to build extremely high-performance FPGA implementations.

D. System Generation Design Flow

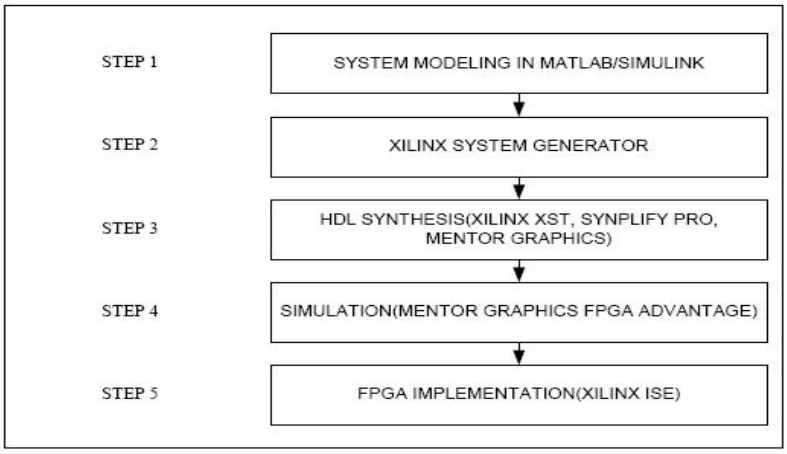

Fig6. XILINX System Generation Design Flow

1) *STEP1:* A high level system design of the model is developed and tested in MATLAB/SIMULINK using the XILINX block set provided in SIMULINK.
2) *STEP2:* System Generation is invoked in SIMULINK using the "XILINX System Generation" icon in the SIMULINK model. This process generates VHDL code for all the XILINX blocks in the SIMULINK design. FPGA designs are generated using XILINX's LogiCOREs to produce the most efficient implementation.
3) *STEP3:* The VHDL design is synthesized to FPGA using one of the three most popular synthesis tools namely XILINX's XST, SYNPLICITY's SYNPLIFY PRO and MENTOR GRAPHICS's FPGA Advantage.
4) *STEP4:* This step is optional and can be used to simulate the VHDL design using MENTOR GRAPHICS's FPGA Advantage. A test bench and data vectors can be created using the System Generator. The data vectors represent the input and the expected outputs as simulated in the SIMULINK design.
5) *STEP5:* The synthesized design is loaded into a XILINX FPGA using place and route tools of XILINX's ISE.

IV. CONCLUSIONS

An FSK transmitter suitable for short-range wireless communications has been implemented in SIMULINK. A detailed description for both transmitter and receiver units was given. Different channel propagation effects like noise, path loss, multipath fading, and interference were introduced in the model. The transceiver system performance was tested under different conditions. The implemented model showed a good capability in recovering the original data at the receiver side with different transmission frequencies. The simulation running time is considered to be the main limitation of using SIMULINK.

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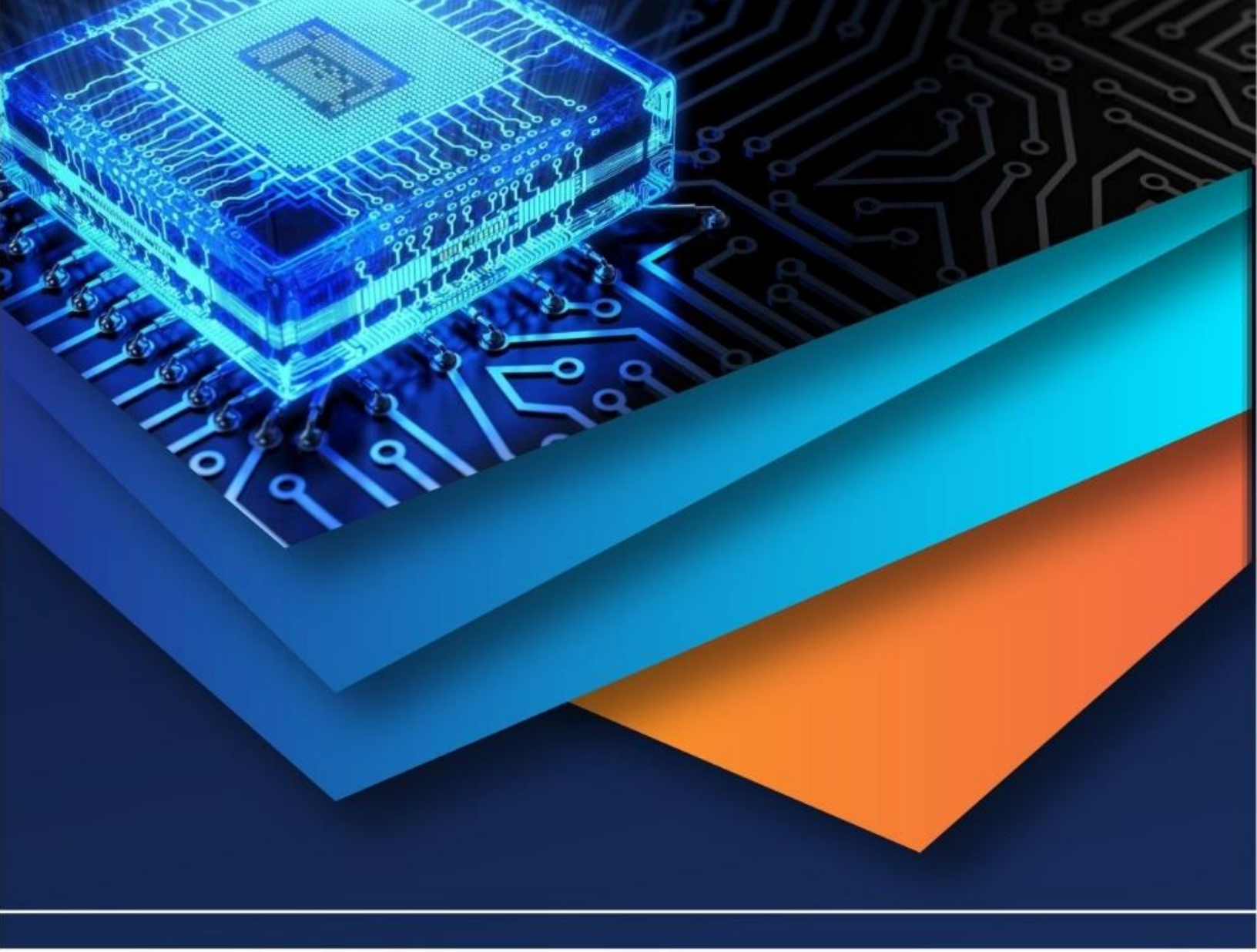

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