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A Multilevel Inverter with Reduced Number of Switches

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Abstract: This paper proposes a multilevel inverter with reduced number of switches. Compared to conventional inverters, the proposed VR topology for 17 level gives higher levelled MLI and thus harmonics is reduced. The use of an H bridge plays the key role of reducing the number of switches particularly for higher levels. Here, a new Sine Property method to adjust the step angles of each level in the output is implemented to reduce the harmonics in the output waveform.

I. LITERATURE REVIEW

This chapter briefly discusses the development of nonlinear transcendental Selective Harmonic Elimination (SHE) equation problem in control of multilevel inverter with an objective of controlling the chosen multilevel inverter configuration during whole range of modulation index from 0 to 1 with less %THD which complies with IEEE 519-1992 harmonic guidelines and also with less switching losses. Commercially existing topologies of multilevel inverters and modulation strategy for the control of multilevel inverters are briefly reviewed. It also reviewed the research progress of various techniques for solving non linear transcendental SHE equation problem. This chapter also presents the objective of research, research methodology and the thesis organization.

In order to meet the challenges such as high dv/dt causing voltage doubling effect in motor output voltage waveform, %THD to comply with IEEE 519-1992 harmonic guidelines, high electromagnetic interference (EMI), high common-mode voltages and requirements of synthesizing higher voltages for modern industrial applications have subsequently led the development of various inverter topologies [40]-[42]. The commercially existing inverter topologies are neutral point clamped (NPC) inverter, flying capacitor (FC) and cascaded H-bridge (CHB) inverter topologies and are briefly reviewed in next section. One of the traditionally accepted and widely used topology for various industrial and power sector applications is neutral point converter which was proposed by Nabae, Takahashi and Akagi in 1981[39]. As the two-level inverter has the drawback of achieving higher power levels with the available GTOs of 4.5kV voltage rating at that time, for traction applications, three-level inverter configuration was developed to meet the requirement of high voltage dc operation in traction application in Austrian railways [43]-[46]. Three-level neutral point converter often called as three-level diode-clamped inverter has found wide range application because of the advantages such as higher power handling capability, less dv/dt and less %THD when 21 compared to conventional two-level inverter. Later, direct extensions of the original NPC for higher number of levels are presented by several researchers in 1990s and presented experimental results for the applications such as variable motor drives, static var compensation and medium voltage systems interconnections [44]-[48].

A. Multilevel Inverter

Now a day's many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage. The multi level inverter as alternative in high power and medium voltage situations. The Multi level inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations.

B. Existing Method

Normal Inverters can be broadly classified into two types. They are

1) Voltage Source Inverter (VSI)
2) Current Source Inverter (CSI)

When the DC voltage remains constant, then it is called *Voltage Source Inverter (VSI)* or Voltage Fed Inverter (VFI).

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When input current is maintained constant, then it is called *Current Source Inverter (CSI)* or Current Fed Inverter (CFI). Sometimes, the DC input voltage to the inverter is controlled to adjust the output. Such inverters are called *Variable DC Link Inverters*. The inverters can have single phase or three-phase output.

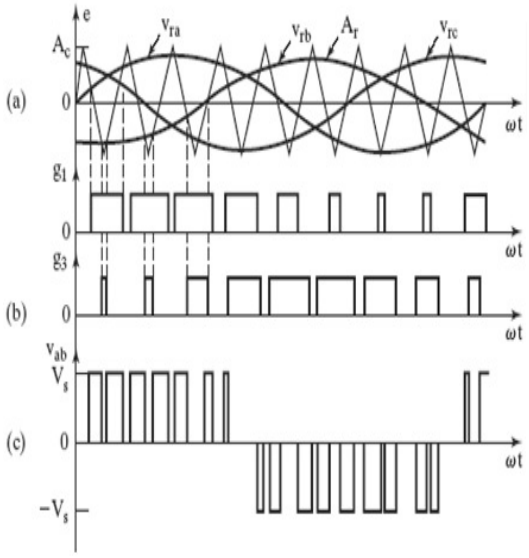
a) A voltage source inverter(VSI) is fed by a stiff DC voltage, whereas a current source inverter is fed by a stiff current source.

b) A voltage source can be converted to a current source by connecting a series inductance and then varying the voltage to obtain the desired current.

c) A VSI can also be operated in current-controlled mode, and similarly a CSI can also be operated in the voltage control mode.

The inverters are used in variable frequency ac motor drives, uninterrupted power supplies, induction heating, static VAR compensators, etc.

The following table gives us the comparative study between VSI and CSI Using analogue ICS generated the carrier and reference signals generated the PWMsignals.



C. Proposed Method

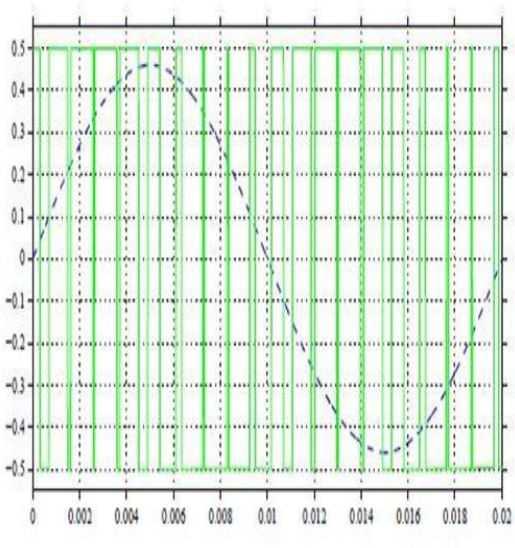
1) Diode Clamped Multilevel Inverter: The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage. It is the main drawback of the diode clamped multilevel inverter. This problem can be solved by increasing the switches, diodes, capacitors. Due to the capacitor balancing issues, these are limited to the three levels. This type of inverters provides the high efficiency and it is a simple method of the back to back power transfer systems.

2) Flying Capacitors Multilevel Inverter: The main concept of this inverter is to use capacitors. It is of series connection of capacitor clamped switching cells. The capacitors transfer the limited amount of voltage to electrical devices. In this inverter switching states are like in the diode clamped inverter. Clamping diodes are not required in this type and the output is half of the input DC voltage. It is drawback of the multi level inverter. It also has the switching redundancy within phase to balance theflaying capacitors. It can control both the active and reactive power flow. But due to the high frequency switching, switching losses will takes place.

II. CONCEPT OF MULTILEVEL INVERTER

First take the case of a two-level inverter. A two-level Inverter creates two different voltages for the load i.e. suppose we are providing *Vdc* as an input to a two level inverter then it will provide + *Vdc*/2 and – *Vd* on output. In order to build an AC voltage, these two newly generated voltages are usually switched. For switching mostly PWM is used as shown in the Figure 2.1, reference wave is shown in dashed blue line. Although this method of creating AC is effective but it has few drawbacks as it creates harmonic distortions in the output voltage and also has a high dv/dt as compared to that of a multilevel inverter. Normally this method works but in few applications it creates problems particularly those where low distortion in the output voltage is required.

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PWM voltage output of a two-level inverter

The concept of multilevel Inverter (MLI) is kind of modification of two-level inverter. In multilevel inverters we don't deal with the two level voltage instead in order to create a smoother stepped output waveform, more than two voltage levels are combined together and the output waveform obtained in this case has lower dv/dt and also lower harmonic distortions. Smoothness of the waveform is proportional to the voltage levels, as we increase the voltage level the waveform becomes smoother but the complexity of controller circuit and components also increases along with the increased levels. The waveform for the three, five and seven level inverters is shown in the F where we clearly see that as the levels are increasing, waveform becoming smoother.

A. Reduced Switch Multilevel Invereter

The proposed MLI generated fifteen level output without using bidirectional switches and capacitors. It consisted of four sources and diodes connected in between the switches S1, S2, S3, andS4 as shown in the Figure 1. The sources V1, V2, V3 and V4 generate voltages in the ratio 8:4:2:1 respectively. The H-Bridge inverter uses the four sources in series as its voltage source. The sources V1-V4 can be connected or disconnected using the switches S1-S4 respectively for producing different voltage levels. Switches S5-S6are used to control the direction of current flow and hence produces alternating output across the load. For the generation of 15 level output, an Diode clamped MLI requires 24 Switching devices, 60 diodes and 12 dc link capacitors whereas in the proposed topology, it requires only 8 switching devices and 4 diodes to generate same fifteen level output.

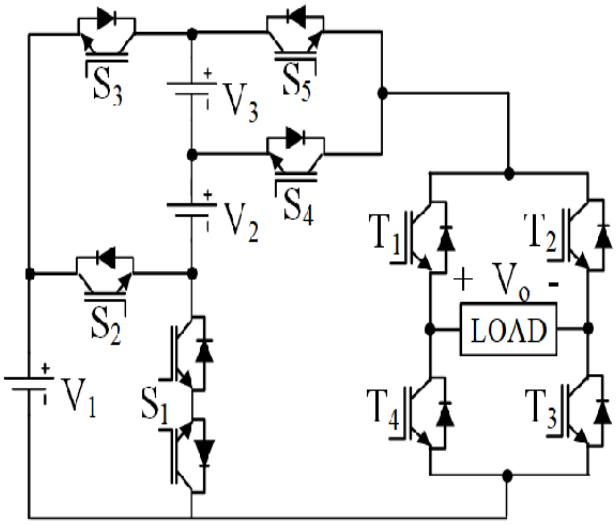


Fig. 1: Circuit diagram of the proposed multilevel inverter

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B. Analysis of FPGA Control

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks. Although one-time programmable (OTP) FPGAs are available, the dominant types are SRAM based which can be reprogrammed as the design evolves. - Learn More

C. Difference Between an ASIC and an FPGA

ASIC and FPGAs have different value propositions, and they must be carefully evaluated before choosing any one over the other. Information abounds that compares the two technologies. While FPGAs used to be selected for lower speed/complexity/volume designs in the past, today's FPGAs easily push the 500 MHz performance barrier. With AAunprecedented logic density increases and a host of other features, such as embedded processors, DSP blocks, clocking, and high-speed serial at ever lower price points, FPGAs are a compelling proposition for almost any type of design. - Learn More

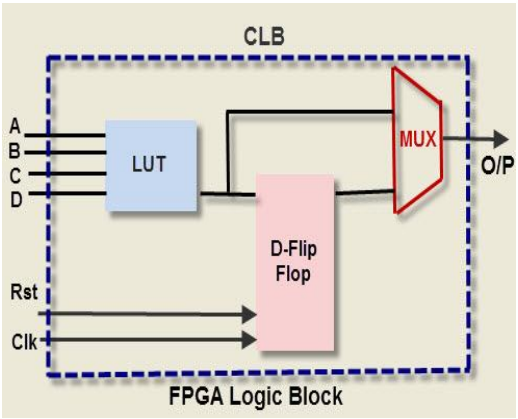
D. FPGA Applications

Due to their programmable nature, FPGAs are an ideal fit for many different markets. As the industry leader, Xilinx provides comprehensive solutions consisting of FPGA devices, advanced software, and configurable, ready-to-use IP cores for markets and applications such as:

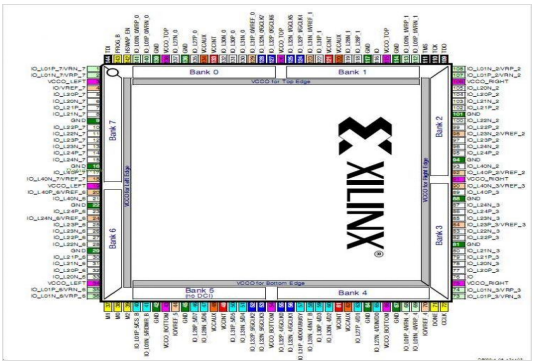
1) Aerospace & Defense - Radiation-tolerant FPGAs along with intellectual property for image processing, waveform generation, and partial reconfiguration for SDRs.

2) ASIC Prototyping - ASIC prototyping with FPGAs enables fast and accurate SoC system modeling and verification of embedded software

E. FPGA Logic Block



F. FPGA Pin Details



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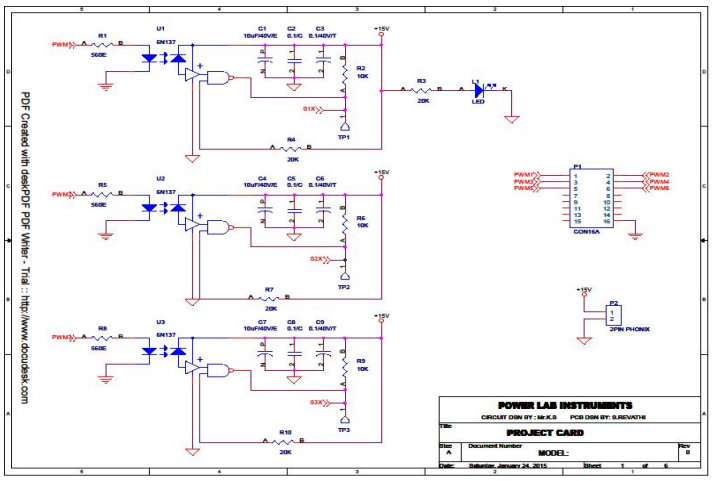
G. LCD Details

Pin No.	Symbol	Level	Description
1	V_{SS}	0V	Ground
2	V_{DD}	5.0V	Supply Voltage for logic
3	VO	(Variable)	Operating voltage for LCD
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read(MPU→Module) L: Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bus line
8	DB1	H/L	Data bus line
9	DB2	H/L	Data bus line
10	DB3	H/L	Data bus line
11	DB4	H/L	Data bus line
12	DB5	H/L	Data bus line
13	DB6	H/L	Data bus line
14	DB7	H/L	Data bus line
15	A	—	Supply power for LED +
16	R	—	Supply power for Red -
17	G		Supply power for Green -
18	B		Supply power for Blue -

H. Switching States Of Five Level

Voltage (Vo)	S1	S2	S3	S4	S5	S6	S7	S8
0	0	1	0	1	1	0	1	0
V_{dc}	1	0	0	1	0	1	0	1
$2\ V_{dc}$	1	1	0	0	1	1	0	0
$-\ V_{dc}$	0	1	0	1	1	0	0	1
$-2\ V_{dc}$	0	0	1	1	0	0	1	1

I. Hardware Details



This power module is designed and study of multilevel inverter. Its consist of Optocoupler, driver section, Igbt module.

1) Optoxoupler is used to isolate the control circuit from power circuit.
2) Driver circuit is designed to connect the gate directly to voltage bus.
3) Gate driver acts as a high power buffer stage between pwm output of control device and gate of primary switching device.

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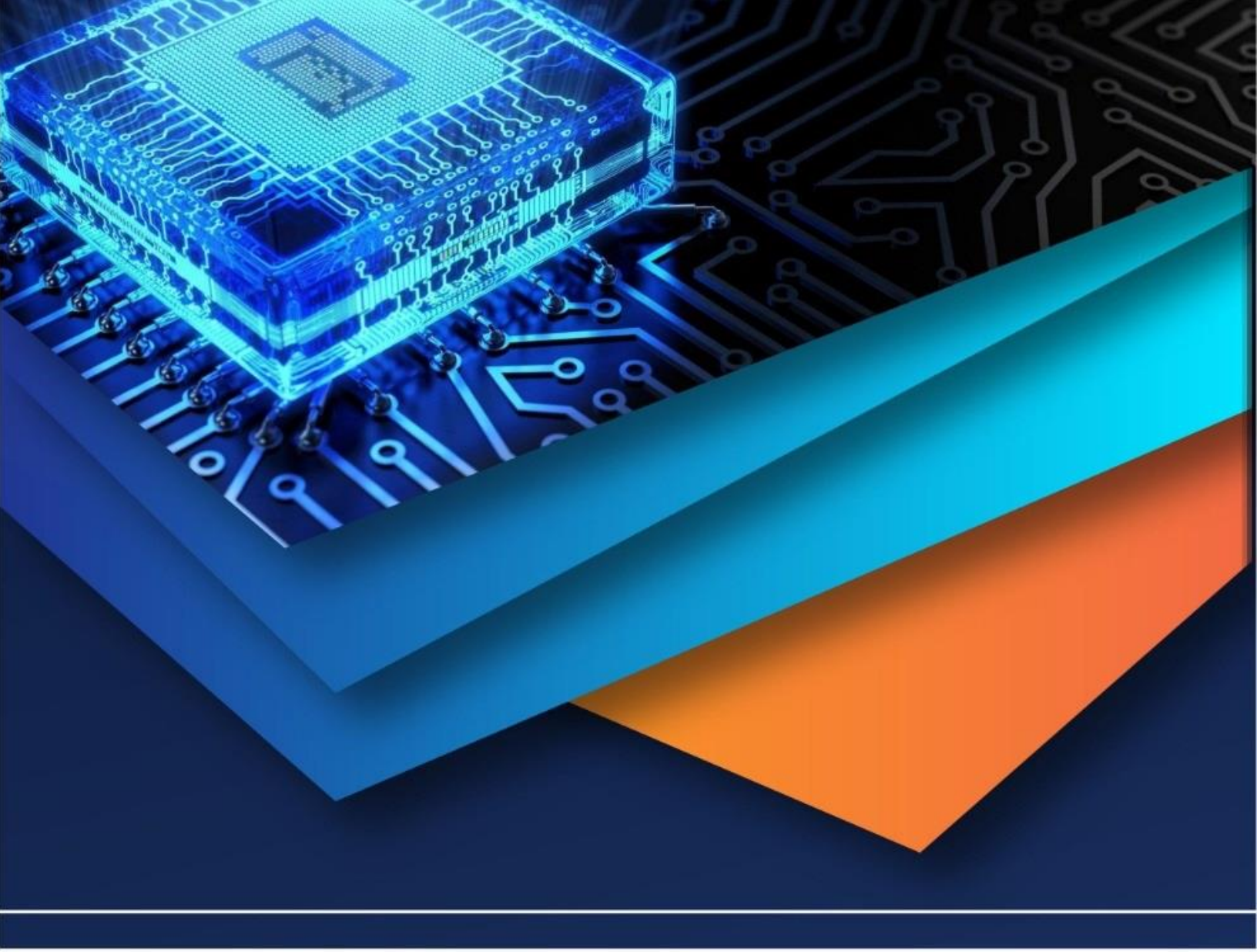
III. CONCLUSION

This project is based on multilevel inverter,. In this project we make the pulse arrangement and the multilevel inverter topology along with its feature extraction system in which we calculate the voltage, and observe the waveform

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