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Stuck-at-Faults: A Survey

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Abstract: This paper gives the detailed study of stuck-at-faults and its functionalities for various circuits. Test vectors generation and testing time of fault model also be studied. A survey about the single stuck faults and double stuck faults and proposed method for fault diagnosis were discussed in this paper.
Keywords: Stuck-at fault, Test vector, ATPG.

I. INTRODUCTION

A fault model is used to check a circuit with efficiency supported its structure instead of on its practicality. one The fault model is associate abstraction of the physical faults which have a tendency to try and discover. however, this higher exactness is obtained at the expense of a lot of advanced test generation algorithms and longer test times.

Fault models will describe the faults at completely different abstraction levels. the foremost common abstraction level is that the gate level, however fault models exist that describe faults at the semiconductor level in addition as on higher levels. Most fault models assume that the circuit solely contains one fault, as the number of potential multiple fault combos is therefore massive that test generation becomes impracticable. A wide used fault model for synchronous circuits is that the (input) stuck-at fault model.

In this fault model, it's assumed that a physical fault will be modelled as a symptom within the circuit being either stuck-at-O or stuck-at-1. A gate will have either an input stuck-at-0 or stuct-at-1, or the output stuck-at-0 or stuck-at-1. Thus, a gate with n inputs has 2(n + 1) completely different possible stuck-at faults. A wire branching bent on n gates additionally has 2(n + 1) stuck-at faults: 2 at the "input" to the wire and 2 for every of the n end- points.

A simpler fault model solely considers faults on the outputs of the gates. A wire branching bent on n gates has solely 2 completely different faults, freelance of n, equivalent to the complete internet being either stuck-at-0 or stuck-at-1. This fault model is termed the output stuck-at fault model.

II. PATTERN GENERATION DIAGNOSIS

Stuck-at test generation has been accustomed generate tests for stuck-open faults techniques developed for stuck-at test generation strategies are applied to discover stuck-open faults. but within these early studies 100% fault potency either for stuck-at or for stuck-open faults wasn't continuously achieved in the experimental results. These days, many efficient techniques are developed for the stuck-at test generation drawback, together with redundancy identification techniques. As a result, for nearly all circuits, 100% stuck-at fault potency are often achieved.

Detection of stuck-open faults needs consecutive 2 test vectors, defects inflicting delays are possible to be detected by increasing stuck-open fault coverage. The test vectors that discover all the stuck-open faults in an exceedingly gate will detect all the transition faults of the gate. thus increasing stuck-open fault coverage victimisation. stuck-at test vectors are often effective in increasing the defect coverage of recent LSIs.

The author [1] proposed the method consists of the following three steps.

1) *Step 1:* Record test vectors that satisfy the conditions on the first vector and the second vector for each stuck-open.
2) *Step 2:* Select test vector pairs such that all the detectable stuck-open faults are detected.
3) *Step 3:* Generate a test sequence using the selected test vector pairs.

Enhanced scan flip-flops were assumed in the sequential circuits. First we give the data
on fault efficiency with application of original stuck-at test vectors in the order they appear in the test set.

The proposed method achieves higher fault efficiency with small number of test vectors.

From the survey, generate test sequences mistreatment stuck-at test vectors, and supply test sequences that covers high stuck-open fault coverage whereas maintaining the first stuck-at fault coverage.

Two totally different test mechanisms, combinatory circuit or increased scan technique and launch on capture method were thought of. Experimental results showed that the projected ways achieved one thousandth stuck-open fault potency or each circuit. Further more, the generated test sequences achieved higher results than N detection test set.

The technique is predicted to be supported many fault models that capture the behaviours of different types of defects. it's conjointly expected that one among the fault models, that matches the defect behaviour most closely, will be elect to perform the diagnosis. If none of the fault models used by the planned technique captures the defect behaviour accurately enough, the diagnosis might fail. the identical applies to other diagnosis processes once the defect behaviour cannot be explained by the models used for diagnosis.

III.DEFECT COVERAGE

In this survey, the author proposes [4] two operations to generate patterns for different fault pairs and identify equivalent-fault pairs, where a fault pair contains a stuck-at fault and a bridging fault:

O1: Generate a pattern to detect one fault while inactivating the other, where inactivating a fault means that the fault effect of the fault does not appear at the fault site.

O2: Generate a pattern that creates different fault effects for the two faults at some primary or pseudo-primary output, or determine that the two faults are equivalent.

It is clear that O1 can cover all possible ways to distinguish two faults when one of them is inactivated, while O2 can cover all possible ways to distinguish two faults. In general, O2 alone provides complete solution, instead the efficient method to differentiate fault pairs is O1.

The author suggests, the FIM is developed to facilitate O1, which can process all fault pairs at a time and generate a very compact set of diagnosis patterns in a short time, while the FTTM is developed to facilitate O2, which can distinguish all the remaining distinguishable fault pairs and identify equivalent fault pairs given enough CPU time. Thus the proposed procedure is a complete diagnosis pattern generation procedure.

Here, an efficient diagnosis-aware ATPG procedure to identify equivalent-fault pairs and generate diagnosis patterns targeting fault pairs consisting of stuck-at faults and bridging faults. Two major techniques are presented, namely the fault-inactivation method and the fault-types-transformation method. These two methods together can generate very compact patterns in a short time while achieving very high diagnosis resolution.

Experimental results on a large number of fault pairs in both ISCAS'89 and IWLS'05 circuits show that 100% diagnosis resolution can be achieved with only 0.64X extra diagnosis patterns of the original, already very compact test patterns. On average one pattern can distinguish 10.89 pairs. The average run time for one fault pair is no more than 0.18 seconds for all circuits.

IV.CONCLUSION

This survey had presented the study of various stuck-at faults. Test time analysis for the benchmark circuits are discussed. also presented the various techniques for test pattern generation for the fault models and too observe the efficiency in testing.

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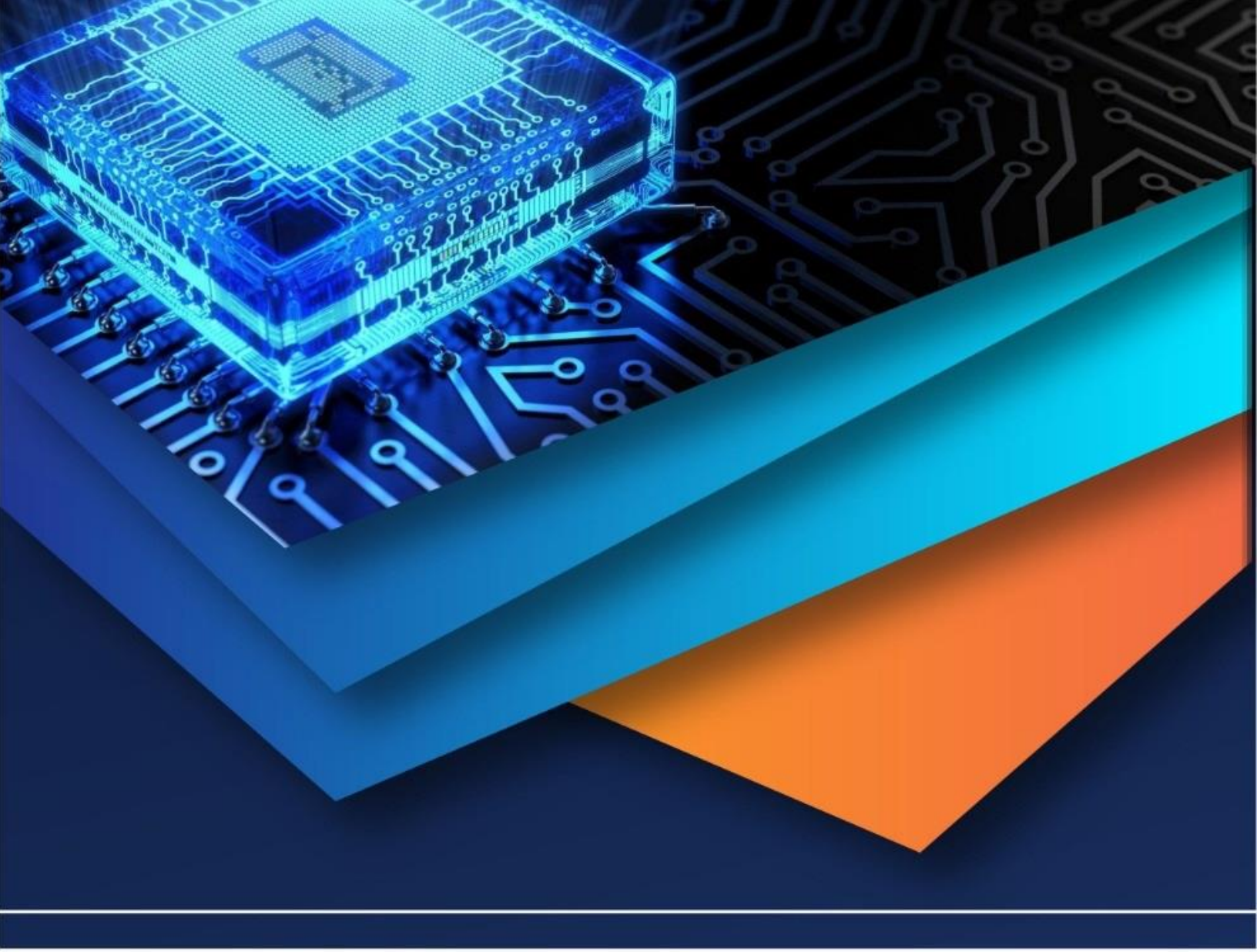

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