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High Speed Low Power Self Timed CAM Application Based On Reordered Overlapped Search Method

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***Abstract*—This paper introduces a reordered overlapped search mechanism for high-throughput low-energy content-addressable memories (CAMs). Most mismatches can be found by searching a few bits of a search word. To lower power dissipation, a word circuit is often divided into two sections that are sequentially searched or even pipelined. Because of this process, most of match lines in the second section are unused. Since searching the last few bits is very fast compared to searching the rest of the bits, we propose to increase throughput by asynchronously initiating second-stage searches on the unused match lines as soon as a first-stage search is complete. This allows the circuits to be in the required phase for their own local operation: evaluate or precharge, instead of having to synchronize their phase to the rest of the word circuits, which greatly reduces the cycle time. The proposed asynchronous CAM operates faster than a synchronous CAM with smaller energy dissipation. An internet protocol (IP) filter is used to unblock particular applications which determine the next hop for a packet by finding the longest prefix match. This lookup often occurs in content addressable memory (CAM), which allows bit masking of the IP address.**

***Index Terms*—CAM, Asynchronous circuits, associative memory, NAND-type CAM, IP filter**

I. INTRODUCTION

Content-addressable memory (CAM) is a special type of computer memory used in certain very-high-speed searching applications. It compares input search data against a table of stored data, and returns the address of matching data. CAMs are used for many applications, such as Data Compression, Network Switch, IP Filters, IP Address Resolution, ATM Switch, Cache Tags, Cache for Large External CAM, Cache Reference Design CAMs often contain a few hundred to 32 K entries for net-work routers, where each entry or word circuit contains several dozens of CAM cells. Each input-search bit is compared with its CAM-cell bit and the comparison result determines whether a pass transistor in the CAM cell attached to the match line (ML) of a word circuit is in on or off states

CAM cells are used with NAND type cells in the existing system. A NAND-type word circuit operates at medium speed because pass transistors are connected seri-ally between a ML to a ground line. Because very few matched word circuits discharge their ML capacitances, a NAND-type word circuit reduces the power dissipation of MLs type word circuit. To improve the throughput of the NAND-type word circuit, some techniques at the circuit level [11], [12].

In this paper, we introduce a reordered overlapped search mechanism for a high-throughput low energy CAM version of this mechanism in [17] and this work is the extension. It includes two new approaches: a reordered word-overlapped search (RWOS) at the scheduling level and phase-overlapped processing (POP) at the circuit level. In a CAM, most mismatches can be found by searching a few bits of a search word. In the proposed CAM, An IP filter is a security feature that prohibits unauthorized users from accessing LAN resources. It can also restrict IP traffic over a wide-area network (WAN) link. With an IP filter, LAN users can be restricted to specific applications on the Internet (such as e-mail). CAM works as a filter to block all access except for packets that have permission. The addresses that have permission are stored in CAM; when an address is sent to memory, CAM reports whether it contains the address. If the address resides within CAM, it has permission for a particular activity. When multiple permissions are required, a combination of CAM and RAM enables this operation. A sample application that regulates access to e-mail, the web, file transfer protocol (FTP), and telnet. This application uses a 4-bit RAM block; each bit of RAM refers to one permission or access.

In the proposed RWOS scheme, an input word is assigned to word circuits at a rate based on the short delay of the first segment instead of the long delay of the whole word circuit. As long as consecutive input words match in unused different word circuits, the proposed CAM properly operates at a rate based on the short delay. A pre-computation block checks the last few bits of consecutive input words. If they are found to be the same, then the next

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search is only initiated once the current search has completed in both segments.

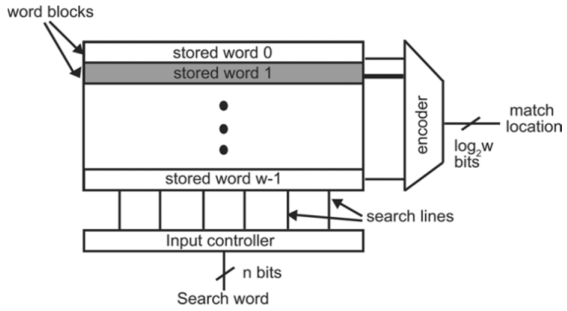


Fig.1 Block diagram of Content Addressable Memory

II. REVIEW OF CONTENT ADDRESSABLE MEMORY

Fig. 1 shows a block diagram of a CAM. A search word is broadcast onto search lines (SLs) to the table of stored words whose sizes are n bits. The number of bits n in a CAM word usually ranges from 36 to 144 bits. A typical CAM employs a table size ranging between a few hundred entries to 32 K entries. Each word block has a match line (ML) that indicates whether search and stored words are the same or different. The outputs of the word blocks are fed to an encoder that generates a binary match location corresponding to the ML that is in the match state.

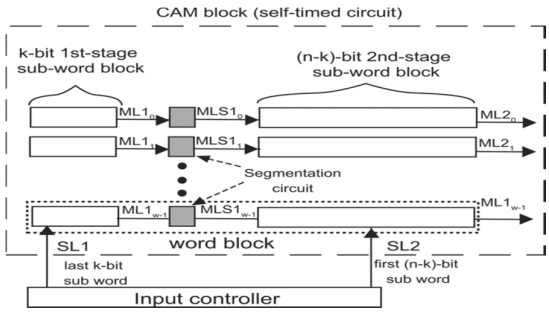


Fig. 2. High-level structure of a CAM

III. OVERLAPPED SEARCH MECHANISM

A. *Word-Overlapped Search*

An overlapped search mechanism that eases the worst-case restriction to improve the throughput of a CAM. It contains two approaches: a word-overlapped search (WOS) and phase-overlapped processing (POP). The overlapped search mechanism can be realized in hardware using synchronous circuits [20] and asynchronous circuits [17].

Fig. 2 shows the high level structure of the CAM based on the WOS scheme. It contains a CAM block that operates using self- timed control and an input controller. There are w word blocks that store -bit words in the CAM block. The word block is divided into a small n -bit sub-word block and its subsequent large (n-k bit) sub word block using a segmentation circuit. This segmentation method is usually used to reduce the switching activity of the subsequent word blocks [21], [22].

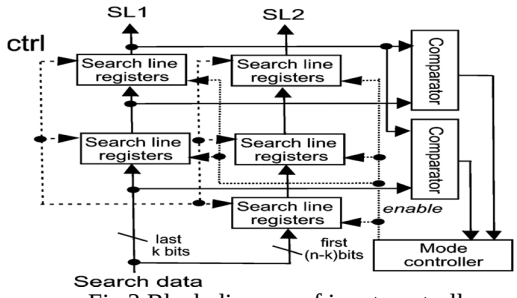


Fig.3 Block diagram of input controller

Once consecutive last k bits of search words are the same, the operation mode changes to slow mode because the current and at

least one of the next search words assign the same word block. Otherwise, the CAM operates at fast mode.

Fig. 3 shows the block diagram of the input controller when m is set to 2. It includes registers, a k bit comparator and a mode controller, which operates in one of two modes: fast and slow. As search words are processed before searching them in a CAM, this method can be categorized as a pre-computation method [19]. A search word is partitioned into the last k bits and the first(n-k) bits of the words. Consecutive last k bits of the current and m search words are compared to check whether they are the same or not. As long as these sub words are not the same, the input controller sends search words to the cam block at high speed.

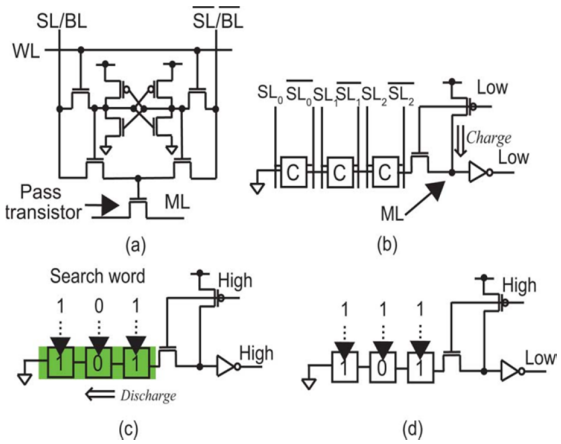


Fig.4. CAM word circuit: (a) a NAND cell, (b) block diagram on precharge phase, (c) block diagram when a search word matches, and (d) mismatches on evaluate phase.

B. Phase-Overlapped Processing

Fig. 4 shows the block diagrams of a typical word circuit based on a NAND-type cell. Fig. 4(a) shows the circuit diagram of a typical NAND-type cell. A word line (WL) is high to write words into the cells, and is low in the search operation. The NAND-type word circuit is implemented using a series of pass transistors in the NAND-type cells. It operates in two phases: precharge and evaluate, based on dynamic logic. In the precharge phase shown in Fig. 4(b), the ML is charged through the PMOS transistor. In the evaluate phase, if a search word is the same as a stored word shown in Fig. 4(c), all pass transistors in the CAM cells are in on states. Hence, the ML capacitance is discharged. This operation is called "match". If a search word is different from a stored word shown in Fig. 4(d), all pass transis-tors in the CAM cells are not in on states. Hence, the voltage of the ML remains high. The operation is called "mismatch." The NAND-type word circuit reduces the power dissipation of MLs compared to the NOR-type one because only a matched circuit discharges the ML capacitance.

IV. REORDERED WORD OVERLAPPED SEARCH

A reordered word-overlapped search (RWOS) scheme to improve the throughput. It is the extension of the WOS scheme.

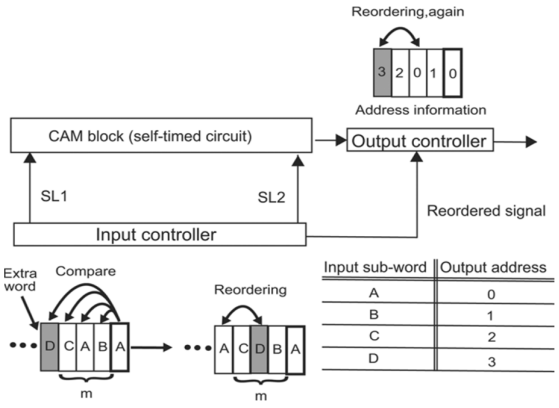


Fig.5 High level structure of proposed CAM

Fig.5 shows the high-level structure of the proposed CAM based on the RWOS and the POP schemes. It contains a CAM block, an input controller, and an output controller. Once input words are reordered in the input controller, the input controller sends a signal, which indicates a reordered input word to the output controller. The output controller reorders the output address based on the signal.

V. ASYNCHRONOUS CIRCUIT

Fig. 6 shows the circuit diagram of the proposed CAM word circuit based on the RWOS and POP schemes. It contains a k-bit 1st-stage sub-word circuit, a segmentation circuit, a self- precharge circuit and a (n-k) bit 2nd-stage sub-word circuit. The 1st-stage sub-word circuits store the last k bits of stored words and the 2nd-stage sub-word circuits store the first (n-k) bits of stored words. All CAM cells are implemented using the NAND-type cell. This circuit is implemented using asynchronous circuits [18].

The 1st-stage segment is implemented using a series of NAND type cells, a precharge PMOS transistor, and a weak feedback PMOS transistor shown in Fig. 6(a). The last k bits of a search word sent from the input controller is assigned and compared with the last of the segmentation circuit bits of stored words.The weak feedback PMOS transistor is added to the ML to solve a charge sharing problem in the NAND type cell.

The 2nd-stage segment contains the local match circuits. The local match circuit contains an inverter, precharge and weak feedback PMOS transistor, a series of k NAND type cells, and an NMOS transistor whose gate is connected as shown in Fig.6(b). All local match circuits of the word circuit operate.

All output are connected to the global match circuit. The global match circuit has a global match line (GML) that contains a series of NMOS transistors, precharge and weak feedback PMOS transistors, and an inverter shown in Fig. 6(c).

The self precharge circuit shown in Fig. 6(d) also operates. The self precharge circuit is a delay element that precharges a matched word circuit after the completion of the current search in the word circuit. In the proposed circuit, the delay element and a combinational block (sub-word circuit) are designed separately. The delay element is designed using a dummy word circuit of the sub-word circuit and several AND gates. The use of the dummy word circuit reduces the delay difference between the delay element and the sub-word circuits under voltage and temperature variations. In contrast, the previous CAM uses just AND gates as the delay element [17]. The dummy word circuit contains the same stored sub-word as that of the 1st segment of the word circuit.

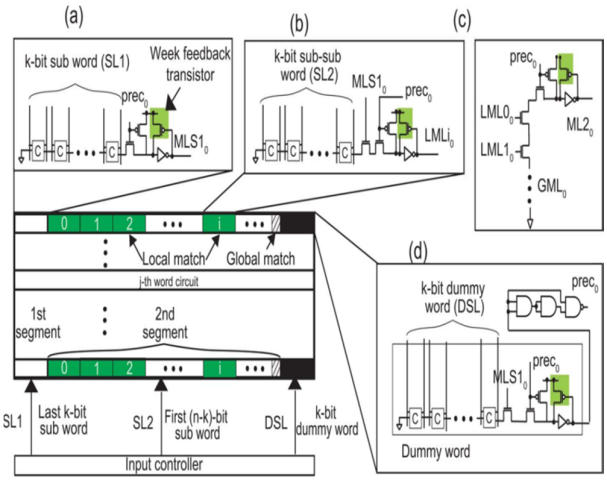


Fig.6.Circuit diagram of the proposed n-bit word circuit

VI. IP FILTER

An IP filter is a security feature that prohibits unauthorized users from accessing LAN resources. It can also restrict IP traffic over a wide-area network (WAN) link.

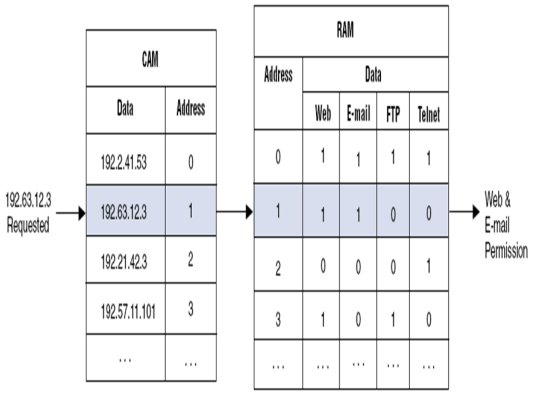


Fig.7 Multiple Permission IP Filter

With an IP filter, LAN users can be restricted to specific applications on the Internet (such as e-mail). CAM works as a filter to block all access except for packets that have permission. The addresses that have permission are stored in CAM; when an address is sent to memory, CAM reports whether it contains the address. If the address resides within CAM, it has permission for a particular activity. When multiple permissions are required, a combination of CAM and RAM enables this operation. A sample application that regulates access to e-mail, the web, file transfer protocol (FTP), and telnet. This application uses a 4-bit RAM block; each bit of RAM refers to one permission

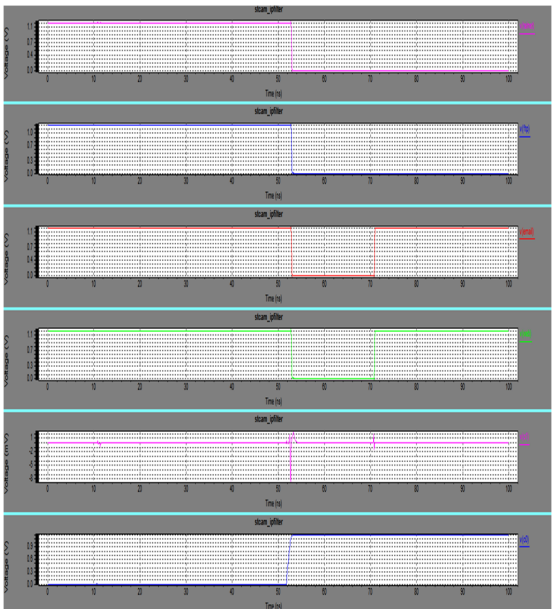
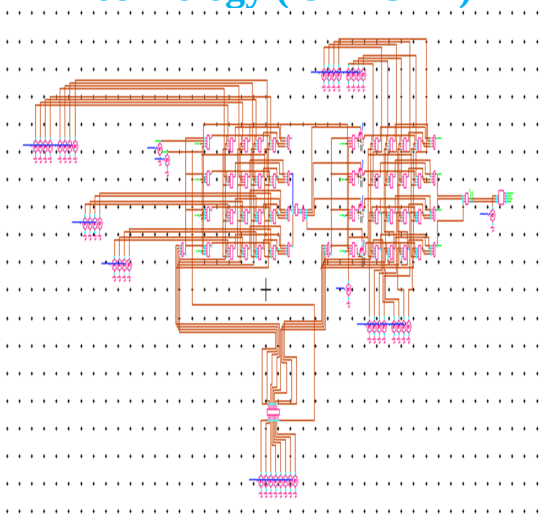


Fig.9 Simulation Waveform

The simulation waveform has been shown in the Fig. 9. This waveform shows the blocked and unblocked IP address. With the help of the IP filter user can request the needed website from the server by using this filter user can unblock the blocked website. For example the user needs the E-mail and the Web the server unblocks the two IP address and permit to access the user.

VII. RESULT AND DISCUSSION

The Schematic View has been shown in the below Fig 8. These methods are realized using Asynchronous circuit, which operates properly. All CAM cells are simulated by using IP filter. This Circuit is simulated by using asynchronous circuits.



Fig, 8 Schematic View

In this paper, we have proposed a high-throughput low-energy content-addressable memory (CAM) based on a reordered overlapped search mechanism. The proposed CAM operates at a rate based on the short delay of the last few-bit search rather than the long delay of whole-word search. These method are realized using Asynchronous circuits. Asynchronous CAM is proposed to increase the speed of IP filter. Proposed method will reduce the power and delay decrease the total number of extra bits. So, proposed method will increase the data accuracy of the memory.

Drawback of the existing system is rectified in this method. IP filter of the proposed system is designed and implemented. The IP filter will be implemented and will be compared with existing system results.

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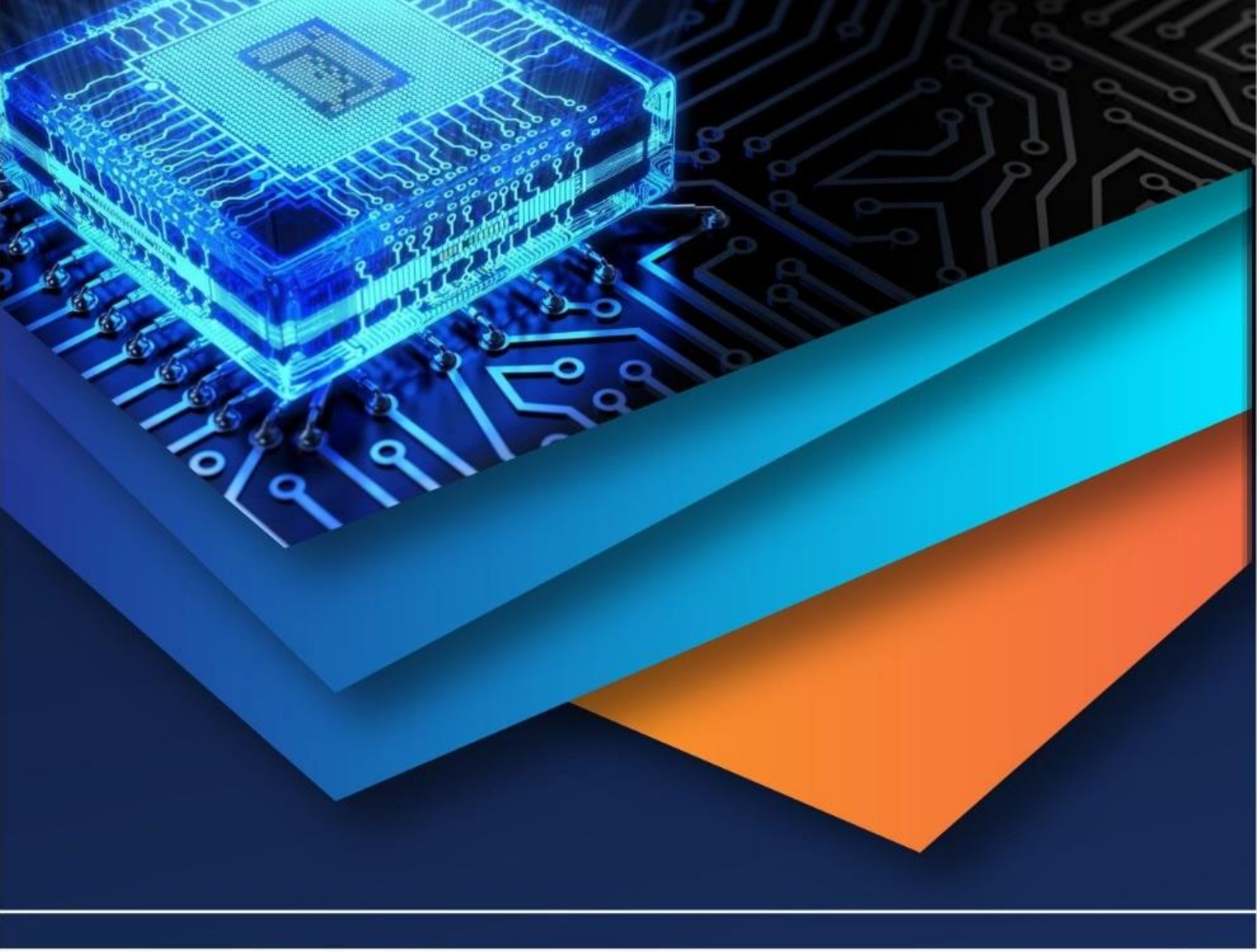
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