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Performance of Cascaded MLI Fed Induction Motor Drive using SPWM technique

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Abstract: ***This paper presents performance of induction motor for five-level and seven-level inverter using cascaded H-bridge topology.***
Mathematical model of asynchronous motor in d-q reference frame and analysis of five and seven level inverter is done. In this paper the THD values of line and phase voltages of five and seven level inverter and the speed and torque characteristics of induction motor using cascaded H bridge inverters is obtained .Sine PWM technique is used to control the performance of induction motor.
The main goal here is to implement the SEVEN level and FIVE level cascade H bridge inverters with less number of switches compared to other topologies. Using this scheme, we can control the speed and reduces the torque ripples of Induction motor. In this paper software implementation is performed by using MATLAB SIMULINK software.
Keywords: THD, Induction Motor, Cascaded H Bridge, Five and Seven level inverter.

I. INTRODUCTION

Pulse width modulation inverters have been gained importance in high performance applications without requiring high ratings on individual devices as static variable compensators, drives and active power filters. Multilevel converters can be applied to utility interface systems and motor drives.

A Multilevel inverter divides the dc rail directly or indirectly, so that the output of the leg can be more than two discrete levels. As both amplitude modulation and pulse width modulation are used in this the quality of the output waveform gets improved with low distortion. The advantages of multilevel inverter are good power quality, low switching losses, reduced output and high voltage capability. Increasing the number of voltage levels in the inverter increases the power rating. The pulse width modulation schemes of multilevel inverters are classified into two types:

A. Multicarrier sub-harmonic pulse width modulation (MC-SHPWM)
B. Multicarrier switching frequency optimal pulse width modulation (MC-SFOPWM)

The MC-SHPWM diode clamped multilevel inverter strategy reduced total harmonic distortion and the MC-SFOPWM technique for multilevel inverter strategy enhances the fundamental output voltage. The Three main topologies of multilevel inverters are :

1) Neutral point clamped or Diode clamped
2) Flying capacitors
3) Cascaded H Bridge

Among these cascaded H bridge multilevel inverter topology is the most attractive as they got a higher level of The aim is to increase the level number of the H bridge inverter such that the harmonic contents can be reduced as much as possible while keeping low switching frequencies and switching loses. Several identical H bridge cells are cascaded in series as per the requirements constitute a cascade H bridge this type of topologies are used for high power applications. Cascaded H Bridge is further classified into two types, they are 1. Symmetrical, 2.Asymmetrical. For symmetrical inverter the input dc voltages are equal in all the cascaded power cells and for asymmetrical inverter the input dc voltages are unequal. Advantages of multilevel inverters are:

a) They are suitable for high-voltage and high current applications.
b) They have higher efficiency since the devices can be switched at a low frequency.
c) Power factor is close to unity for multilevel inverters
d) No Electromagnetic Interference (EMI) problem exist

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II. INDUCTION MOTOR DRIVE

AC asynchronous motor, also called as induction motor has become the most widespread electrical motor in use today. These facts are due to the induction motors advantages over the rest of the motors. The main advantage they do not need any mechanical commutator, leading to the fact that they are maintenance free motors. Induction motors also have low weight and inertia, high efficiency and a high overload capability. Therefore, they are cheaper and more robust, and less proves to any failure at high speeds. Furthermore, the motor can work in explosive environments because no sparks are produced. However, mechanical energy is more than often required at producing an infinitely variable induction motor speed drive is to supply the induction motor with the three phase voltages of variable frequency and variable amplitude. A variable frequency is required because the rotor speed depends on the speed of the rotating magnetic field provided by the stator. A variable voltage is required because the motor impedance reduces at low frequencies and consequently the current has to be limited by means of reducing the supply voltages.

III. MATHEMATICAL MODELING OF INDUCTION MOTOR

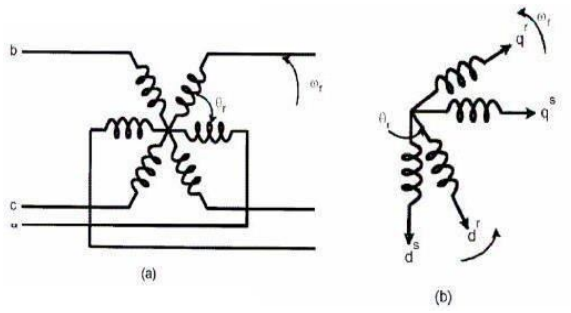


Fig.1.Induction Motor Stator and rotor windings

Three phase induction motor voltage equations in three phases and two phase axis are expressed as:

$$\begin{bmatrix} v_{qs}^{s} \\ v_{ds}^{s} \\ v_{os}^{s} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta-120^{o}) & \cos(\theta+120^{o}) \\ \sin(\theta) & \sin(\theta-120^{o}) & \sin(\theta+120^{o}) \\ 0.5 & 0.5 & 0.5 \end{bmatrix}\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix}$$

$$v_{as} = v_{qs}^{s}$$

$$v_{bs} = \frac{1}{2}v_{qs}^{s} - \frac{\sqrt{3}}{2}v_{ds}^{s}$$

$$v_{cs} = -\frac{1}{2}v_{qs}^{s} + \frac{\sqrt{3}}{2}v_{ds}^{s}$$

The inverse relation for the above is:

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$$v_{qs}^{s} = R_s i_{qs}^{s} + \frac{d}{dt}\Psi_{qs}^{s} \qquad v_{qs}^{s} = R_s i_{qs}^{s} + \frac{d}{dt}\Psi_{qs}^{s}$$

$$v_{ds}^{s} = R_s i_{ds}^{s} + \frac{d}{dt}\Psi_{ds}^{s} \qquad v_{ds}^{s} = R_s i_{ds}^{s} + \frac{d}{dt}\Psi_{ds}^{s}$$

$$v_{qs}^{s} = R_s i_{qs}^{s} + \frac{d}{dt}\Psi_{qs}^{s}$$

$$v_{ds}^{s} = R_s i_{ds}^{s} + \frac{d}{dt}\Psi_{ds}^{s}$$

The two phase ds-qs winding are transformed into the hypothetical winding mounted on de- qe axes. The voltages on ds-qs axes can be transformed into d_e-q_e frame by following equations,

$$v_{qs} = R_s i_{qs} + \frac{d}{dt}\Psi_{qs} + \omega_e \Psi_{ds}$$

For rotor circuit,

$$v_{qr} = R_r i_{qr} + \frac{d\Psi_{qr}}{dt} + (\omega_e - \omega_r)\Psi_{dr}$$

$$v_{dr} = R_r i_{dr} + \frac{d\Psi_{dr}}{dt} - (\omega_e - \omega_r)\Psi_{qr}$$

Three Phase Induction Motor torque balance and developed torque equations are written as:

$$T_e = T_L + J\frac{d}{dt}\omega_m = T_L + \frac{2}{p}J\frac{d\omega_r}{dt}$$

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$$T_e = \frac{3}{2}\left(\frac{P}{2}\right)(\Psi_{dm} i_{qs} - \Psi_{qm} i_{ds})$$

$$T_e = \frac{3}{2}\left(\frac{P}{2}\right)(\Psi_{ds} i_{qs} - \Psi_{qs} i_{ds})$$

$$T_e = \frac{3}{2}\left(\frac{P}{2}\right) L_m (i_{qs} i_{dr} - i_{ds} i_{qr})$$

$$T_e = \frac{3}{2}\left(\frac{P}{2}\right)(\Psi_{dr} i_{qr} - \Psi_{qr} i_{dr})$$

IV. ANALYSIS OF SEVEN LEVEL CASCADED H BRIDGE INVERTER

A cascaded multilevel inverter consists of a series of single-phase full bridge inverter units. Each separate DC source is connected to a full bridge inverter. The cascaded multilevel inverter does not require any voltage clamping diodes or voltage balancing capacitors like other two topologies. The seven-level multilevel inverter is obtained by cascading three full bridge inverter circuits. The three full bridge inverters are connected in series and a single- phase output is taken. Each full bridge is fed from separate DC source. The number of output levels m in each phase is related to number of full bridge inverter unit's n by, m/2n+1. Here the number of levels is seven, hence number of inverter circuits connected in series is three. The single phase seven- level topology of cascaded H bridge multilevel inverter is shown in Fig. 2(a) Each H-bridge is fed with the same value of DC voltage hence it can be called as symmetrical cascaded multilevel inverter. Each full bridge inverter can generate three different voltage outputs: +Vdc, 0, and -Vdc. The output voltage is synthesized by sum of three inverter outputs are at three angles. These three angles are used for giving pulses to twelve switches. The switching pattern for single phase seven-level topology of cascaded H-bridge multilevel inverter is shown in Table.

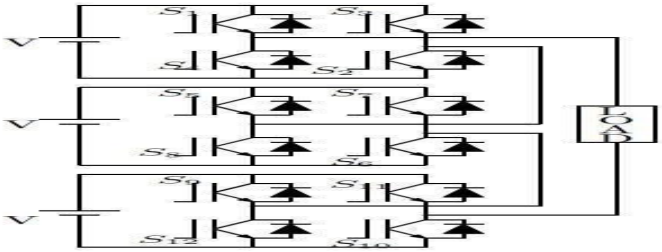


Fig-2(a) Cascade inverter circuit topology

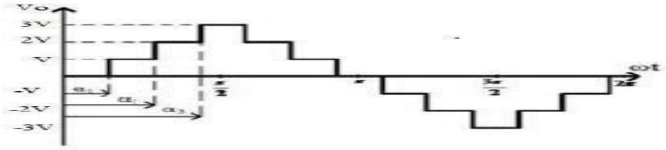


Fig. 2 (b) Seven-level output waveform

Table 1.Switching States for a seven level cascaded H Bridge inverter

V_0	+V	+2V	+3V	0	-V	-2V	-3V
S_1	1	1	1	0	0	0	0
S_2	1	1	1	1	0	0	0
S_3	0	0	0	0	1	1	1
S_4	0	0	0	1	1	1	1
S_5	0	1	1	0	0	0	0
S_6	1	1	1	1	1	0	0
S_7	0	0	0	0	0	1	1
S_8	1	0	0	1	1	1	1
S_9	0	0	1	0	0	0	0
S_{10}	1	1	1	1	1	1	0
S_{11}	0	0	0	0	0	0	1
S_{12}	1	1	0	1	1	0	1

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A. Advantages

1) The number of possible output voltage levels is more than twice the number of DC sources (m = 2s + 1).

2) The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

3) Possibility to implement soft-switching.

B. Disadvantages

1) Separate DC sources are required for each of the H bridges. This will limit its application to products that already have multiple SDCSs readily available.

2) No common DC-bus.

V. ANALYSIS OF FIVE LEVEL CASCADED H BRIDGE MULTILEVEL INVERTER

Conventional cascaded multilevel inverters are one of the most important topologies in the family of multilevel and multi-pulse inverters. The cascade topology allows the use of several levels of DC voltages to synthesize a desired AC voltage. The DC levels are considered to be identical since all of them are fuel cells or photovoltaic, batteries, etc. [20]. It requires least number of components compared to diode-clamped and flying capacitors type multilevel inverters and no specially designed transformer is needed as compared to multi pulse inverter. Since this topology consist of series power conversion cells, the voltage and power level may be easily scaled. The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are 2n+1, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. An n level cascaded H bridge multilevel inverter needs 2(n-1) switching devices where n is the number of the output voltage level**.**

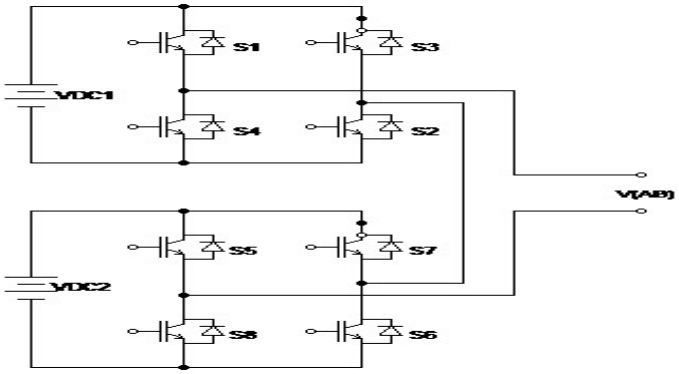


Fig3: Five Level Cascaded H Bridge

Cascade topology proposed in uses multiple dc levels, which instead of being identical in value are multiples of each other. It also uses a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical, modular units for each level.

Table 2.Switching States for a Five-level cascaded H Bridge inverter

Switches Turn On	Voltage Level
S1, S2	+Vdc
S1,S2,S5, S6	+2Vdc
S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

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VI. SIMULATION RESULTS

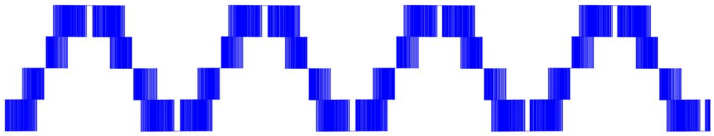


Fig.4:Line voltage of five level inverter

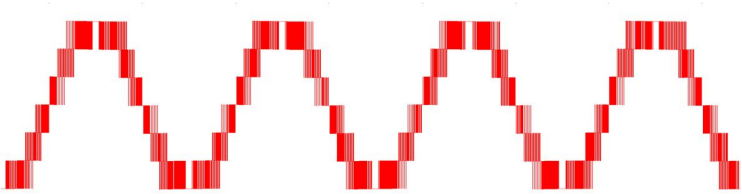


Fig.5:Line voltage of seven level inverter

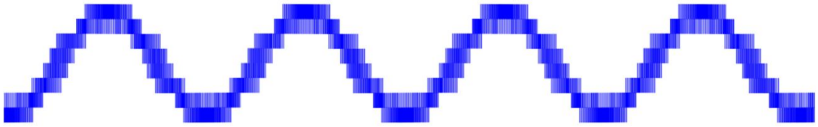


Fig.6:phase voltage of five level inverter

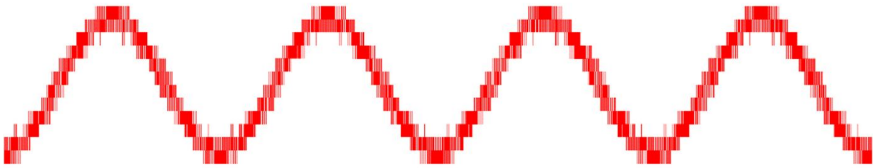


Fig.7:phase voltage of seven level inverter

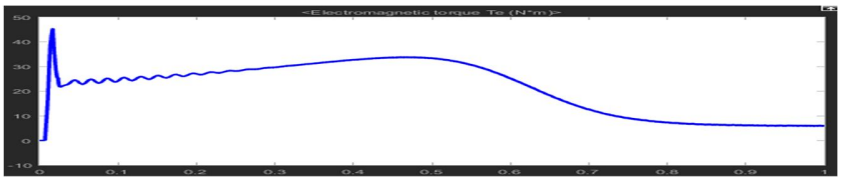


Fig.8. Response of torque of induction motor using five level inverter

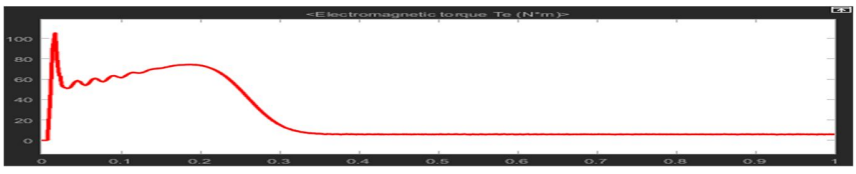


Fig.9: Response of torque of induction motor using seven level inverter

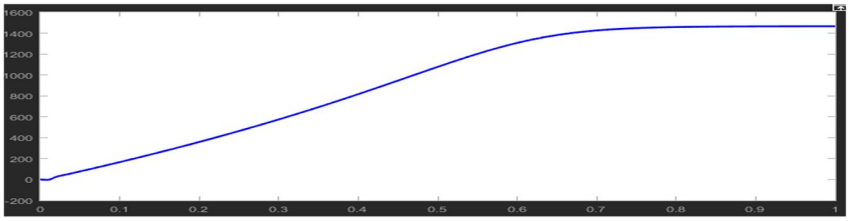


Fig.10: speed of motor using five level inverter

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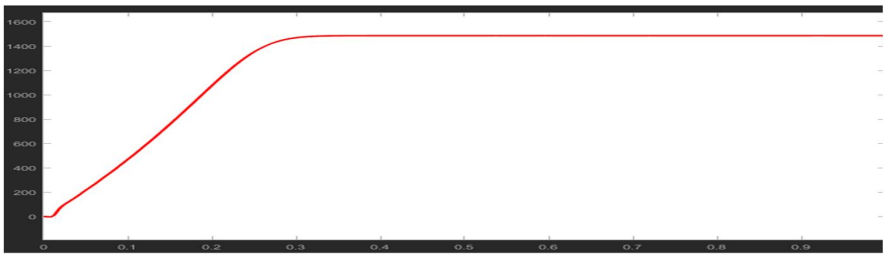


Fig11: speed of motor using seven level inverter

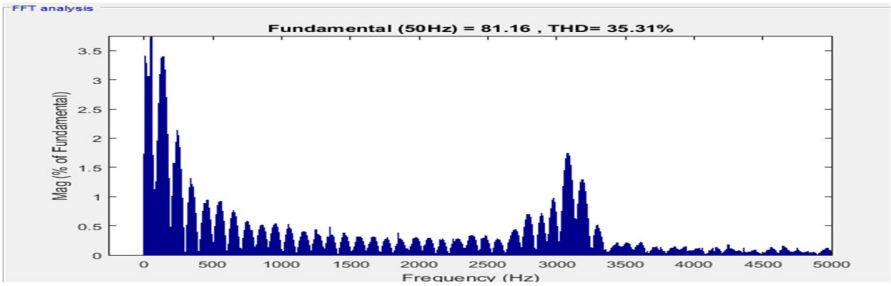


Fig 12: THD of line voltage using five-level inverter

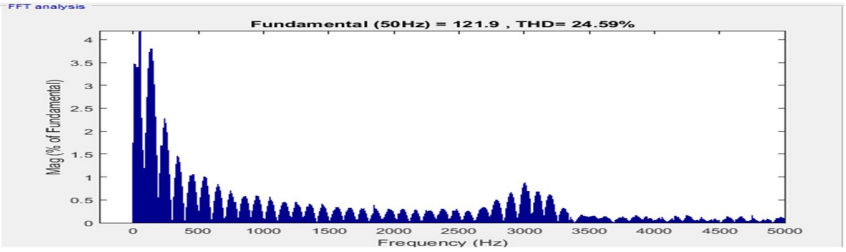


Fig13: THD of line voltage using seven-level inverter

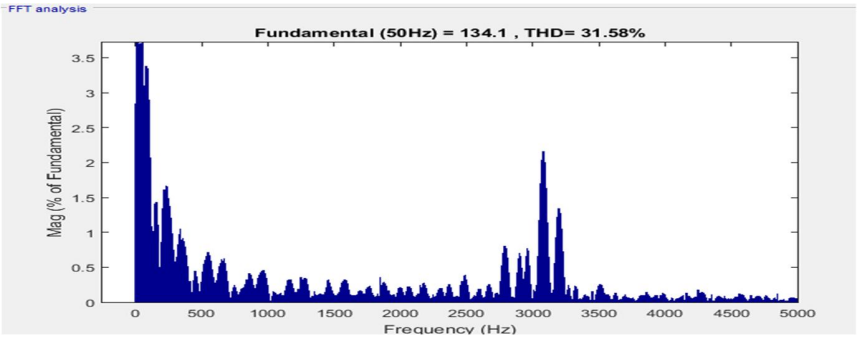


Fig14: THD of phase voltage using five-level inverter

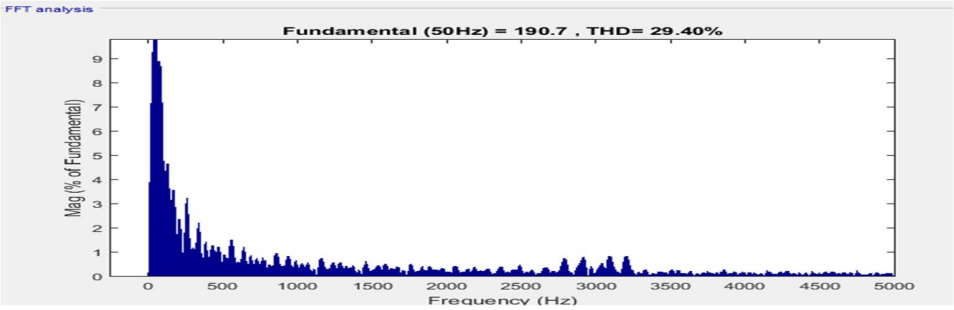


Fig.15: THD of phase voltage using seven-level inverter

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VII. CONCLUSION

In this paper, Sinusoidal PWM inverter fed induction motor has been analyzed and simulated using MATLAB/SIMULINK. This paper has provided a brief summary and comparison of Five-level and Seven-level multilevel inverter Cascaded H Bridge inverter circuit topologies. The THD using FFT analysis was compared in this paper. Simulation results of Five-level and Seven-level inverter fed three phase Induction motor topologies are discussed. Also this paper concludes that when the number of levels increasing, harmonics are reduced for same technique. This paper shows the steady state response of speed and electromagnetic torque of three phase induction motor using Sinusoidal PWM technique.

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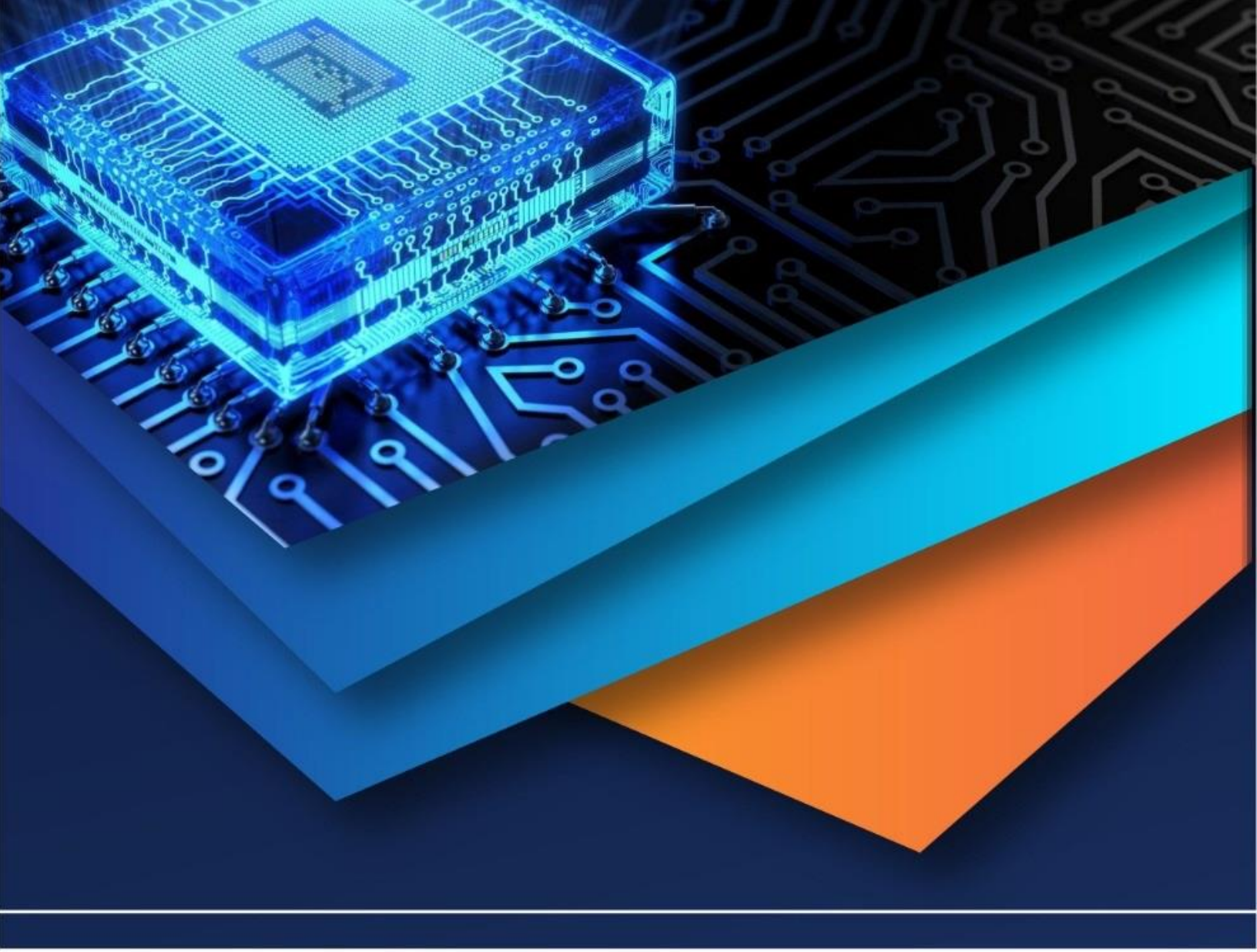
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