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Leakage Reduction in 180nm CMOS Full Adder using Modified Lector Technique

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***Abstract:** In designing of digital signal processors, image processing, microprocessors full adder is the main requirement in VLSI design. Today, full adder design with better performance, high speed, less area with less delay is one of the main challenges for VLSI engineers. This project proposes 1-bit full adder using a stacking effect. This proposed full adder will be simulated using 180nm CMOS process technology at 1.8V supply voltage using Tanner EDA. The results of the proposed full adder will be compared with results of the conventional full adder. The comparisons will show that the proposed adder circuit is efficient in terms of static power dissipation as a conventional adder circuit.*

I. INTRODUCTION

The well-engineered deep submicron CMOS technologies are explored to address the challenging criteria of these emerging high-speed and low-power communication digital signal processing chips. In very-large-scale integration (VLSI) systems, there are most frequently and widely used circuits namely fast arithmetic computation cells including adders and multipliers. The most efficient implementation of simple gates (e.g. NAND/NOR) which have only a few transistors and nodes and a small delay due to a single inversion level is allowed by conventional CMOS. The large PMOS transistors have some disadvantages that result in high input capacitances and area requirements, and the weak output driving capability caused by series transistors. The conventional CMOS full adder is designed in Tanner S-edit and the circuit is simulated. When compared to the hybrid adder, the power consumed by the conventional CMOS adder is high because the transistors count is high which may lead to large dynamic power dissipation, due to this the circuit will draw more power. The parallel combination of p-mos and n-mos are used in Multiplexer based adder. For designing a 4:1 multiplexer full adder 16 transistors are required. Similar to conventional CMOS adder the hybrid adders and the proposed hybrid adders is designed in tanner s-edit and the circuit is simulated. The power consumed by hybrid adders is less than conventional CMOS adder but higher than a proposed hybrid adder, and the power consumed by each adder circuit is tabulated.

The paper is organized as follows: Section 2 explains the physics of operation of modified lector technology and shows logic gate design using that. Section 3 provides an explanation of Adder design using the same methodology in 3 different cases. Section 4 shows the result and analysis. Finally, Section 5 gives a conclusion.

II. MODIFIED LECTOR TECHNOLOGY

A parallel combination of two low Vth transistors (NMOS) in series and one capacitor is connected between the bottom of pull-down network and the ground terminal of conventional CMOS NAND and NOR gate as shown in fig. 1.

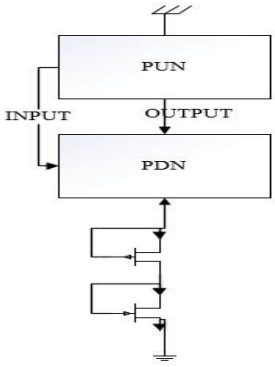


Fig.1: Block diagram of modified lector technique

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This arrangement is considered as the proposed circuit/section, used later of this article. Gate terminal of the NMOS is connected to the drain terminal and thus the ON-OFF condition of this NMOS is self-generated. For reducing leakage power, generally high Vth MOSs has been used. But in this technique instead of high Vth NMOS, we are working with low Vth NMOS. Obviously, a circuit with high Vth NMOS consumes less leakage power than the circuit with low Vth NMOS. But in that case, the low level of the output waveform is much greater than the VSS level which is not desirable. However, as in this extra arrangement, gate and drain terminal is tied to each other and thus low Vth NMOS satisfies our requirement. The series connection of two transistors enhances the stacking effect. It is expected that leakage will be lesser if two transistors are connected in series.

III. ADDER CIRCUIT

Now let us extend the concept to verify the combinational circuit operation. We have chosen to design a 1-bit full adder using the proposed section. Before that, we have studied the conventional adder structure and have divided it into four blocks. The Conventional adder structure is shown in figure 6.

From figure 6 it is clear to have four different parts of the adder circuit which is shown in figure 7 as a block diagram.

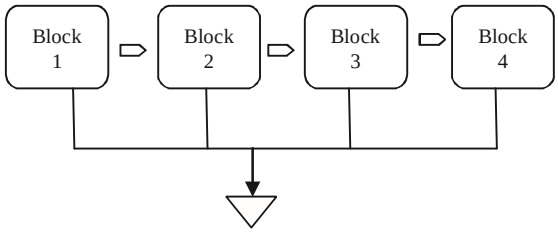


Fig.2: Block diagram of Conventional Adder

Now, one or several blocks are to be grouped and proposed section (external block) is to be added. When less number of external blocks is used, the delay will be increased as large amount switching will be there and hence less power is consumed. On

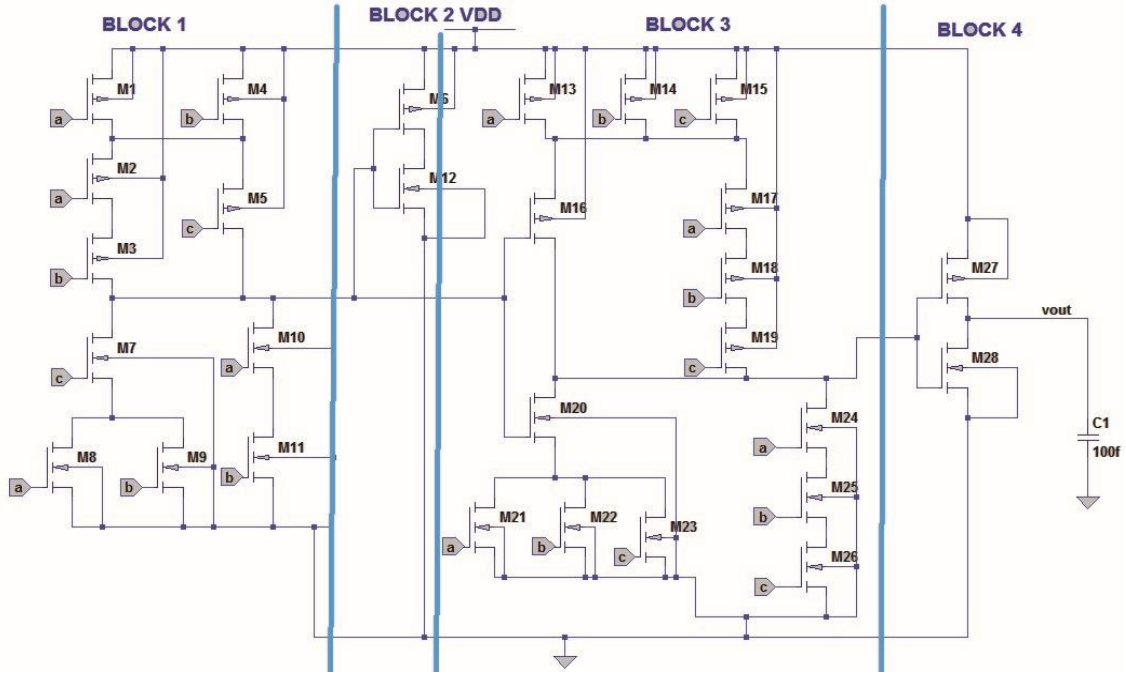


Fig.3: Conventional 28T Adder the other hand, when a large number of external blocks is added, delay time decreases and power consumption increases.

We have proposed three different configurations proposed section separately as shown in figure 10. (Case-1, Case-2, and Case-3) and they are discussed here.

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1) *Case-1Approach:* In this case, all the blocks of the adder are connected to ground through a single proposed section as shown in the figure.

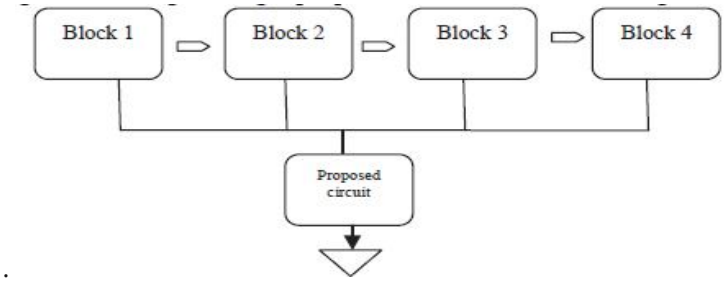


Fig 4: Block Diagram of Case-1 Approach

2) *Case-2 Approach:* In this case, Block 1 & Block 2 are clubbed together to connect towards the ground through the proposed section.

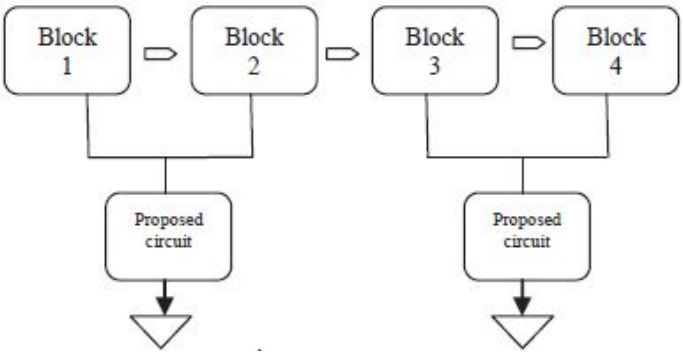


Fig 5: Block diagram of Case-2 Approach

In the same way, Block 3 & Block 4 is clubbed and proceeds towards the ground through another proposed section as shown in the figure.

3) *Case-3 Approach:* In this case, each block is connected to ground through a proposed section separately as shown in figure

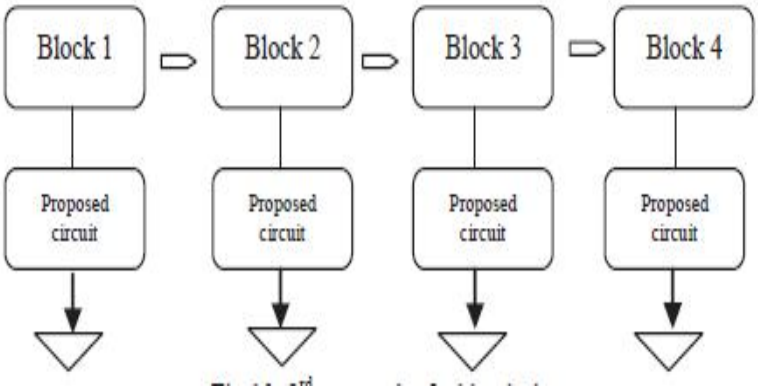


Fig 6: Block diagram of Case-3 Approach

In this work, we have proposed a new methodology for logic gates to provide lesser delay and power savings. This design methodology is used for the operation of 1-bit full Adder. After dividing the conventional adder into 4 segments we have proposed 3 different methodologies of adder design. We have shown that all 3 proposed cases are better than the conventional circuit in terms of power and delay.

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IV. RESULTS AND ANALYSIS

All the three cases mentioned in the last section has been designed in TANNER EDA and all the schematic's of Different approaches for the Adder is shown below along with their output waveforms.

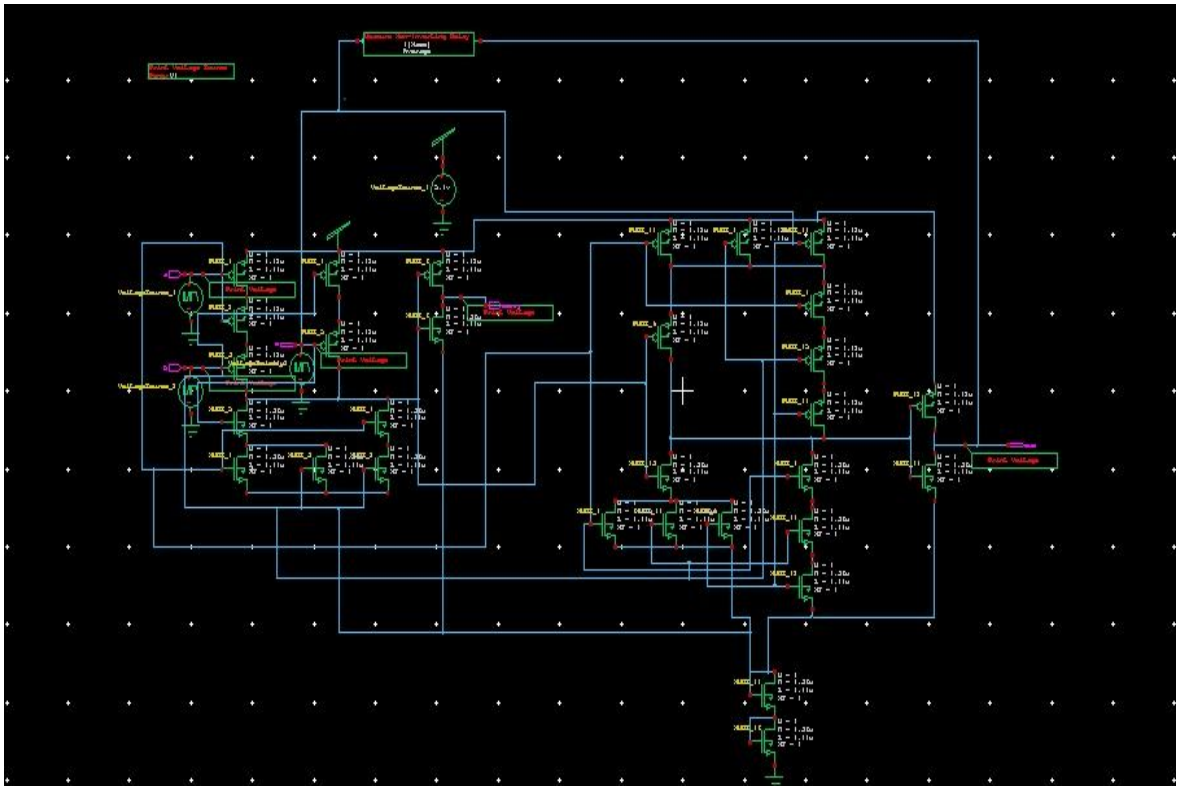


Fig7: schematic of case-1 approach

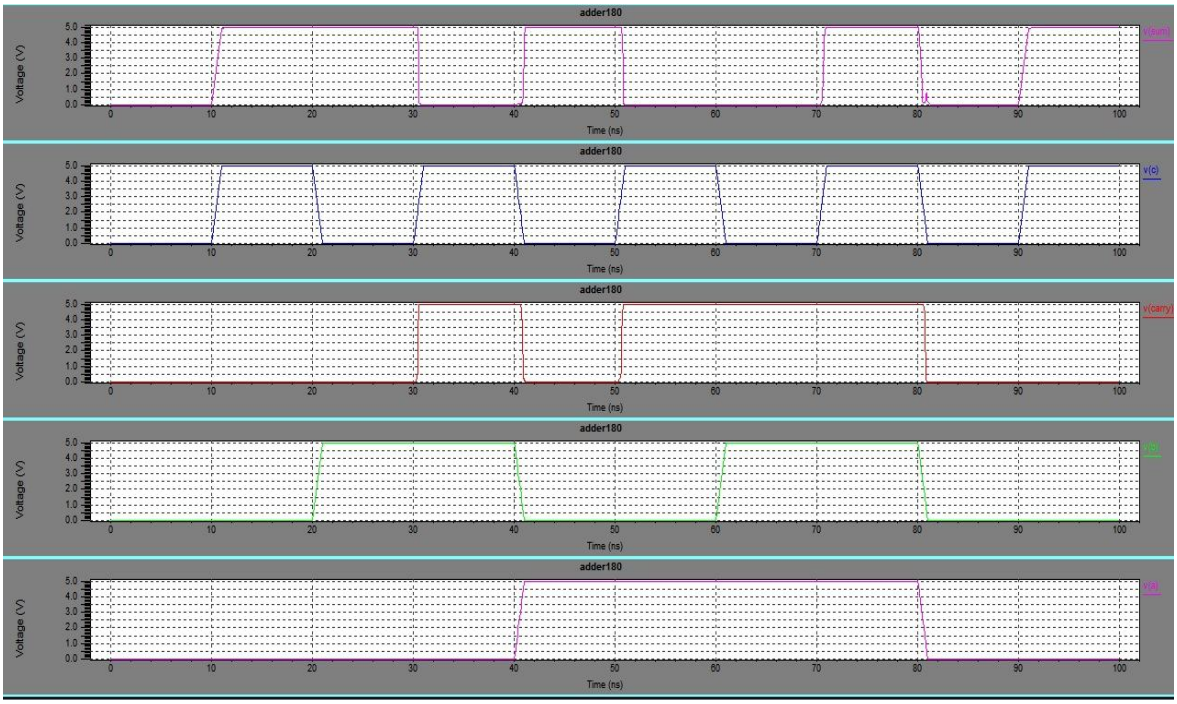


Fig8: Output waveform of case-1 approach

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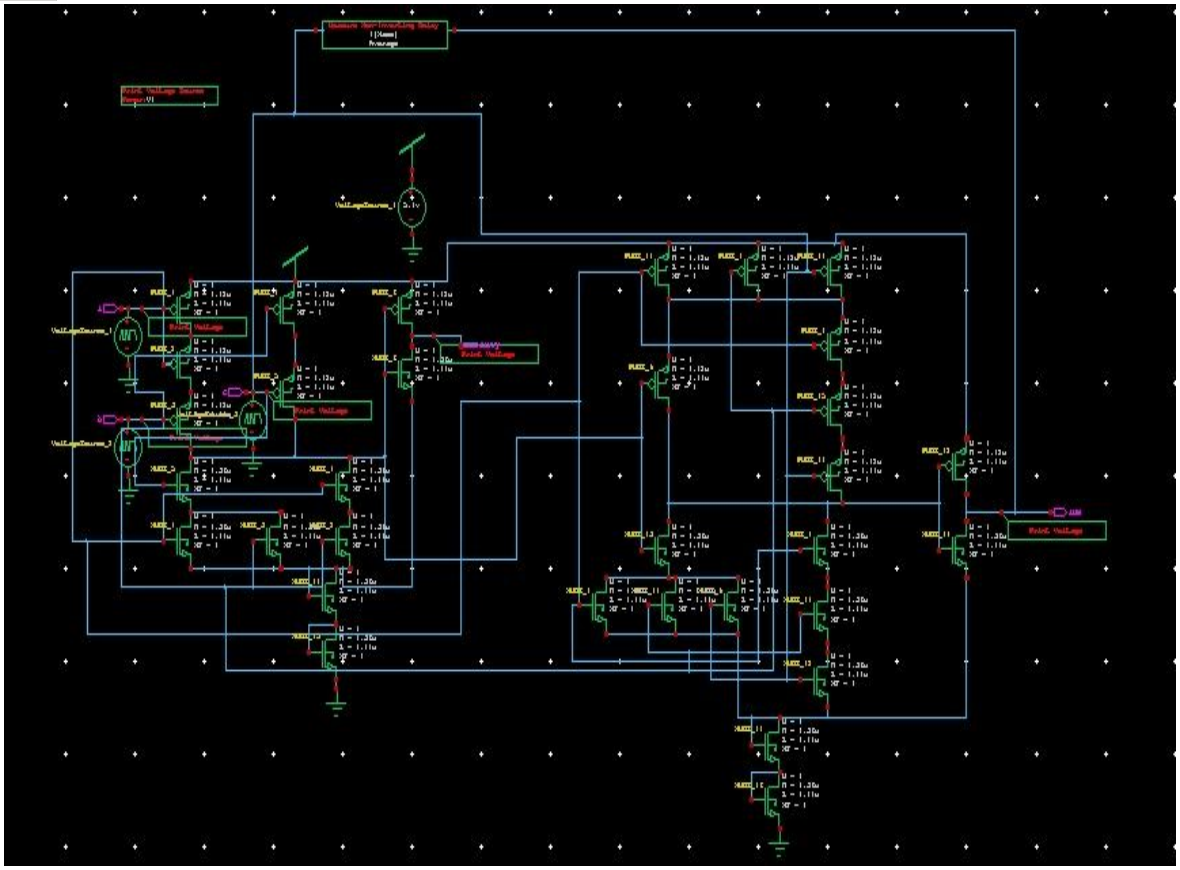


Fig9: schematic of case-2 approach

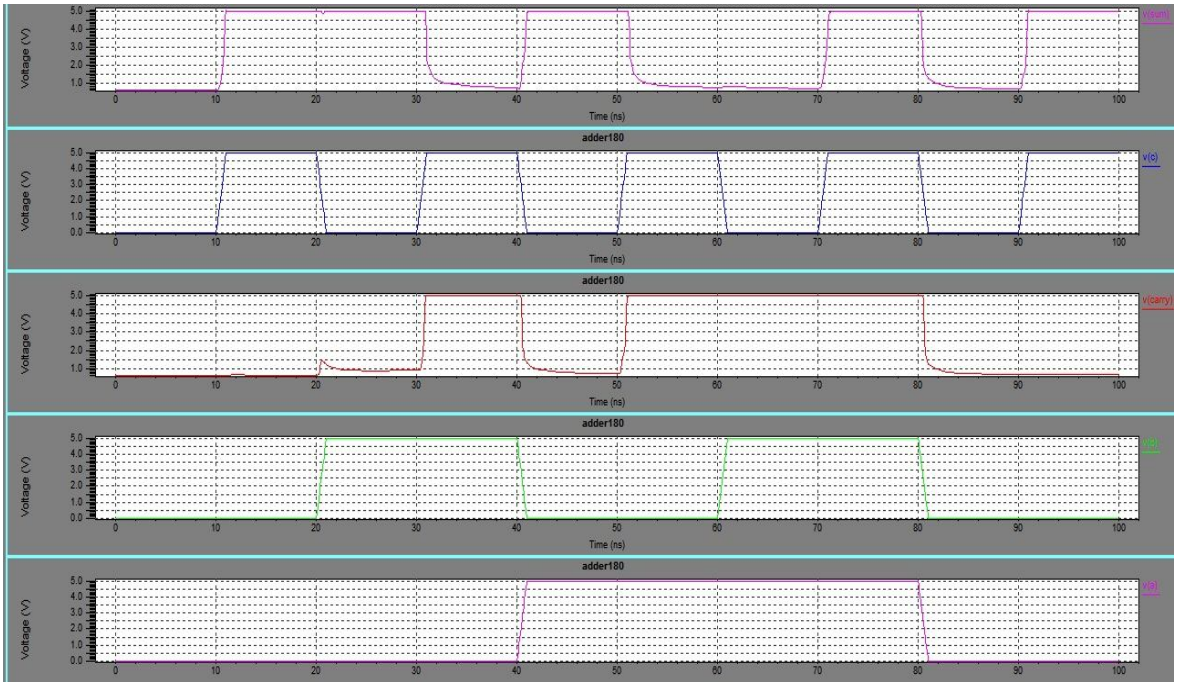


Fig10: output waveform of the case-2 approach

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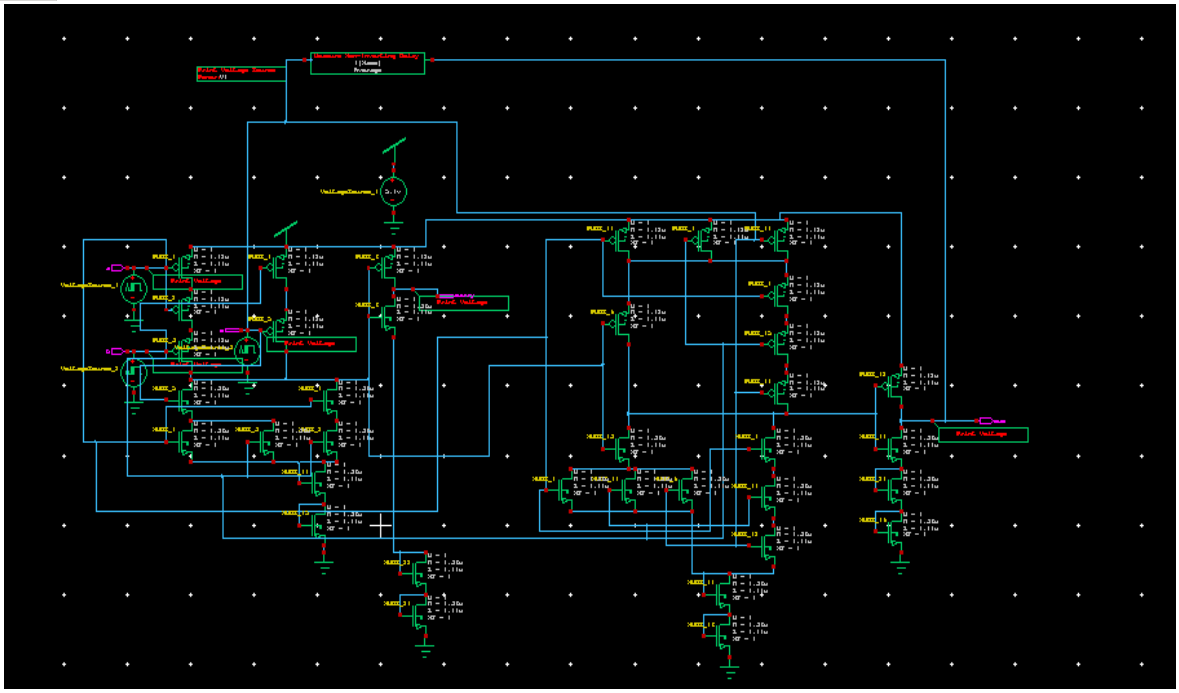


Fig11: schematic of case-3 approach

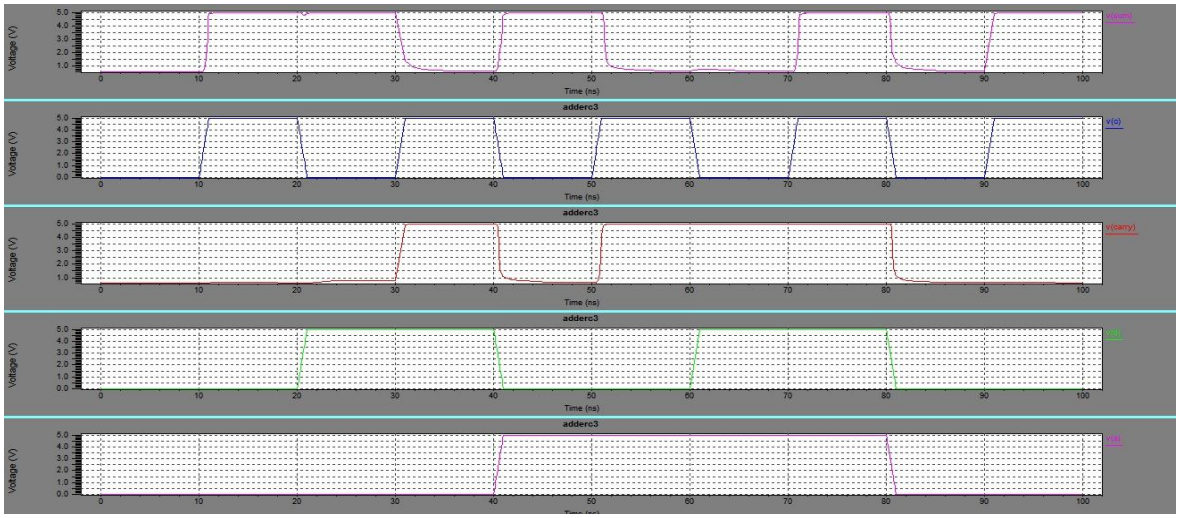


Fig12: output waveforms of case-3 approach

The leakage power analysis of the adder circuits is shown in Table 1.

Measured Unit	Basic Full Adder	Case-1 (Single Lector)	Case-2 (Double Lector)	Case-3 (Four Lector)
Delay	10 ns	10 ns	5.7 ns	5.6 ns
Power	12.34uW	1.5 uW	2.4 uW	2.7 uW
Power Delay Product	123.4fW (femto)	15 fW	13.68 fW	15.12 fW

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Table 1 : leakage power analysis

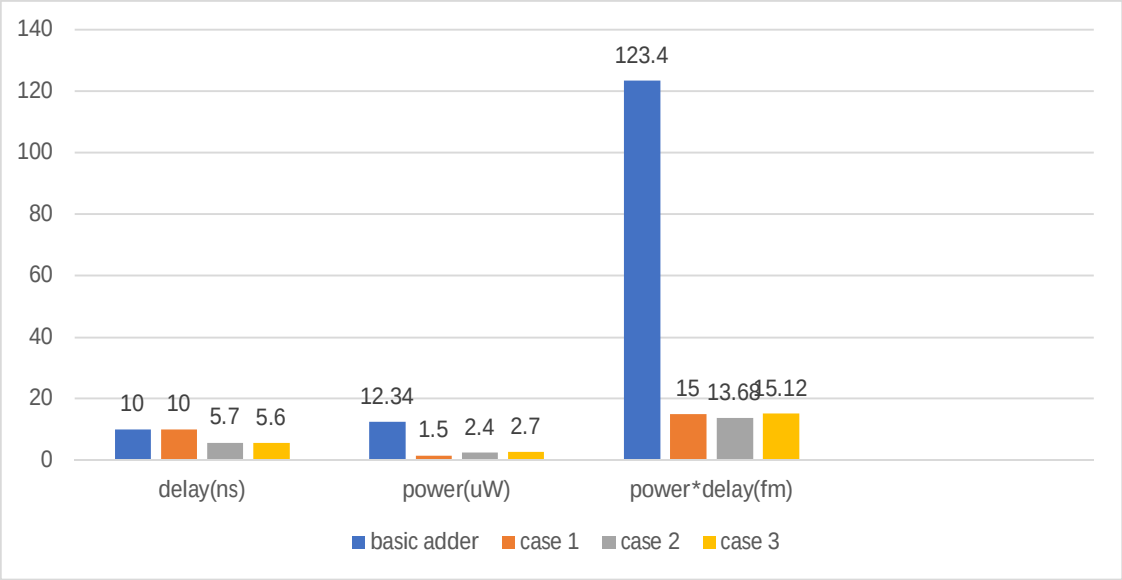


Fig13: Illustrating the comparisons using a bar graph

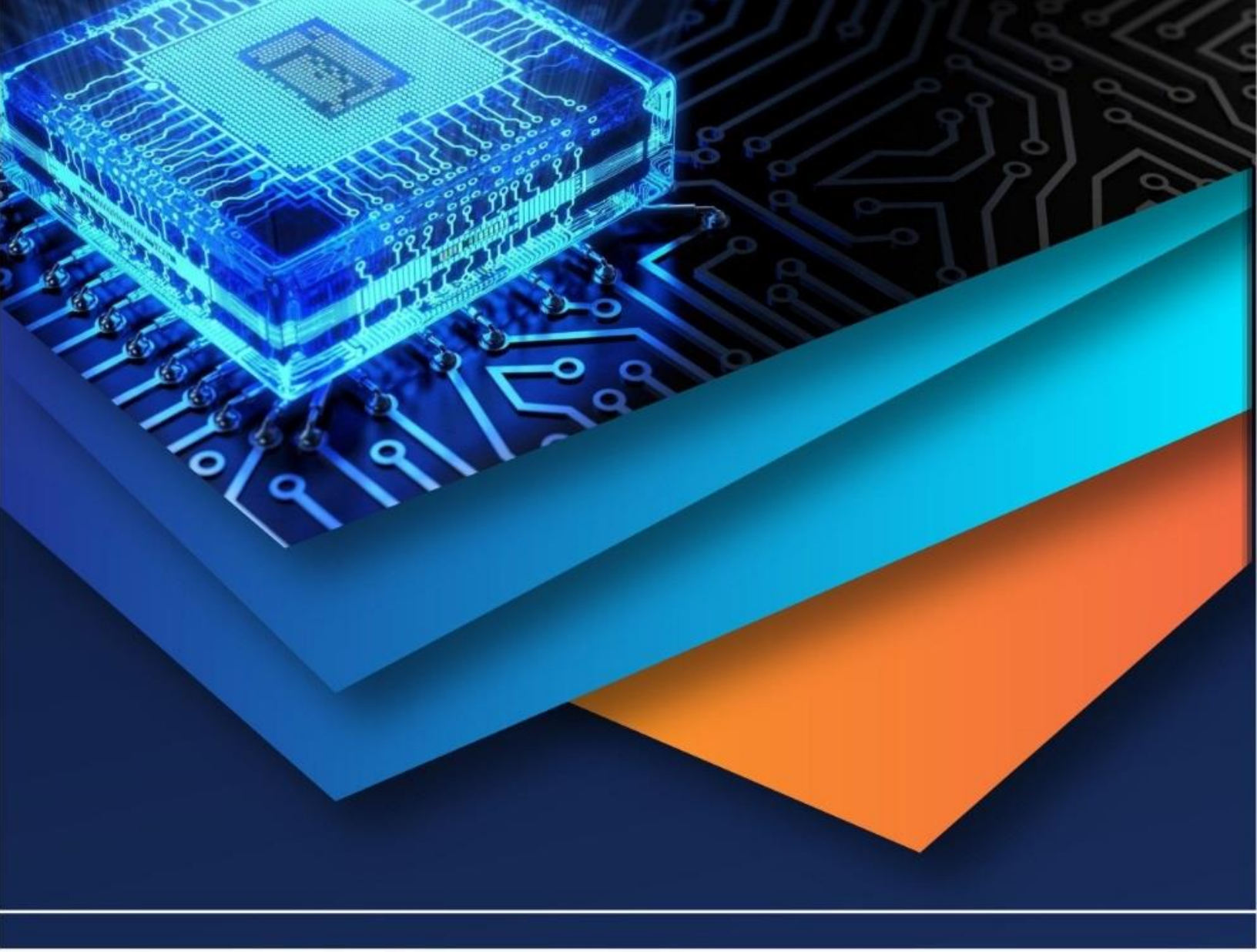
V. CONCLUSION

Leakage power dissipation has increased due to scaling down the device size and threshold voltage. To reduce the standby leakage current a new modified lector technique is proposed for full adder circuit. This proposed circuit increases the resistance of conducting path from the pull-down network to ground terminal during stand by condition. The proposed section is applied to full adder and analyzed in three different cases. We observed that all three proposed full adder performs better than the conventional full adder by reducing the leakage power. It is be noticed that if we are looking only for a full adder having less power consumption then design based of proposed case-1 approach is preferable, whereas only if delay is considered in the design of full adder then case-3 approach is preferable and if we consider both delay and power consumption in the design of full adder then case-2 is preferable.

REFERENCES

[1] Third International Conference on Devices, Circuits and Systems (ICDCS'16)978-15090-2309-7/16/$31.00©2016 IEEE
[2] International Journal of Emerging Technology and Advanced Engineering Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 5, Issue 11, November 2015)
[3] Guide to the Tanner EDA v12.6 Design Tools for use in designing, simulating, and laying out ICs. Department of Electrical and Computer Engineering.
[4] International Journal of Engineering Research & Technology (IJERT)Vol. 2 Issue 12, December – 2013IJERTIJERTISSN: 2278-0181.
[5] International Journal of Engineering Science and Technology Vol. 2(5), 2010, 1250-1252 on Implementation and Analysis of SC-LECTOR CMOS Circuit.
[6] M. Morris Mano, "Digital circuit design", 3rd Edition, Pearson Education, 2006.
[7] N. Hanchate and N.Ranganathan, "LECTOR: A Technique for Leakage Reduction in CMOS Circuits", IEEE Transactions on VLSI Systems, vol. 12, pp. 196-205, Feb., 2004.
[8] CHANDRAKASAN, A. P., SHENG, S., and BRODERSEN, R. W,"Low- Power CMOS Digital Design," IEEE Journal of Solid-StateCircuits, vol. 27, no. 4, pp. 473-484, April 1992.

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