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Design & Implementation Of On Chip Permutation Network for MPSOC on FPGA

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Abstract: This paper presents the silicon-proven design of a novel on-chip network to support guaranteed traffic permutation in multiprocessor system-on-chip applications. The proposed network employs a pipelined circuit-switching approach combined with a dynamic path-setup scheme under a multistage network topology. The dynamic path-setup scheme enables runtime path arrangement for arbitrary traffic permutations. The circuit-switching approach offers a guarantee of permuted data and its compact overhead enables the benefit of stacking multiple networks. .Design and development is done by XILINX 12.2 using Verilog and simulated on Modelsim 6.3f and implemented on Spartan 3 FPGA Device

I. INTRODUCTION

A trend of multiprocessor system-on-chip (MPSoC) design being interconnected with on-chip networks is currently emerging for applications of parallel processing, scientific computing, and so on. Permutation traffic, a traffic pattern in which each input sends traffic to exactly one output and each output receives traffic from exactly one input, is one of the important traffic classes exhibited from on-chip multiprocessing applications .Standard permutations of traffic occur in general-purpose MPSoCs, for example, polynomial, sorting, and fast Fourier transform (FFT) computations cause shuffled permutation, whereas matrix transposes or corner-turn operations exhibit transpose permutation. Recently, application-specific MPSoCs targeting flexible Turbo/LDPC decoding have been developed, and they exhibit arbitrary and concurrent traffic permutations due to multi-mode and multi-standard feature . In addition, many of the MPSoC applications (e.g., Turbo/LDPC decoding) compute in real-time, therefore, guaranteeing throughput (i.e., data lossless, predictable latency, guaranteed bandwidth, and in-order delivery) is critical for such permutation traffics. Most on-chip networks in practice are general-purpose and use routing algorithms such as dimension-ordered routing and minimal adaptive routing. To support permutation traffic patterns, on-chip permutation networks using application-aware routings are needed to achieve better performance compared to the general-purpose networks. These application-aware routings are configured before running the applications and can be implemented as source routing or distributed routing. However, such application-aware routings cannot efficiently handle the dynamic changes of a permutation pattern, which is exhibited in many of the application phases. The difficulty lies in the design effort to compute the routing to support the permutation changes in runtime, as well as to guarantee the permutated traffics. This becomes a great challenge when these permutation networks need to be implemented under very limited on-chip power and area overhead.

II. STATEMENT OF THE PROBLEM

The MPSoC applications compute in real-time, therefore, guaranteeing throughput (i.e., data lossless, predictable latency, guaranteed bandwidth, and in-order delivery) is critical for such permutation traffics. To support permutation traffic patterns, on-chip permutation networks using application-aware routings are needed to achieve better performance compared to the general-purpose networks. These application-aware routings are configured before running the applications and can be implemented as source routing or distributed routing. However, such application-aware routings cannot efficiently handle the dynamic changes of a permutation pattern. These permutation networks need to be implemented under very limited on-chip power and area overhead.

III. LITERATURE SURVEY

S. Borkar in their paper Present a Moore's Law continues with technology scaling, improving transistor performance to increase frequency, increasing transistor integration capacity to realize complex architectures, And reducing energy consumed per logic operation to keep power dissipation within limit. The future advances in technology, architecture, and software will not help to continue this law so, Network power for many core having difficult in power management . F. Gilbert in their paper proposes a Fat

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tree topology used for on chip network in order to achieve feasible condition for physical design but not support the scalability. A. Baghdadi and M. Jezequel in their paper propose an On-chip interconnection network adapted to a flexible multiprocessor LDPC/turbo decoder and based on the de-Bruijn network topology. Here the network having unique trade-off between flexibility and performance (scalability, frequency, area). O. Muller in their paper propose a Two multistage interconnection networks architectures are proposed in order to handle the on-chip communications in multiprocessor parallel turbo decoders based on Butterfly and Benes topologies. The main feature of the presented on-chip networks is their scalability and capability of permutation. S. R. Vangal in their paper propose a NoC architecture basic building block is the "network tile". The tiles are connected to an on-chip network that routes packets between them. Here tiled architecture use mesh topology provides greater integration high performance, good scalability and high energy efficiency. In the Proposed design on chip network supports guaranteed traffic permutation by using Clos network topology and pipelined circuit-switching approach. This networks implemented under very limited on-chip power and area.

IV. EXISTING METHODOLOGY

A. Topology: regular direct topologies, such as mesh and torus are intuitively feasible for physical layout in a 2-D chip. On the contrary, the high wiring irregularity and the large router radix of indirect topologies such as Benes or Butterfly pose a challenge for physical implementation. However, an arbitrary permutation pattern with its intensive load on individual source-destination pairs stresses the regular topologies and that may lead to throughput degradation. In fact, indirect multistage topologies are preferred for on-chip traffic-permutation intensive applications.

B. Switching technique: packet switching requires an excessive amount of on-chip power and area for the queuing buffers (FIFOs) with pre-computed queuing depth at the switching nodes and network interfaces.

C. Routing algorithm: Deflection routing is not energy-efficient due to the extra hops needed for deflected data transfer, compared to a minimal routing. Moreover, the deflection makes packet latency less predictable; hence, it is hard to guarantee the latency and the in-order delivery of data.

V. PROPOSED METHODOLOGY

A. Topology: Clos network is a kind of multistage circuit switching network, first formalized by Charles Clos in 1952 which represents a theoretical idealization of practical multi-stage telephone switching systems. Clos networks are required when the physical circuit switching needs to exceed the capacity of the largest feasible single crossbar switch. The key advantage of Clos networks is that the number of cross points (which make up each crossbar switch) required can be much fewer than were the entire switching system implemented with one large crossbar switch. When the Clos network was first devised, the number of cross points was a reasonable approximate indication of the total cost of the switching system. While this was acceptable for electromechanical crossbars, it has become less relevant with the advent of VLSI.

B. Switching technique: On-chip network employs a circuit-switching mechanism with a dynamic path-setup scheme under a multistage network topology. The dynamic path setup tackles the challenge of runtime path arrangement for conflict-free permuted data. The pre-configured data paths enable a throughput guarantee. By removing the excessive overhead of queuing buffers, a compact implementation is achieved and stacking multiple networks to support concurrent permutations in runtime is feasible.

C. Routing algorithm: Clos network, each input sends a probe containing a 4-bit output address to find an available path leading to the target output. During the search, the probe moves forwards when it finds a free link and moves backwards when it faces a blocked link. By means of non-repetitive movement, the probe finds an available path between the input and its corresponding idle output. The EBP-based path-setup scheme is designed with a set of probe routing algorithms

VI. PROPOSED ON-CHIP NETWORK DESIGN

Using small crossbar switches, Charles Clos introduced a type of interconnection network which is extensively studied and applied as a framework for ATM switches because it is economical, regular, scalable, fault-tolerant and highly efficient. Special attention has been paid to Clos three-stage networks as they are re-arrange able for developing multi-stage networks. These three stage

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networks are intended to be used for data communication and parallel computing system. A switching network is composed of one or more switch stages that can create various paths through creating various connections between their inputs and outputs. Clos three-stage network is an example of multi-stage switching networks Clos network is a multistage switching network. The advantage of such network is that connection between a large number of input and output ports can be made by using only small-sized switches. A bipartite matching between the ports can be made by configuring the switches in all stages. Clos network is defined as C (*n,m,p)* where n represents the number of inputs in each of p first-stage switches and m is the number of second-stage switches. In order to support a parallelism degree of 16 as in most practical MPSoCs .In proposed to use C (4,4,4) as a topology for the designed network. This network has a re-arrangeable property that can realize all possible permutations between its input and outputs. The choice of the three-stage Clos network with a modest number of middle-stage switches is to minimize implementation cost, whereas it still enables a re-arrangeable property for the network.

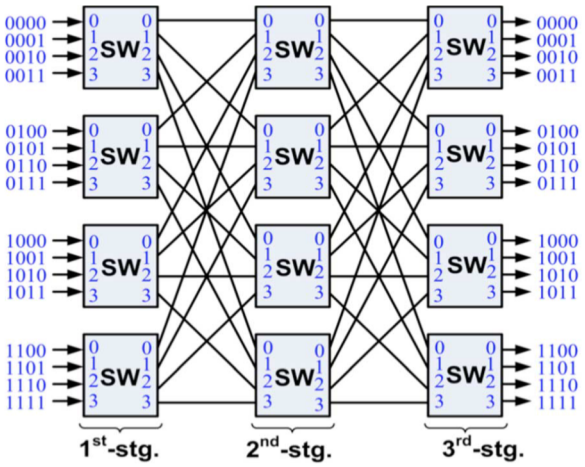


Fig.1: Proposed on-chip network topology with port addressing scheme

A. Path-Diversity Capacity

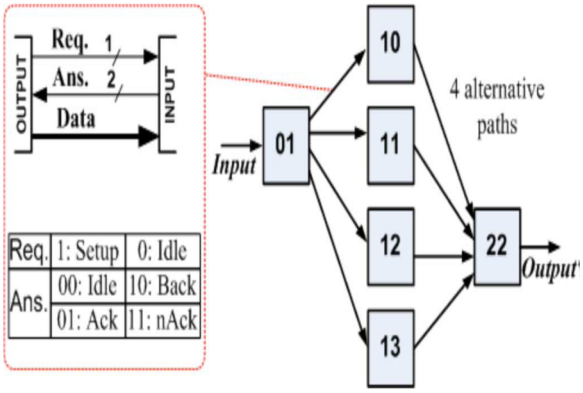


Fig.2: Switch-by-switch interconnection and path-diversity capacity

A pipelined circuit-switching scheme is designed for use with the proposed network. This scheme has three phases: the setup, the transfer, and the release A dynamic path-setup scheme supporting the runtime path arrangement occurs in the setup phase. In order to support this circuit-switching scheme, a switch-by-switch interconnection with its handshake signals is proposed A dynamic path-setup scheme supporting the runtime path arrangement occurs in the setup phase. In order to support this circuit-switching scheme, a switch-by-switch interconnection with its handshake signals is proposed. The bit format of the handshake includes a 1-bit Request (Req) and a 2-bit Answer (Ans). Req= 1 is used when a switch requests an idle link leading to the corresponding downstream switch in the setup phase. The Req=1 is also kept during data transfer along the set up path. A Req=0 denotes that the switch releases the occupied link. This code is also used in both the setup and the release phases. Ans=01(Ack) means that the destination is ready to receive data from the source. When the Ans=01 propagates back to the source, it denotes that the path is set up, then a data transfer

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can be started immediately. An Ans= 11(nAck)is reserved for end-to-end flow control when the receiving circuit is not ready to receive data due to being busy with other tasks, or overflow at the receiving buffer, etc. An Ans=10 (Back) means that the link is blocked. This Back code is used for a backpressure flow control of the dynamic path-setup Scheme. Assumed that a probe from a source (e.g., an input of switch 01) is trying to set up a path to a target destination (e.g., an available output of switch 22). First, the probe will non-repetitively try paths through the second-stage switches in the order of 10-11-12-13 Assuming that the link 01-10 is available, the probe first tries this link (Req=1) and then arrives at switch 10. If link 10-22 is available, the probe arrives at switch 22 and meets the target output. An Ans=Ack then propagates back to the input to trigger the transfer phase. If link 10-22 is blocked, the probe will move back to switch 01 (Ans=Back) and link 01-10 is released (Req=0) From switch 01, the probe can then try the rest of idle links leading to the second-stage switches in the same manner. By means of moving back when facing blocked links and trying others, the probe can dynamically set up the path in runtime in a conflict-avoidance.

B. Probe Routing Algorithm

A dynamic path-setup scheme is the key point of the proposed design to support a runtime path arrangement when the permutation is changed. Each path setup, which starts from an input to find a path leading to its corresponding output, is based on a dynamic probing mechanism. In which a probe (or setup flit) is dynamically sent under a routing algorithm in order to establish a path towards the destination. Exhausted profitable backtracking (EPB) is proposed to use to route the probe in the network work. A path arrangement with full permutation consists of sixteen path setups, whereas a path arrangement with partial permutation may consist of a subset of sixteen path setups. In the clos network, each input sends a probe containing a 4-bit output address to find an available path leading to the target output. During the search, the probe moves forwards when it finds a free link and moves backwards when it faces a blocked link. By means of non-repetitive movement, the probe finds an available path between the input and its corresponding idle output. The EBP-based path-setup scheme is designed with a set of probe routing algorithms.

C. Switch Design For Clos Network

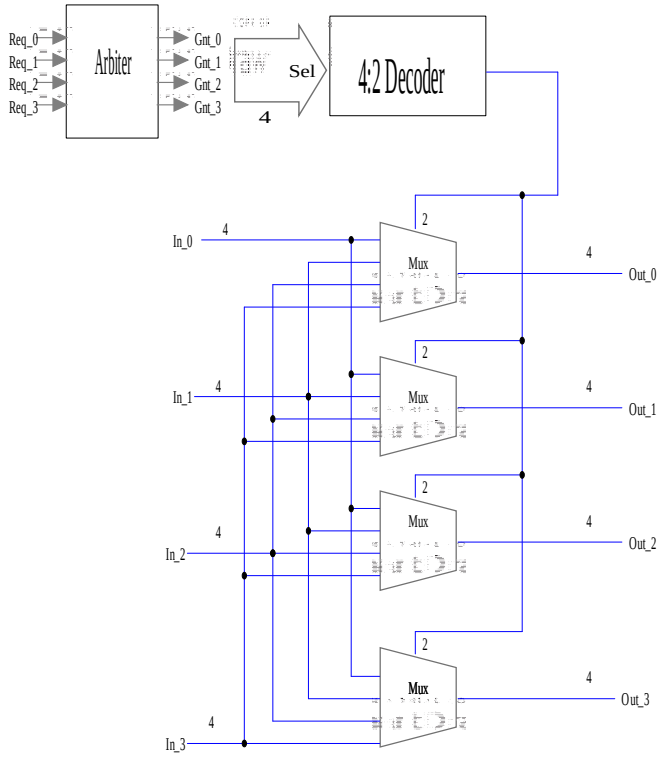


Fig.3: Common switch architecture.

The switch designing requires Arbiter; Decoder and Cross bar .In the above switch design arbiter input is the requests are Req_0; Req_1; Req_2; Req_3 and the output is the grants are Gnt_0; Gnt_1; Gnt_2; Gnt_3 this output is generated depending on the

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Request input . If reset is 0 in the arbiter we get the same output as input here request does not alter the output priority and If reset is 1 output priority get changed depending on request. 4:2 Decoder is connected to Cross bar or Mux architecture .This Mux architecture having input Data in_0; Data in_1; Data in_2; Data in_3 and Data out_0; Data out_1; Data out_2; Data out_3 here the data output is generated depending on the Request input in the arbiter.

D. Switch Flow Diagram

Arbiter input is the requests and the output is the grants this output is generated depending on the Request input. If reset is 0 in the arbiter we get the same output as input here request does not alter the output priority and If reset is 1 output priority get changed depending on request. Decoder is connected to Cross bar or Mux architecture .This Mux architecture having input Data input and Data output here the data output is generated depending on the Request input in the arbiter.

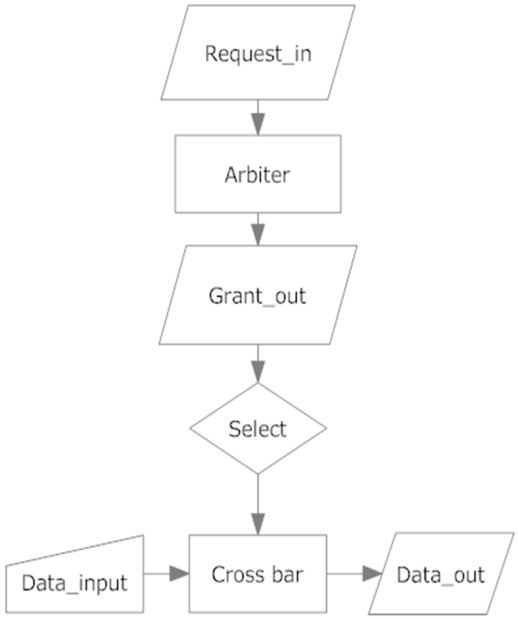


Fig.4: Switch design flow diagram

E. FIFO-Based Test Wrappers

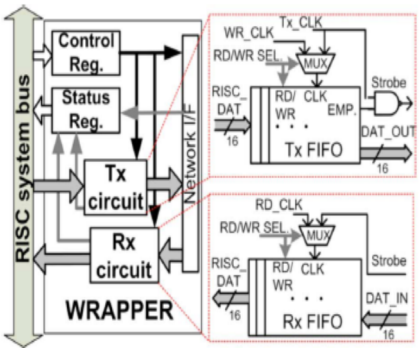


Fig.6: FIFO-based test wrappers supporting end to end source synchronous data transfer scheme

The above figure show the the FIFO-based test wrappers supporting and end to end source synchronous data transfer scheme here in order to check the end to end source synchronous data transfer scheme the FIFO-based test wrappers is used the four transmitter FIFO and four receiver FIFO is used between switches in the Proposed on-chip network topology with port addressing scheme .The Source-Synchronous clocking refers to a technique used for timing symbols on a digital interface. Specifically, it refers to the

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technique of having the transmitting device send a clock signal along with the data signals. The timing of the unidirectional data signals is referenced to the clock (often called the strobe) sourced by the same device that generates those signals, and not to a global clock (i.e. generated by a bus master). Compared to other digital clocking topologies like system-synchronous clocks, where a global clock source is fed to all devices in the system, a source-synchronous clock topology can attain far higher speeds.

VII. ADVANTAGES

Circuit switching provides higher switching capacity, No degradation of the response time and the path between the source and destination is first determined, all links along that path are reserved, and no buffers are needed in each node. After data transfer, reserved links are released for use by other messages and On-chip network achieves reduction of silicon overhead compared to other design approaches

VIII. APPLICATIONS

The main objective of the project is to design and develop an On-Chip Permutation Network for MPSOC for optimizing the area and power parameters based on FPGA, to investigate the shortfalls of the different methods and the present technology and to find out the advancements of new system. Also to analyze the scope for performance enhancements with respect to present system and new architecture will be simulated, implemented on FPGA and tested to reduce the power consumption and area on chip for the given system.

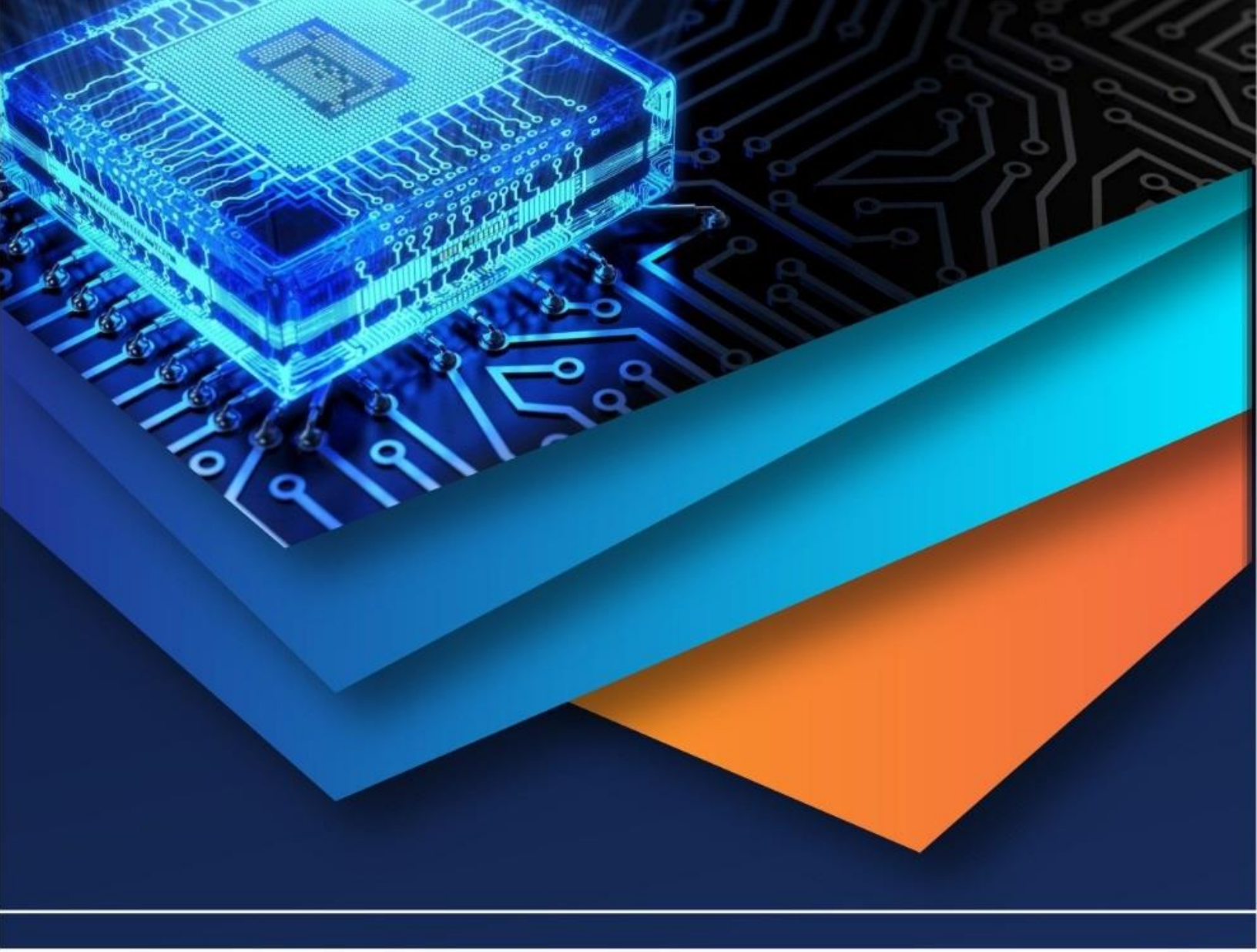
IX. CONCLUSION

An on-chip network design aiding traffic permutations in MPSoC applications has been defined in this paper. Using the Clos network topology, the prospected design offers random transfer arrangements in runtime with solid implementation cost by using a circuit-switching technique together with dynamic path-setup scheme.On-Chip Permutation Network for MPSOC for optimizing the area. The Design and development is done by XILINX 12.2 using verilog and simulated on Modelsim 6.3f and implemented on Spartan 3 FPGA Device.

REFERENCES

[1] S. Borkar, “Thousand core chips—A technology perspective,” in Proc. ACM/IEEE Design Autom. Conf. (DAC), 2007, pp. 746–749.
[2] P.-H. Pham, P. Mau, and C. Kim, “A 64-PE folded-torus intra-chip communication fabric for guaranteed throughput in network-on-chip based applications,” in Proc. IEEE Custom Integr. Circuits Conf. (CICC), 2009, pp. 645–648.
[3] C. Neeb, M. J. Thul, and N.Wehn, “Network-on-chip-centric approach to interleaving in high throughput channel decoders,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2005, pp. 1766–1769.
[4] H. Moussa, A. Baghdadi, and M. Jezequel, “Binary de Bruijn on-chip network for a flexible multiprocessor LDPC decoder,” in Proc. ACM/ IEEE Design Autom. Conf. (DAC), 2008, pp. 429–434.
[5] H. Moussa, O. Muller, A. Baghdadi, and M. Jezequel, “Butterfly and Benes-based on-chip communication networks for multiprocessor turbo decoding,” in Proc. Design, Autom. Test in Euro. (DATE), 2007, pp. 654–659.
[6] S. R. Vangal, J. Howard, G. Ruhl, S. Dighe, H. Wilson, J. Tschanz, D. Finan, A. Singh, T. Jacob, S. Jain, V. Erraguntla, C. Roberts, Y. Hoskote, N. Borkar, and S. Borkar, “An 80-tile sub-100-w TeraFLOPS processor in 65-nm CMOS,” IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 29–41, Jan. 2008.
[7] W. J. Dally and B. Towles, Principles and Practices of Interconnection Networks:. San Francisco, CA: Morgan Kaufmann, 2004.

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