iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 7 **Issue:** VII **Month of publication:** July 2019

DOI: http://doi.org/10.22214/ijraset.2019.7139

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue VII, July 2019- Available at www.ijraset.com

Design and Implementation of RoBA Multiplier on MAC Unit

Deepika Kumari M[1], Sandeep Chilumula[2]
[1, 2]*Electronics and Communication Engineerind Department, JNTUH University*

***Abstract:** In this paper, we design an approximate multiplier that is high speed, less complex & yet energy/power efficient. The main aim of the project is to approximate the multiplying operation. The operands are rounded off to the nearest exponent of two.*
The proposed approach is workable for both signed and unsigned operands as well. The proposed RoBA Multiplier is implemented with MAC unit to improve its speed & low power. MAC unit is the utmost requirement of today's VLSI applications like FFT, FIR Filters, convolutions, etc
Keywords: Accuracy, approximate computing, energy efficiency, error analysis, high speed, multiplier

I. INTRODUCTION

High speed, low power consumption & low area are the main the main parameters in any electronic applications like DSP, ASIC & FPGA. Power efficiency & high performance can be obtained by approximate computing & it can also decrease the design complexity.

A multiplier is one of the key hardware blocks in most of the DSP systems. Typical DSP applications where a multiplier plays an important role. Now a days electronic devices are portable, so power dissipation is one of the main concern .since multipliers are rather complex circuit and operates at high system clock rate, reduces the delay of multiplication.

In this paper, we pay attention to develop a high speed, low power & less complex approximate multiplier which withstands the error. This approach is called as rounding based approximate multiplication. It is workable for both signed & unsigned values.

The outline of this paper is

1) Developing a new method of multiplication by improvising the typical multiplication approach.
2) It is workable for both signed & unsigned operations.

MAC is one of the key building blocks of DSP. MAC unit determines power consumption & delay in the DSP. So it is pivotal in designing mac with less power consumption, less area & less delay.

The rest of the paper is arranged as follows. Section II discusses the proposed multiplier approach. In section III, the implementation of MAC Unit is presented. Results and simulations are studied in the section IV and finally conclusion is drawn in the section V

II. PROPOSED APPROXIMATE APPROACH

The concept behind the approximate multiplier is to easy the operation and to get the approximate results at the price of small error. In the proposed approximate multiplier, the operands are rounded off to the nearest exponent of two. Let us denote the rounded inputs numbers of the input of A & B by Ar & Br respectively.

The multiplication of A & B is written as

$$A \times B = (Ar - A) \times (Br - B) + Ar \times B + Br \times B - Ar \times Br. \quad \rightarrow (1)$$

The main aim is to simplify the operation of the multiplication Ar × Br, Ar×B, A×Br may be executed by the shift operation. The hardware implementation of (Ar – A) × (Br – B) can be neglected, as it is complex. Hence the multiplication can be performed by

$$A \times B = Ar \times B + Br \times B - Ar \times B \rightarrow (2)$$

Thus the operation can be done by using 3 shifters & two addition/subtraction operation. The values of the input values are rounded off to the nearest exponent of 2.

The following method includes:

A. Sign Detector

The sign detector detects the sign of the input values & gives the output. It extracts the most significant bit(MSB) of the input value. If the MSB of the input is '0', it will be considered as positive & if the MSB is '1', it will be regarded as negative.

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue VII, July 2019- Available at www.ijraset.com

B. Rounding

This block rounds off the input values to the nearest exponent of two. In the proposed method Z[i] is one in the following cases:
In the first case, Z[i] is one and all the left sided bits are zero while Z[i-1] is zero.
In the second case, when Z[i] and all the left sided bits are zero, z[i-1] and z[i-2] are both one.
Here we are using three barrel shifter blocks, the products Ar × B, Br × B, Ar × Br are determined. These input bits are shifted towards left side.

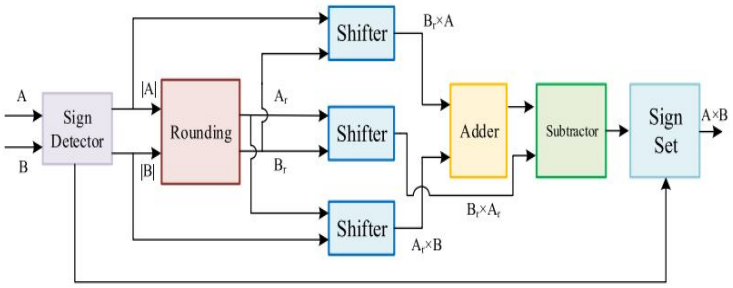


Fig. 1. Block diagram of the proposed multiplier

C. Adder

Parallel-Prefix adders perform parallel addition i.e. most important in microprocessors, DSPs, mobile devices and other high speed applications. Parallel-Prefix adders are primarily fast when compared to adder. The logic complexity & delay can be reduced by these adders. It improves the factors like area and power.
Parallel-Prefix adders are designed by considering carry look adder as base.Parallel-Prefix adders can be computed in these vital steps

1) Precalculation of Pi,Gi terms: Previous carry is calculated to the next bit is called propagate signal and generate is to generate the carry bit below are the signals

$$Gi = Ai.\ Bi$$
$$Pi = Ai \oplus Bi$$

2) Calculation of carries

$$Gi:j = Gi:k + Pi:k\ .\ Gk\text{-}1:$$
$$Pi:j = Pi:k\ .\ Pk\text{-}1:j$$

3) Simple adder to generate sum

$$Si = Pi \oplus Gi\text{-}1:0$$

In this paper we are using kooge-stone adder as it is more efficient.

a) *Kooge Stone Adder:* Kogge-Stone adder is a parallel-prefix form carry look ahead adder. Kogge-Stone adder was developed by Peter M. Kogge and Harold S. Stone which they published in1973. KS adder is a fast adder design as it generate carry signal in O (log2 n) time and has the best performance in VLSI implementations. KS adder has large area with minimum fan-out which increases its performance. Kogge-Stone adder is widely used in high performance 32-bit, 64-bit, and 128- bit adders as it reduces the critical path to great extent. Each vertical stage produce propagate and generate bits. Generate bits are produced in the last stage and XORed with initial propagate and generate bits to produce sum

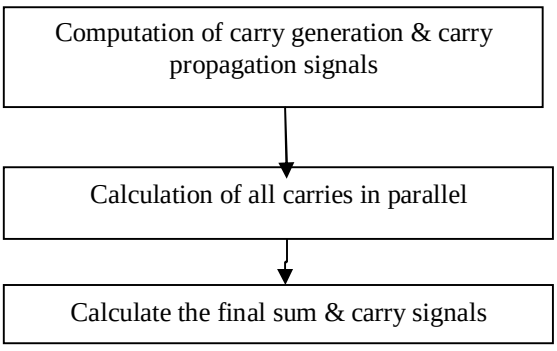


Fig. 2. Parallel Prefix Adder mechanism

©IJRASET: All Rights are Reserved

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue VII, July 2019- Available at www.ijraset.com

D. Sign Set

The main function of the sign set block is to set the sign of the final multiplication result.

III. MAC IMPLEMENTATION

Multiply Accumulate operation is one of the key processes taking place in a Digital Signal Processor. It finds application in filter designs, multimedia information processing, convolution, Fast Fourier Transforms etc. The unit determines the overall power consumption and computational delay of the processor. So it is pivotal in designing a MAC unit with less power consumption, less delay and less area. This is a major concern in the design of real time signal processing and DSP systems. MAC are the building blocks of the processor and has a great impact on the speed of processor.

MAC is composed of adder, multiplier and an accumulator. The inputs for the MAC are to be fetched from memory location and fed to multiplier block of MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location.

MAC mainly consist two parts

A. Multiplier

Two numbers are multiplied together, and added into an accumulator register. As shown in Fig.3, the basic MAC unit consists of multiplier, adder and accumulator. In general MAC unit uses the conventional multiplier unit, which consists of multiplication of multiplier and multiplicand based on adding the generated partial products and to compute the final multiplication. This results to adding the partial products. The key to the proposed MAC unit is to enhance the performance of MAC using RoBA Multiplier to get the final result of the multiplication.

B. Accumulator

Accumulator basically consists of register and adder. Register hold the output of previous clock from adder. Holding outputs in accumulator register can reduce additional add instruction. An accumulator should be fast in response so it can be implemented with one of fastest adder like carry look ahead adder or carry skip adder or carry select adder.

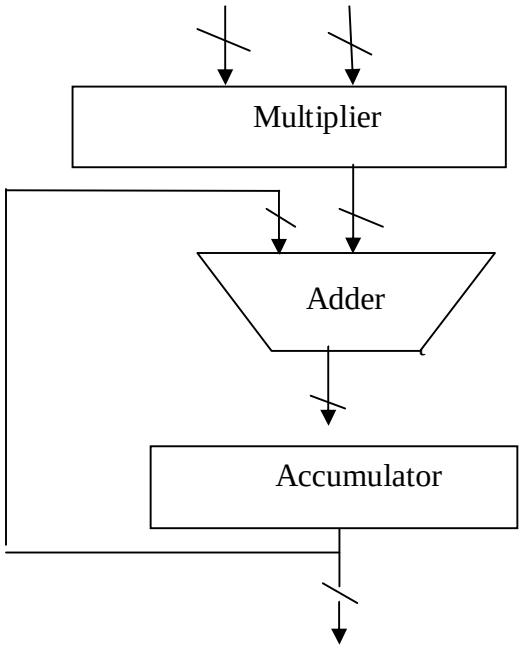


Fig. 3. MAC Unit

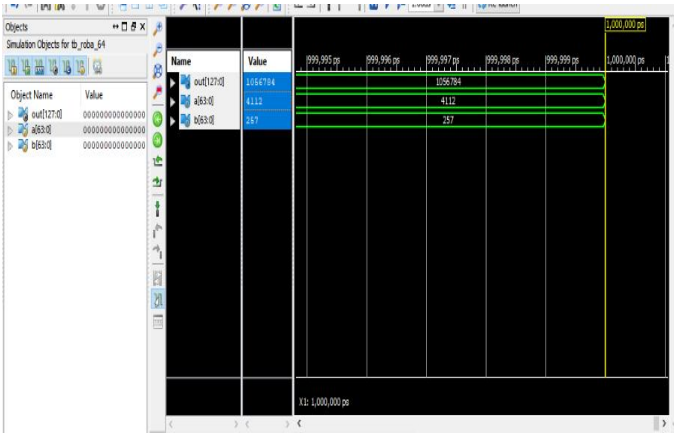
©IJRASET: All Rights are Reserved

IV. RESULTS & SIMULATIONS

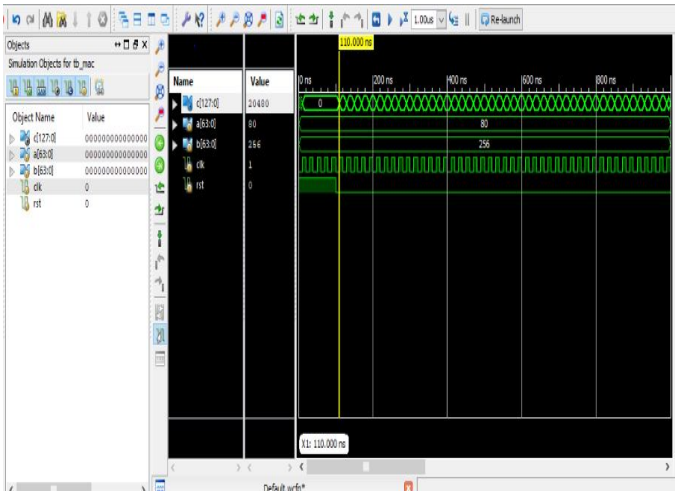
The values of Area, Power & delay of different bit RoBA Multiplier & also RoBA with MAC unit are mentioned in the following table. The multiplier are implemented using Verilog hardware description language and then synthesized using isim simulator.

TABLE I
Area, Delay & Power values of different bit RoBA Multiplier

	AREA	POWER	DELAY
8-bit RoBA Multipler	92 out of 8672	0.158 W	28,275 ns
16-bit RoBA Multipler	132 out of 8672	0.162 W	41.858 ns
32-bit RoBA Multipler	454 out of 8672	0.164 W	66.276 ns
64-bit RoBA Multipler	6779 out of 8672	0.168W	118.936 ns
64-bit RoBA Multipler with MAC unit	6598 out of 8672	0.165 W	70.936 ns



Simulated results of 64 bit RoBA Multiplier



Simulated results of 64 bit MAC Unit

©IJRASET: All Rights are Reserved

V. CONCLUSION

In this paper, we have proposed a 64 bit RoBA Multiplier with MAC unit which improves speed, decreases power consumption and low area.

The implemented method is based on the rounding off the input values to the nearest exponent of two. The proposed approximate multiplier has high accuracy when compared.

RoBA with MAC implementation provides low area, less delay and power in order to meet the current needs of the VLSI Industry. This approach is applicable for both signed and unsigned operations. In future, it can be used in various image processing applications.

.

REFERENCES

[1] M. Alioto, “Ultra-low power VLSI circuit design demystified and explained: A tutorial,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012.

[2] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, “Low-power digital signal processing using approximate adders,” IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137, Jan. 2013.

[3] H. R. Mahdiani, A. Ahmadi, S. M. Fakhraie, and C. Lucas, “Bio-inspired imprecise computational blocks for efficient VLSI implementation of soft-computing applications,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 4, pp. 850–862, Apr. 2010.

[4] R. Venkatesan, A. Agarwal, K. Roy, and A. Raghunathan, “MACACO: Modeling and analysis of circuits for approximate computing,” in Proc. Int. Conf. Comput.-Aided Design, Nov. 2011.

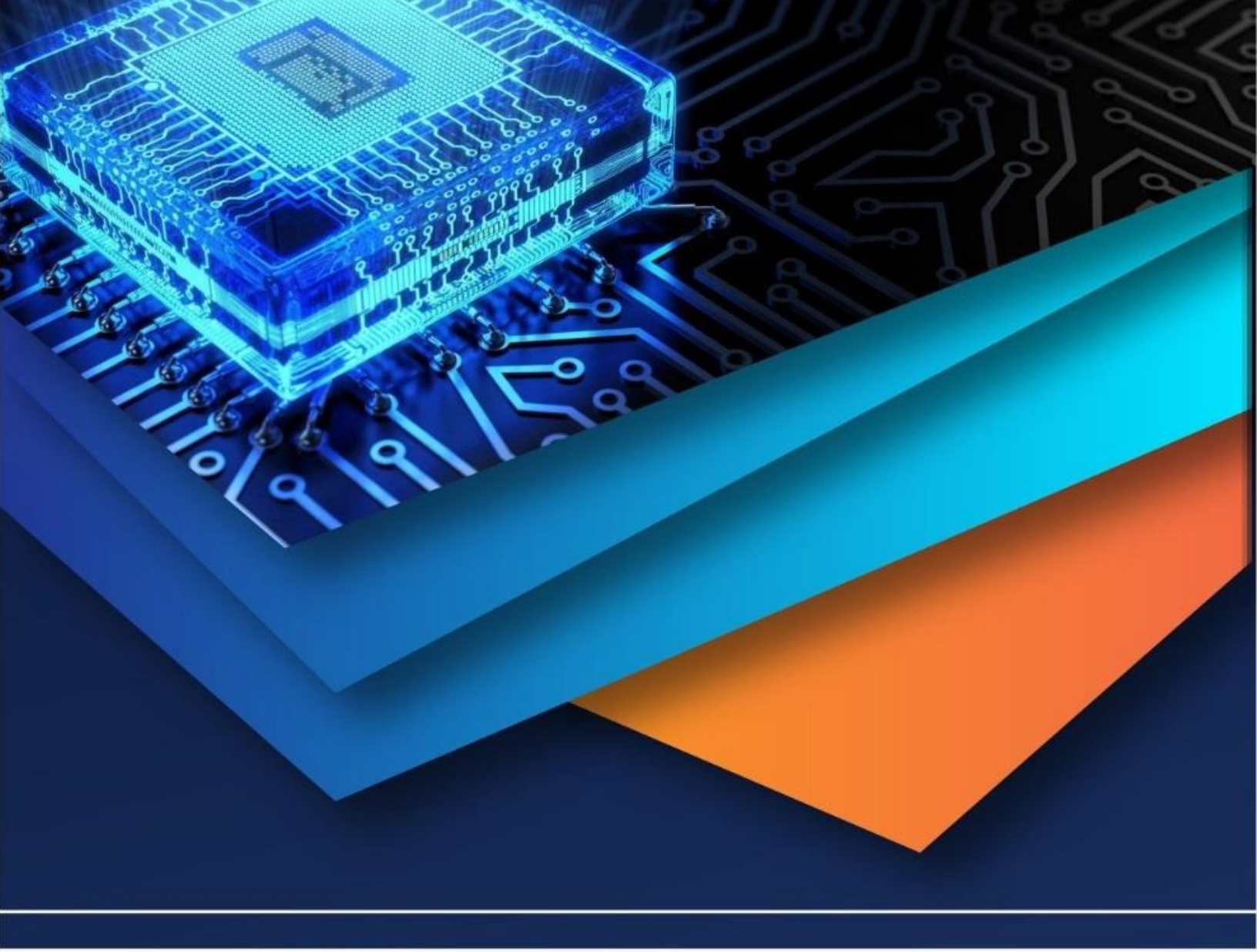
[5] F. Farshchi, M. S. Abrishami, and S. M. Fakhraie, “New approximate Booth Algorithm," IEEE Transactions on very large scale integration (vlsi) systems, vol. 18, no. 2,february 20 1

[6] Young-Ho Seo and Dong-Wook Kim, "New VLSI Architecture of Parallel Multiplier-Accumulator Based on Radix-2 Modified Booth Algorithm," IEEE Transactions on very large scale integration (vlsi) systems, vol. 18, no. 2,february 20 10

[7] Ron S. Waters and Earl E. Swartzlander, Jr., "A Reduced Complexity Wall ace Multiplier Reduction, " IEEE Transactions On Computers, vol. 59, no. 8, Aug

[8] Shanthala S, Cyril Prasanna Raj, Dr.S.Y.Kulkarni, "Design and VLST Implementation of Pipelined Multiply Accumulate Unit," IEEE International Conference on Emerging Trends inEngineering and Technology, ICETET-09 multiplier for low power digital signal is processing,” in Proc. 17th Int. Symp. Comput. Archit. Digit. Syst. (CADS), Oct. 2013.

©IJRASET: All Rights are Reserved



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)