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Elimination of Leakage Current in PV Based Current Source Inverter

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Abstract: ***This paper deals with the implementation of four leg inverter to eliminate the earth leakage current. In the PV based system, some amount of leakage current induces on the inverter output terminals due to high switching frequency and electromagnetic interface problem, which inject the leakage current into output load side. To eliminate the leakage current in the conventional system an isolation transformer can be used. This increase the cost and size of the system and reducing the overall efficiency and lifespan of the inverter. An implementation of four leg inverter in solar power system the leakage current can be eliminate through neutral coupling system. There by increasing efficiency and lifespan of inverter. The effectiveness of this proposed system was verified through MATLAB simulation and small scale prototype model.***
Index Terms— Transformerless CSI Inverter, Common Mode Leakage Current, SV -PWM.

I. INTRODUCTION

In the world, Renewable energy sources become a more and more important contribution to the total energy production. Today the solar energy production is very low as compared to the other renewable energy sources, but the PV systems are one of the fastest growing in the world. The price of PV system components is high, but especially the PV modules are decreasing and the market for PV system is expanding with high rate of rapidly. Solar power will be dominant because of its availability and reliability also. Photovoltaic inverters become more and more wide range of spread within both private and commercial circles.

In this paper, four legs are used to design a proposed system and the parallel connection between DC link inductors and DC link capacitor build in same core of inverter.

A. Addition of the fourth leg to avoids the possibility of undesirable current flow through neutral (or) any phases during zero state condition [2]. Series split capacitor arrangement and connects of neutral midpoint of split capacitor eliminating high frequency component from common mode voltage. This in terms restricts the flow of common mode leakage current [7].

B. Introduction of common mode inductor in DC link of high impedance to flow of common leakage current. The space vector pulse width modulation (SV-PWM) technique is used to producing gate pulse to IGPT switches in proposed inverter.

In the conventional system, three phase PWM CSI requires intermediate isolation transformer need to eliminate leakage current at output side [1]. So the use of transformer reduces 2-3% efficiency of the system. a modified CSI is proposed in this paper. It eliminates the high-frequency component in the common mode voltage, thereby suppressing the common mode earth leakage current.

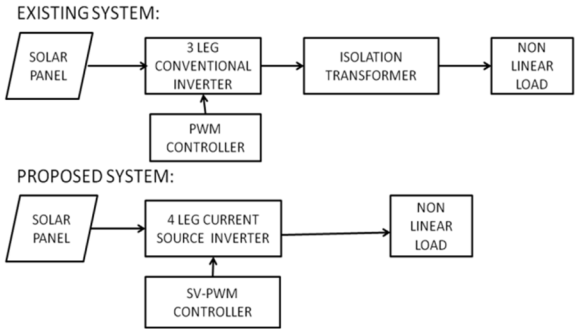


Fig.1.1. Block diagram

II. MODIFIED THREE-PHASE FOUR LEG INVERTER

The proposed four leg inverter consist of PV module is connected across the input dc capacitors. The dc-link is realized by the two

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capacitors are connected in series. Midpoint of these capacitors is connected to the neutral of the overall .DC-link inductors *Ldc*1 and *Ldc*2 are wound on the same core and therefore have a high value of mutual coupling. To generate ac current waveforms from the dc current, eight semiconductor switching devices are used. Each device has unidirectional current flow capability and can block the reverse voltage [2]. Either a diode connected in series with IGBT or reverse blocking (RB) IGBTs can be used to realize these switches. Output of three phases is connected to the load side through capacitor–inductor (C–L) filter and the fourth leg is connected to the neutral of the system as shown in Fig. 2.2. Components of the proposed inverter and their role in suppressing the earth leakage current are discussed below:

EXISTING SYSTEM:

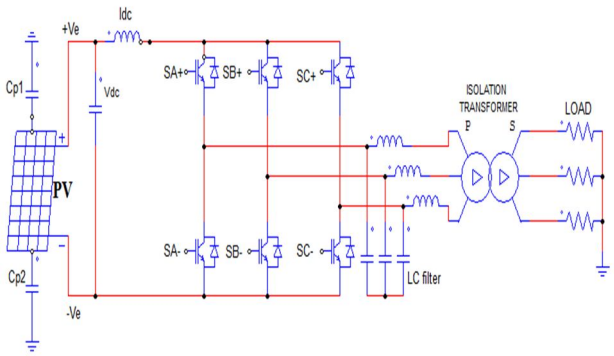


Fig.2.1 Existing three leg inverter

III. PROPOSED SYSTEM

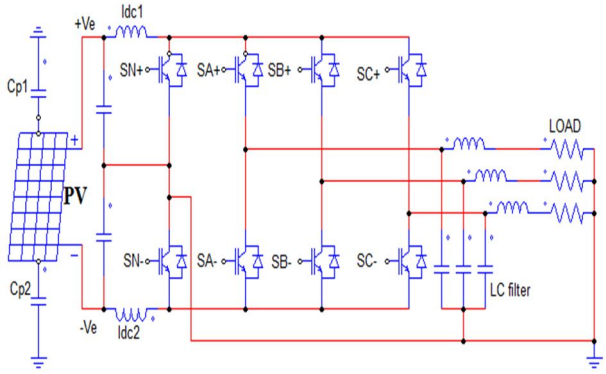


Fig.2.2 Proposed four leg inverter

A. Common Mode Inductor

Earth leakage current is a common mode nature and flows through both the -ve and +ve terminals of dc-link to the earth. Therefore, to reduce this current, common mode inductor is connected in the +ve and −ve dc-link. This inductor offers high impedance to the leakage current and reduces its magnitude. However, this addition does not eliminate the common mode voltage completely.

B. Split Capacitor DC-Link

Split capacitor dc-link is realized by connecting two capacitors in series. Midpoint of the link is connected to the system neutral [3]. During operation, dc-link voltages *vdc*1 and *vdc*2 are maintained almost constant. Therefore, voltage difference between PV terminals and neutral wire is a constant dc value without high frequency ac. Since neutral point is earthed at the substation, voltages across *Cp*1 and *Cp*2 are almost dc \without high-frequency ac. Therefore, no high-frequency earth leakage current would flow. This technique is being used in VSI systems also, but where split capacitor arrangement is used to reduce the leakage current. However, in CSI, this arrangement results in undesirable inverter currents during the “zero state.”

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C. Fourth Leg

Fig. 2.3 shows the reference waveform for inverter ac currents. The complete cycle is divided into six sectors. In sector-I, current reference for phase-A and phase-C is positive and that for phase-B is negative. To realize these reference currents, switches *SA*+, *SA*−, *SB*+, *SB*−, *SC*+, and *SC*− are modulated shows the current waveforms during a sampling period in sector-I. Solid lines are the average phase currents, and dotted lines indicate the instantaneous currents.

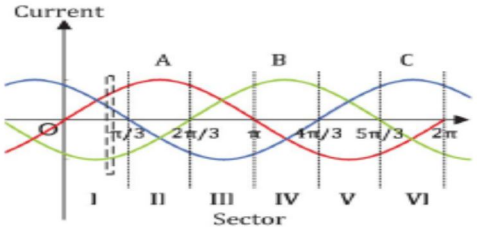


Fig 2.3Inverter reference current waveforms

SWITCHES	S1	S2	S3	S4	S5	S6	N1	N2
0-60	ON	OFF	OFF	OFF	OFF	ON	ON	OFF
60-120	ON	ON	OFF	OFF	OFF	OFF	OFF	ON
120-180	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
180-240	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
240-300	OFF	OFF	OFF	ON	ON	OFF	ON	OFF
300-360	OFF	OFF	OFF	OFF	ON	ON	OFF	ON

Fig.2.4. Switching states for proposed system

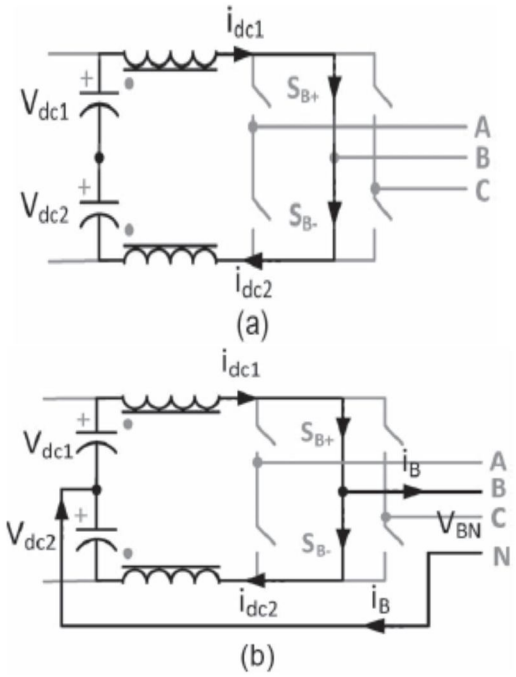


Fig 2.5 Current flow during zero state in(a) conventional CSI and (b) CSI with Split capacitor.

In the existing three leg current source inverter, the current flowing through phase-B and neutral during the zero state. Fig. 2.5(b) shows the flow of this additional current when phase-B voltage is negative. Due to current flow in phase B during the zero state, average value of current during the sampling period deviates from the desired value as shown in Fig. 2.5(b). This current flow during the zero state is undesirable and should be restricted [1]. In order to eliminate the flow of this current, additional pair of switches *SN*+ and *SN*− are connected across the dc-link. Midpoint of this new leg is connected to the neutral. For the zero state,

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instead of closing both switches of a particular phase, these switches are closed. Therefore, no current flows from any phase to neutral during this duration.

D. Space Vector Pulse Width Modulation

The main objectives of space vector pulse width modulation generated gate pulse are the following.

1) Wide linear modulation range.
2) Less switching loss.
3) Less total harmonic distortion in the spectrum of switching waveform Easy implementation and less computational calculations.

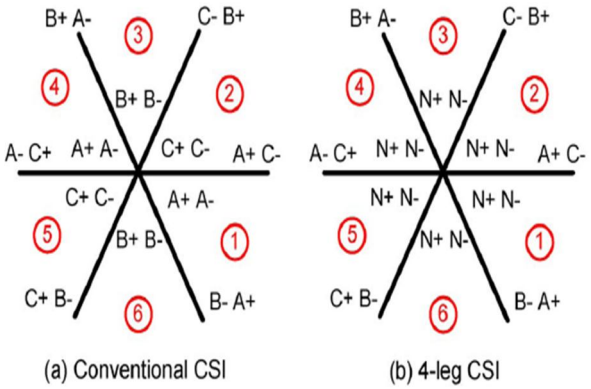


Fig 2.6 Space Vector Diagram

one of the three top switches carry *idc*, and one of the three bottom switches carry *idc*at any time. Since dc link current is same in both topologies (for same power delivered), total conduction losses remain same[7].

Switching losses: Since dc link current is same in both topologies, switching losses in CSI depend on the voltage appearing across the switch during turn-on and turn-off. Fig. 2.6(a) and (b) shows the switching states in conventional and four-leg Fig. 2.6. Space vector diagram for (a) conventional and (b) proposed fourleg CSI, respectively. Switching transitions in sector 1 for both the schemes are

Conventional CSI: (a+ a−) → (a+ b−) → (a+ c−) →
(a+ a−)

Proposed 4 − leg CSI: (n+ n−) → (a+ b−) → (a+ c−) → (n+ n−).

The transition (a+ b−) → (a+ c−) is same for both the circuits, and hence there will not be any difference in the losses for this transition. Consider the switching transition (a+ a−) → (a+ b−) in conventional CSI and the switching transition (n+ n−) → (a+ b−) in four-leg CSI. In conventional CSI, there is only one transition (a−→b−), and its loss is proportional to the line voltage *Vab* appearing across the switches. In case of four-leg CSI, there are two transitions at this instant (n+ → a+) and (n−→b−), and the switching loss depends on phase voltages *Van* and *Vnb* appearing across the switches at that instant, respectively [8]. As *Van* and *Vnb* are positive in this sector, instantaneous value of *Vab* is equal to the sum of instantaneous values of *Van* and *Vnb*. Therefore, loss in conventional CSI for transition (a−→b−) is approximately equal to the sum of losses in proposed CSI for transitions (n+ → a+) and (n−→b−). Similarly, loss in conventional CSI for transition (a+ c−) → (a+ a−) is equal to loss in proposed CSI for transition (a+ c−) → (n+ n−). The total switching loss in conventional and four-leg CSI is approximately same. In case of four-leg CSI, losses are distributed over more number of devices than that in conventional CSI.

IV. SIMULATION AND RESULTS

Simulations were performed by using MATLAB-Simulink to verify that the proposed PV based current source inverter can be practically implemented in power applications such as solar power generation, etc. It helps one to confirm the SV PWM switching

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strategy can be implemented for the proposed topology. Then, this strategy is implemented in a real time environment, i.e., to produce SV PWM switching signals for the switches. The following figures and data are given from the simulated results of proposed topology.

PARAMETER FOR SIMULATION

Parameter	Values
AC filter inductor Lf	5 mh
AC filter capacitor Cf	650 µf
Common mode inductor	400mh
Differential mode inductor	1.3 mh
DC link capacitor	5600µf
Reference DC link voltage	142 V

Table No 3.1 Parameters For Simulation

A. Simulation Circuit

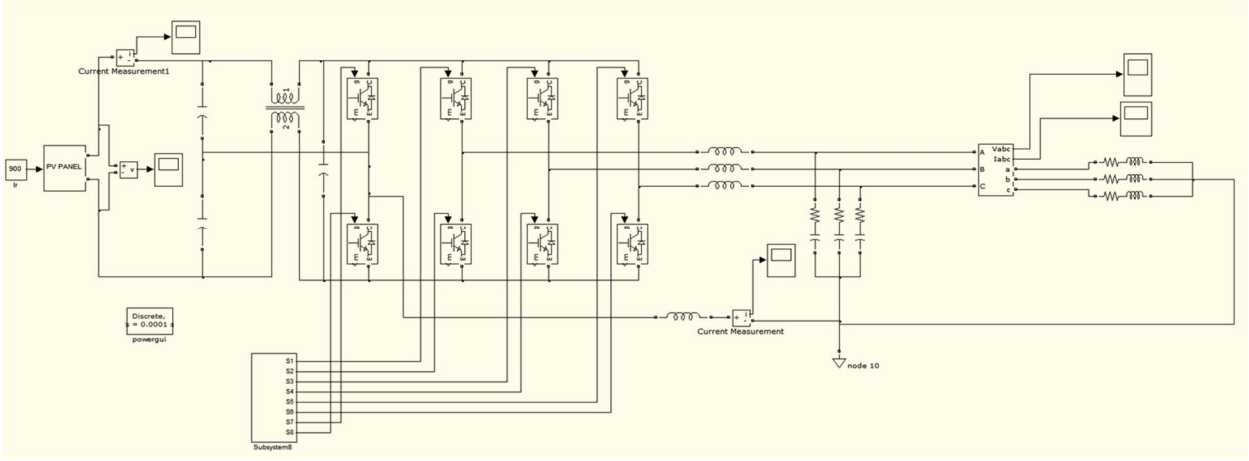


Fig 3.1simulation Circuit

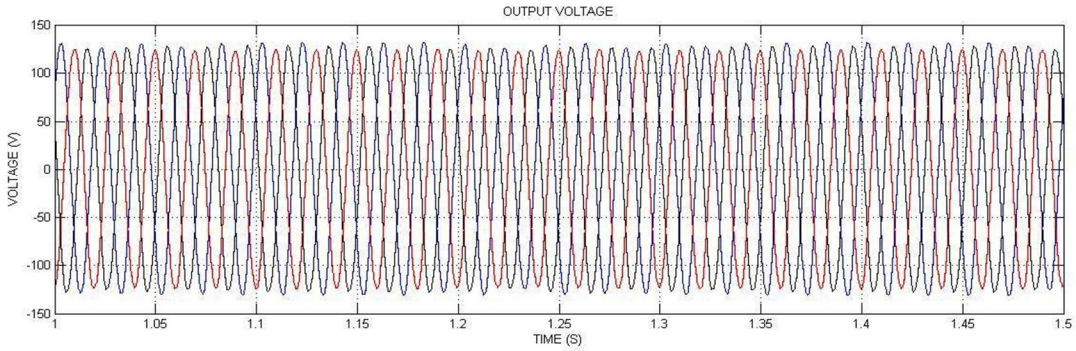


Fig 3.2 Inverter Output Voltage

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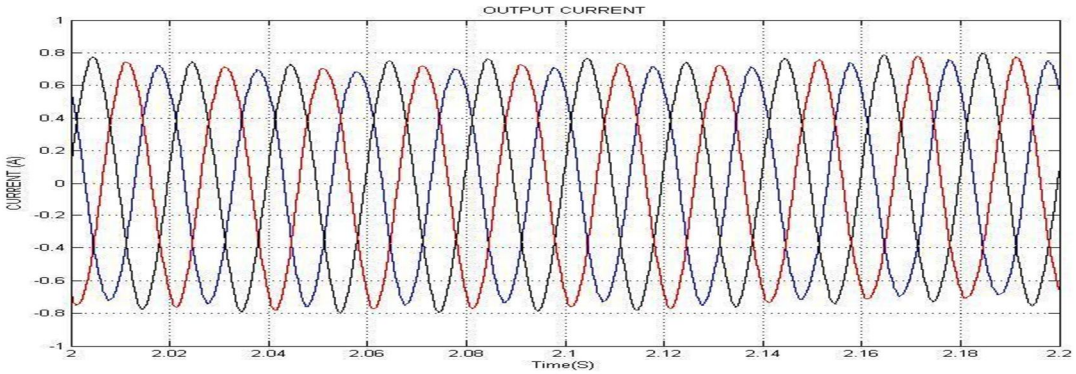


Fig 3.3Inverter output current.

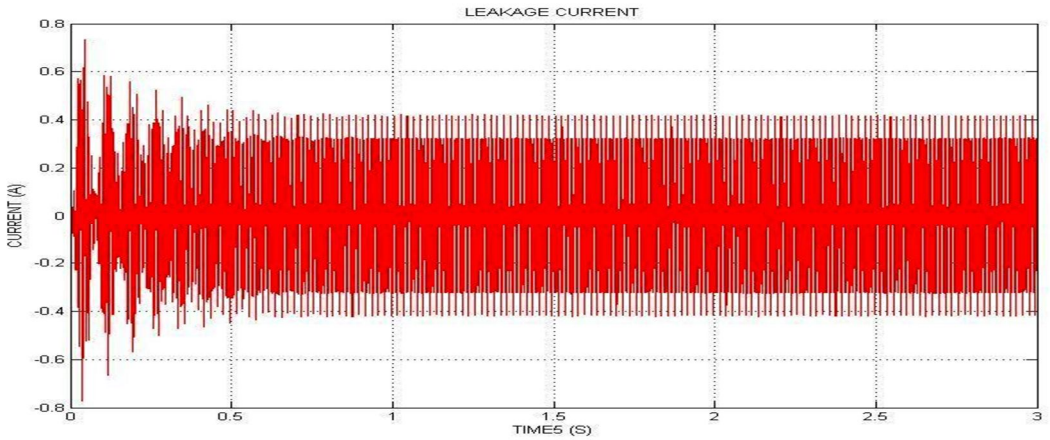


Fig 3.4 Leakage Current

V. HARDWARE DEVELOPMENT

This hardware development describes in detail of the hardware components, which consist of control circuit and driver circuit for hybrid system. The hybrid system having three trigging circuit and Tone controller taken so on. The control circuit is the PIC microcontroller circuit which generates the gate signals to the power circuit. The driver circuit is used to amplify the gate signals generated by the PIC microcontroller. The general structure of hybrid system is given below.

A. Proposed Hardware

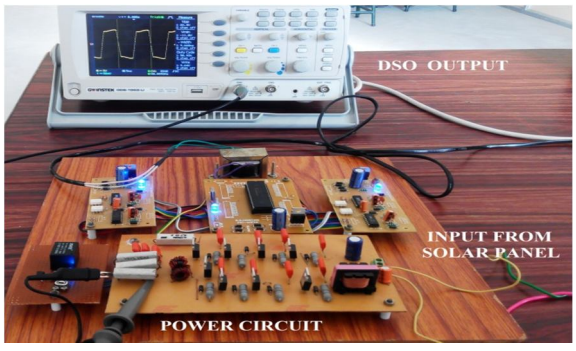


Fig 4.1 Proposed Hardware

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HARDWARE RESULTS

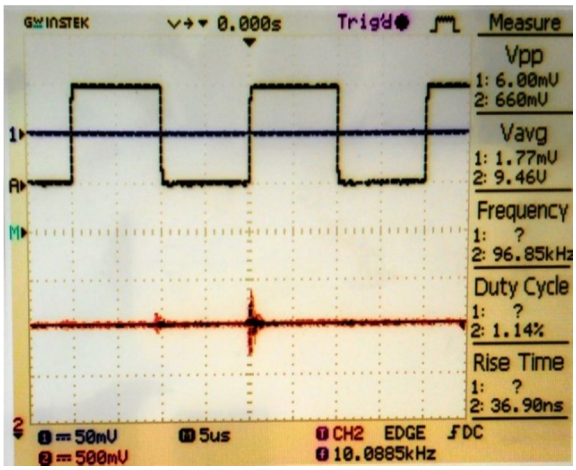


Fig 4.2 Inverter Input Voltage

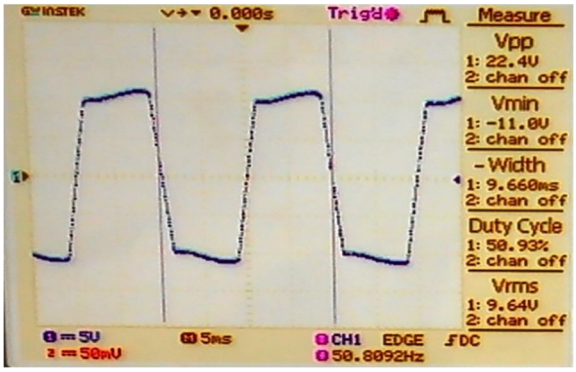


Fig 4.3 Inverter Output Voltage

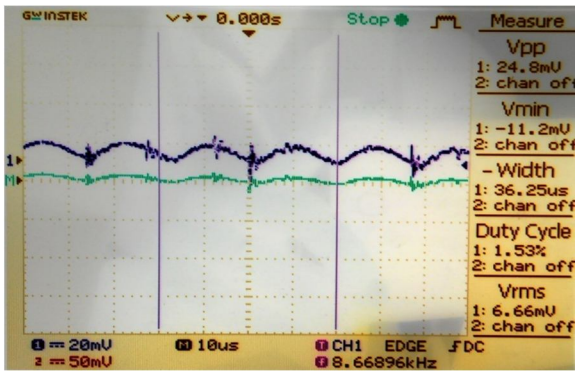


Fig 4.4 Inverter Neutral Voltage

HARDWARE PARAMETERS:

Inverter Input voltage Vdc = 10 volts
Inverter output voltage Vac = 11 volts.
Neutral voltage = 11 mv.

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Neutral resistance = 4.7 ohms.
Therefore neutral current = Vn/Rn.
= 11/4.7
Eliminated neutral current = 2.3 mA .

VI. CONCLUSION

In this proposed system, a four leg current source inverter can be implemented and the leakage current also eliminated through the neutral point of the proposed system in this paper. The simulation and hardware results are discussed in above and Where the THD value for output current was calculated as 3.49%.so the efficiency of this proposed system can be increased and also overall system size, cost can be reduced and lifespan of the proposed system increased through failure of equipment reduced. This proposed four leg current source inverter is very suitable for solar power generation for efficient utilization of solar energy.

REFERENCES

[1] Sandeep Anand, Saikrishna Kashyap Gundlapalli, and B. G. Fernandes, "Transformer-Less Grid Feeding Current Source Inverter for Solar Photovoltaic System,"IEEE Trans. Power Electron., vol., no. 10, oct 2014
[2] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology,"IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 184–191, Jan. 2011.
[3] B. Mirafzal, M. Saghaleini, and A. K. Kaviani, "An SVPWM-based switching pattern for stand-alone and grid-connected three-phase singlestageboost inverters," IEEE Trans. Power Electron., vol. 26, no. 4, pp. 1102–1111, Apr. 2011.
[4] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology,"IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 184–191, Jan. 2011.
[5] P. P. Dash and M. Kazerani, "Dynamic modeling and performance analysisof a grid-connected current-source inverter-based photovoltaic system,"IEEE Trans. Sustain. Energy, vol. 2, no. 4, pp. 443–450, Oct. 2011.
[6] E. Al-Nabi, B. Wu, N. R. Zargari, and V. Sood, "Sensorless control ofCSC-fed IPM machine for zero- and low-speed operations using pulsatingHFI method," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1711–1723,May 2013.
[7] B. Sahan, S. V. Araújo, C. Nöding, and P. Zacharias, "Comparativeevaluation of three-phase current source inverters for grid interfacing ofdistributed and renewable energy systems," IEEE Trans. Power Electron.,vol. 26, no. 8, pp. 2304–2318, Aug. 2011.
[8] M. A. G. de Brito, L. Galotto, L. P. Sampaio, G. e Melo, and C. A. Canesin, "Evaluation of the main MPPT techniques for photovoltaic applications," IEEE Trans. Ind. Electron., vol. 60, no. 3, pp. 1156–1167, Mar. 2013.
[09] Y. Chen, K. Smedley, and J. Brouwer, "A cost-effective three-phase grid connected inverter with maximum power point tracking," in Conf. Rec. 41st IEEE IAS Annu. Meet., Tampa, FL, USA, Oct. 2006, vol. 2, pp. 995– 1000.



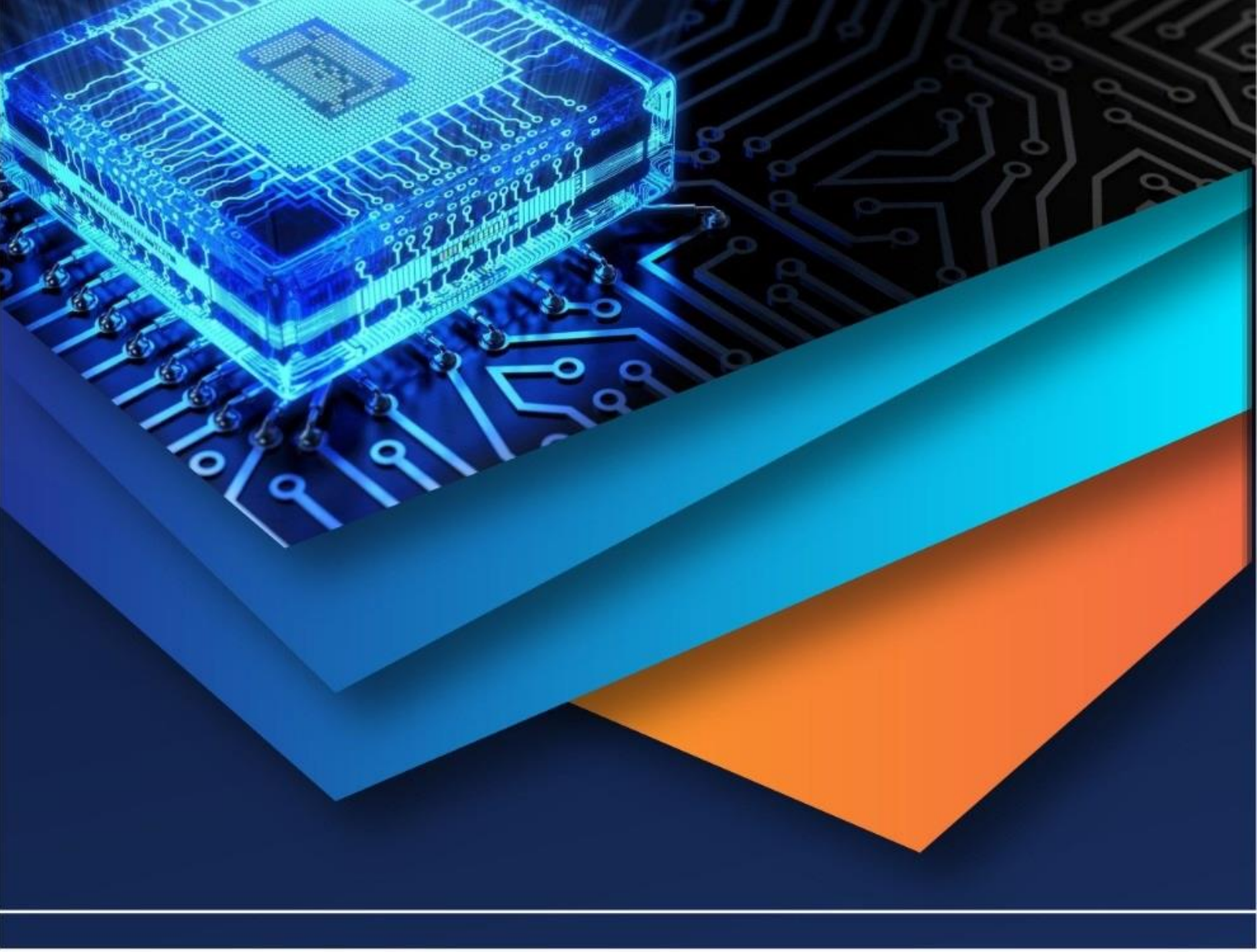
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