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Performance Analysis of High-Speed Adders

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Abstract: ***Adders are one of the most widely digital components in the digital integrated circuit design. In any arithmetic function addition plays a role of most fundamental operation. Adders are commonly used in miscellaneous application in modern VLSI system like multiplier design, design of an ALU, and also in various Digital Signal Processing algorithms like FIR, IIR Filter design. Designing an excellent and efficient of an adder circuit a designer must optimize the parameters like area, delay, and power. We have to tradeoff between all three parameters to get an efficient design. Depending upon the need and application some changes and compromises have to be made In this paper, the design of various adders such as Ripple Carry Adder, Carry Skip Adder, Carry Increment Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Select Adder, Carry Bypass Adder are discussed and are compared on the basis of their performance parameters such as area, delay and power distribution.***
Keywords: Power,Area, Delay, Verilog HDL,Xilinx, Carry Bypass Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Select Adder, Carry Skip Adder, Ripple Carry Adder.

I. INTRODUCTION

The most important feature of modern day electronics is to build low power high speed devices both due to increase in integration of components and reduction in size. Over the decades the battery life has only improved by a factor of 2 or 4 whereas the power of digital IC's has increased with over four orders of magnitude.A low power design needs to be adopted for future advancements or else the devices will suffer from a short battery life or very heavy battery packs. It is also important to avoid local areas of high power dissipation which may cause hotspots, and also to reduce the need for a low power impedance and ground distribution network which may interfere with signal interconnections. All complex adder architectures are constructed from its basic building blocks such as Half Adder (HA) and Full Adder (FA). In this paper, the performance parameters of various adders are compared

II. ADDERS

The design of various adders such as Ripple Carry Adder (RCA), Carry Skip Adder (CSkA), Carry Look Ahead Adder (CLA), Carry Save Adder (CSA) and Carry Select Adder (CSlA) are discussed below.

A. Ripple Carry Adder

A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded , with the carry output from each full adder connected to the carry input of the next full adder in the chain. Figure 3 shows the interconnection of 16 full adder (FA) circuits to provide a 16-bit ripple carry adder[1]. Notice from Figure that the input is from the right side because the first cell traditionally represents the least significant bit (LSB). Bits A0 and B0 in the figure represent the least significant bits of the numbers to be added. The sum output is represented by the bits S0 – S15.

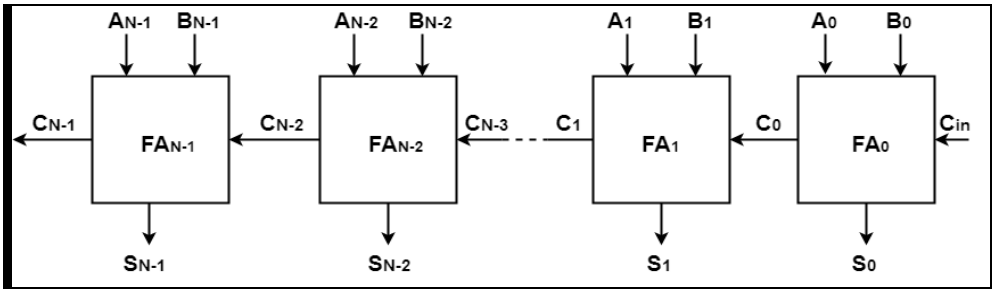


Figure 1 N-Bit Ripple Carry Adder

In the ripple carry adder, the output is known after the carry generated by the previous stage is produced. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay.

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B. Carry Look Ahead Adder (CLA)

The ripple carry adder, although simple in concept, has a long circuit delay due to the many gates in the carry path from the least significant bit to the most significant bit. For a typical design, the longest delay path through an n-bit ripple carry adder is approximately 2n + 2 gate delays. Thus, for a 16-bit ripple carry adder, the delay is 34 gate delays. This delay tends to be one of the largest in a typical computer design[3]. Accordingly, we find an alternative design, the carry lookahead adder, attractive. This adder is a practical design with reduced delay at the price of more complex hardware. The carry lookahead design can be obtained by a transformation of the ripple carry design into a design in which the carry logic over fixed groups of bits of the adder is reduced to two-level logic. The transformation is shown for a 4-bit adder group in Figure 2.

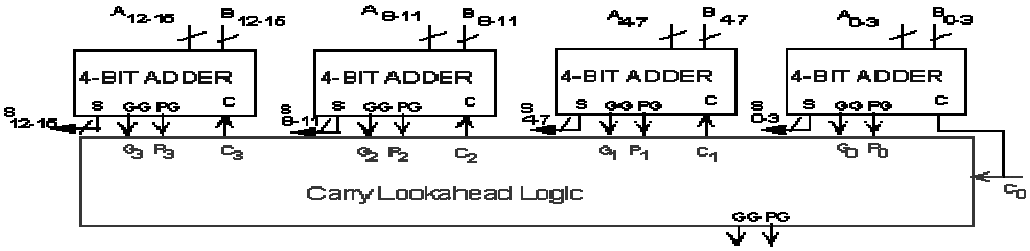


Figure 2. 16-Bit Carry lookahead adder (CLA)

The architecture of CLA is given in figure 3

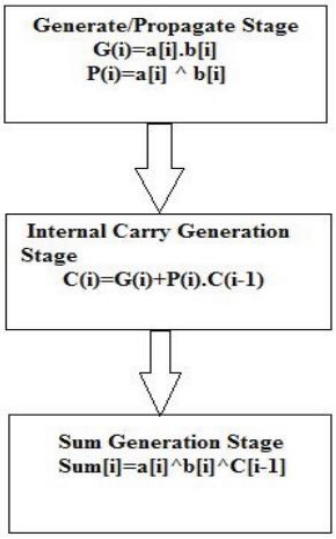


Figure 3 Flow chart of CLA

C. Carry Save Adder (CSA)

A Carry-Save Adder is just a set of one-bit fulladders and Half adders, without any carry-chaining[4]. Therefore, an n-bit CSA receives three n-bit operands, namely A(n-1)..A(0), B(n-1)..B(0), and CIN(n-1)..CIN(0), and generates two n-bit result values, SUM(n-1)..SUM(0) and COUT(n-1)..COUT(0). The architecture of 16 bit CSA is shown in figure 4

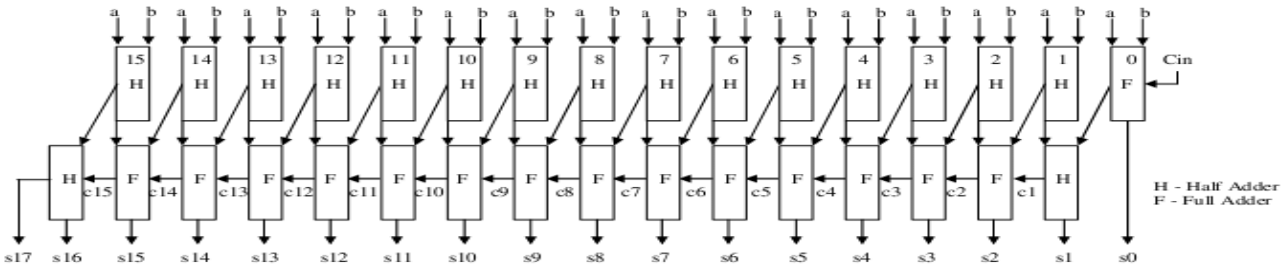


Figure 4. 16-Bit Carry Save Adder (CSA)

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The most important application of a carry-save adder is to calculate the partial products in integer multiplication. This allows for architectures, where a tree of carry-save adders (a so called *Wallace tree*) is used to calculate the partial products very fast. One 'normal' adder is then used to add the last set of carry bits to the last partial products to give the final multiplication result. Usually, a very fast carry-lookahead or carry-select adder is used for this last stage, in order to obtain the optimal performance.

D. Carry Skip Adder (CSkA)

Since the Cin-to-Cout represents the longest path in the ripple-carry-adder an obvious attempt is to accelerate carry propagation through the adder[2]. This is accomplished by using Carry-Propagate pi signals within a group of bits. If all the pi signals within the group are pi = 1, the condition exist for the carry to bypass the entire group:

$$P= P_i \, . \, P_{i+1}.P_{i+2}.....P_{i+k}$$

The Carry Skip Adder (CSKA) divides the words to be added into groups of equal size of k-bits. The basic structure of an N-bit Carry Skip Adder is shown on figure. Within the group, carry propagates in a ripple-carry fashion. In addition, an AND gate is used to form the group propagate signal P. If P = 1 the condition exists for carry to bypass (skip) over the group as shown in figure 5.

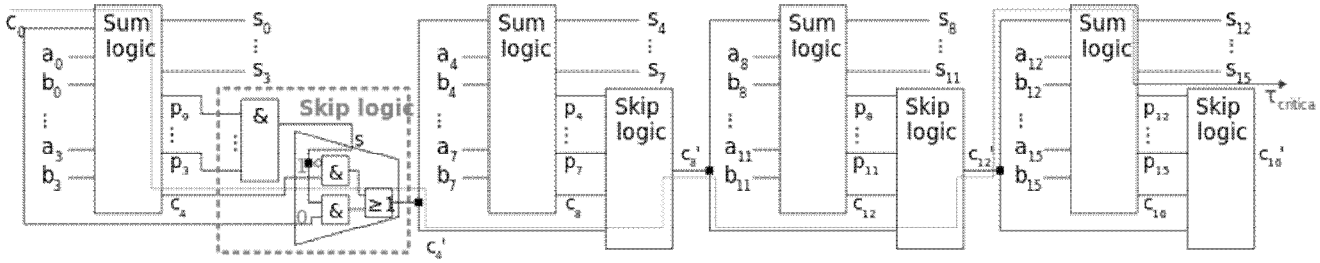


Figure 5. 16-Bit Carry Skip Adder (CSkA)

E. Carry Select Adder (CSlA)

Carry Select Adder (CSlA) architecture consists of independent generation of sum and carry i.e., Cin=1 and Cin=0 are executed parallelly[5] . Depending upon Cin, the external multiplexers select the carry to be propagated to next stage. Further, based on the carry input, the sum will be selected. Hence, the delay is reduced. However, the structure is increased due to the complexity of multiplexers . A carry-select adder speeds 40% to 90%faster than RCA by performing additions in parallel and reducing the maximum carry path[6]. The architecture of CSlA is illustrated in figure 6.

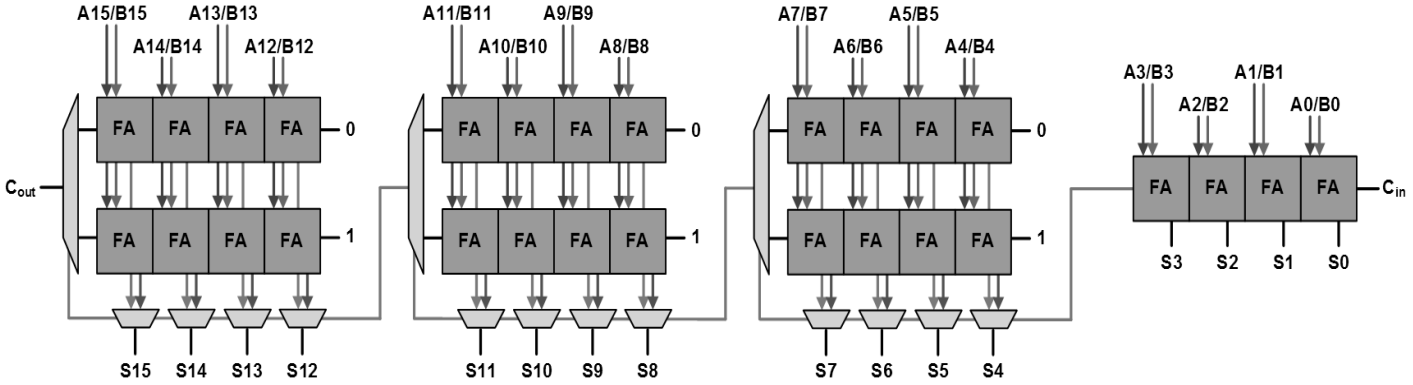


Figure 6. 16-Bit Carry Select Adder (CSlA)

TABLE I
PERFORMANCE COMPARISON TABLE FOR 8 BIT ADDERS

Name of Adders	Power (in mw)	Delay (ns)	Area(cell area)
RCA	0.7	5.2	2199
CLA	0.9	4.1	2256
CSA	0.8	4.3	1993
CSkA	1.1	3.7	1879
CSlA	1.3	3.5	2100

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III.DEVICE UTILIZATION

A. Ripple Carry Adder

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	32	7,168	1%
Logic Distribution			
Number of occupied Slices	24	3,584	1%
Number of Slices containing only related logic	24	24	100%
Number of Slices containing unrelated logic	0	24	0%
Total Number of 4 input LUTs	32	7,168	1%
Number of bonded IOBs	50	97	51%
Total equivalent gate count for design	192		
Additional JTAG gate count for IOBs	2,400		

B. Carry Look Ahead Adder (CLA)

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	32	7,168	1%
Logic Distribution			
Number of occupied Slices	24	3,584	1%
Number of Slices containing only related logic	24	24	100%
Number of Slices containing unrelated logic	0	24	0%
Total Number of 4 input LUTs	32	7,168	1%
Number of bonded IOBs	50	97	51%
Total equivalent gate count for design	192		
Additional JTAG gate count for IOBs	2,400		

C. Carry Save Adder (csa)

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	48	3,840	1%
Logic Distribution			
Number of occupied Slices	28	1,920	1%
Number of Slices containing only related logic	28	28	100%
Number of Slices containing unrelated logic	0	28	0%
Total Number of 4 input LUTs	48	3,840	1%
Number of bonded IOBs	50	97	51%
Total equivalent gate count for design	303		
Additional JTAG gate count for IOBs	2,400		

D. carry Skip Adder (cska)

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	39	7,168	1%
Logic Distribution			
Number of occupied Slices	24	3,584	1%
Number of Slices containing only related logic	24	24	100%
Number of Slices containing unrelated logic	0	24	0%
Total Number of 4 input LUTs	39	7,168	1%
Number of bonded IOBs	49	97	50%
Total equivalent gate count for design	237		
Additional JTAG gate count for IOBs	2,352		

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E. Carry Select Adder (csla)

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	44	7,168	1%
Logic Distribution			
Number of occupied Slices	25	3,584	1%
Number of Slices containing only related logic	25	25	100%
Number of Slices containing unrelated logic	0	25	0%
Total Number of 4 input LUTs	44	7,168	1%
Number of bonded IOBs	50	141	35%
Total equivalent gate count for design	282		
Additional JTAG gate count for IOBs	2,400		

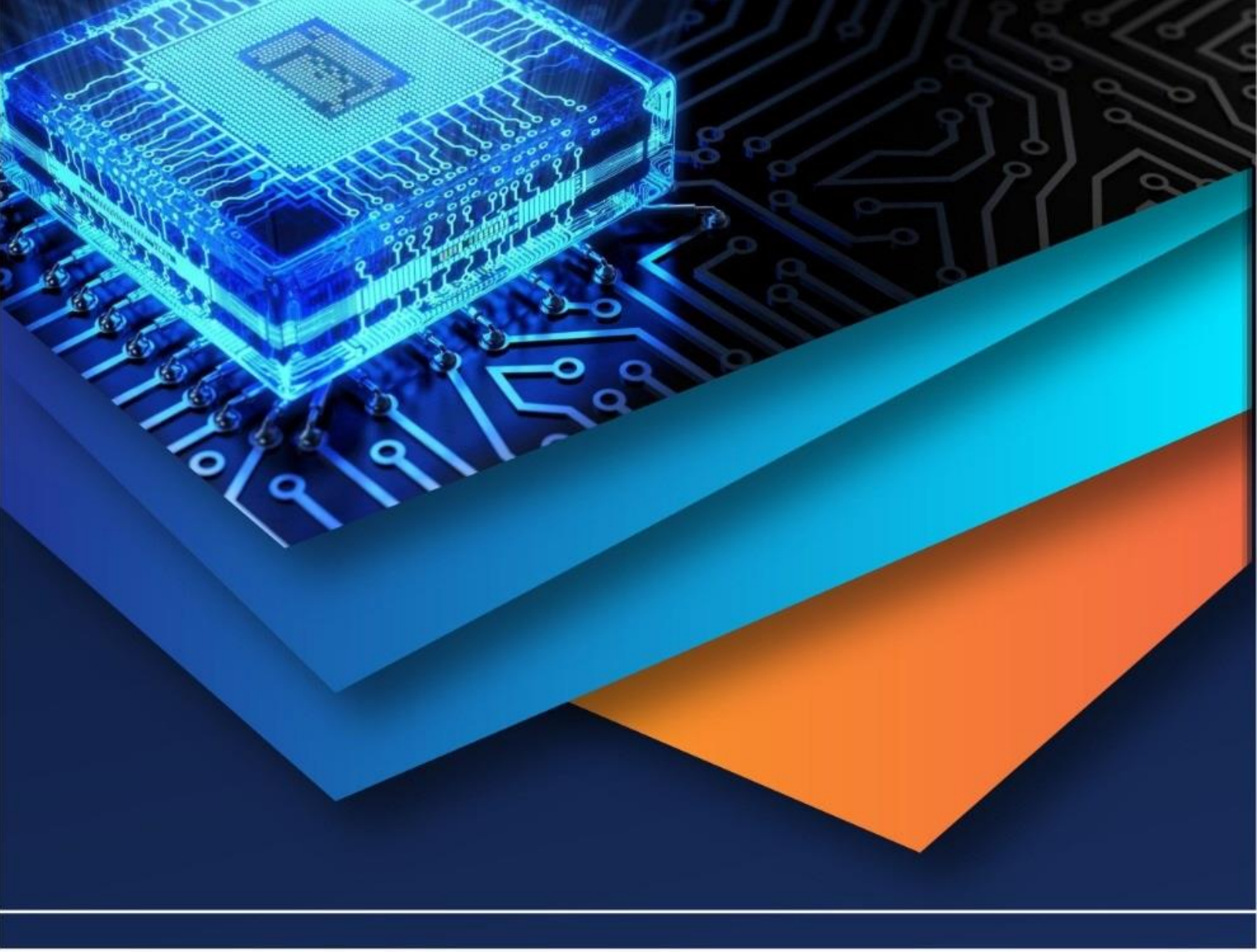
IV. CONCLUSION

Various Adders are designed simulated and synthesized using Verilog HDL in Xilinx ISE.Adder achieves better performance in terms of area and delay compared to that of other adder topologies. In future work, it is needed to design unique adder which provides low area as well as delay in order to meet the needs of current VLSI industry.

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