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Wide Bandwidth CMOS Low Noise Amplifier Using Matched Coplanar Waveguide Line for Wireless Communication

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Abstract—In this work, the simulation analysis of low noise amplifier and rectangular micro-strip patch antenna is proposed. In this, two different modules are proposed and analysed through Agilent ADS tool. Firstly, a rectangular patch antenna is designed that is resonant at approx 14GHz with micro-strip feeding and simulated in ADS tool and achieves reflection coefficient of -22dB. Secondly, a low noise amplifier using coplanar waveguides as an input-output matching network is analysed and achieves a gain of 15.7dB and input-output matching of -24 and -12dB respectively with noise figure of 1.5dB.

Key words— CMOS low noise Amplifier, Coplanar Waveguides, Rectangular Micro-strip antenna.

I. INTRODUCTION

Even though CMOS technology has been used in digital circuits and low-frequency analogy circuits for many years, it is only within the early nineteen that research has shown that CMOS is capable of being used in RF circuits. With the backend of transceivers already being implemented in CMOS, it is attractive to use in the RF frontend in order to integrate the receiver on a single chip. Low noise amplifier as the first block of the receiver wireless systems add a very low noise while it amplifies the received signal from the antenna to a desirable level over a relatively broad range of frequency. Low noise amplifier is a device which amplifies the weak signal captured by an antenna. It is necessary that the received signal be amplified earlier in the receiver chain, while adding as little noise as possible [1]. In an RF receiver, it is a challenge in the design of an LNA to simultaneously achieve the low noise figure and high gain. Also one of the necessary needs is to obtain the good input and output match. Differential Low Noise Amplifier for On chip Ultra Wide-Band Transceiver uses an inductively degenerated input stage that allows achieving minimum noise figure, matched input impedance and maximum transconductance gain for given current consumption [2].

In this world of wireless communication, Rectangular Microstrip patch antenna plays a vital role. Despite of having many advantages like omni-directional radiation pattern, low cost and low profile it has many disadvantages like that of low gain and narrow bandwidth which are targeted for improvement. The drawbacks of RMPA can be overcome by using metamaterial [6]. A 1.3GHz Cascode low noise amplifier based on 0.25µm CMOS technology has been successfully designed with achieved good NF of 1.42dB [3]. In this work, a cascade is added to the input stage to mitigate the interaction between the input tank and output tank that reduces the reverse gain through the amplifier, thus increasing the stability of the circuit, CPW lines has been adapted to achieve matching. This paper is also complimented with design of Rectangular patch antenna that is resonant at 10-20 GHz with micro-strip feeding and simulated in ADS tool.

II. ANALYSIS OF LNA AND RMSA

The main purpose of designing an LNA at 10-20 GHz is to achieve minimal noise figure, higher power gain, more efficiency and better linearity. But all these factors are in conflict with one another if any of the parameter is considered. As fulfilling these requirements of LNA design, different topologies like Inductive Source Degeneration, Common Gate etc. are there which are discussed here.

A Common gate amplifier structure has better input impedance than a common source structure. By carefully choosing the size

of the transistor and biasing conditions, the 50 Ω impedance matching can be easily obtained.

A 20GHz differential two-stage low-noise amplifier (LNA) is demonstrated in a foundry digital 130nm CMOS technology with 8 metal layers. A differential two-stage cascode amplifier topology with inductive degeneration at the source is used [4]. A fully integrated low noise amplifier with technique of source inductive feed-back achieves the goal of low noise and low Power dissipation for 5GHz wireless applications. A micro-strip line matching network was used for the impedance transformation for achieving higher output power and higher efficiency [5]. In this, CPW lines are used for better impedance matching as well as to utilize the maximum bandwidth available. LC network used in impedance matching achieves PAE up to 50% whereas if 50 Ω transmission line like micro-strip line, CPW line etc. are used then it is possible to achieve PAE of 80%. As compared to Micr-strip lines, CPW lines are less dispersive, reduced radiation loss. The gap in the coplanar waveguide is usually very small and supports electric fields primarily concentrated in the dielectric. The LNA usually only involves one or two transistors to achieve low noise operation. The performance of the LNA circuits is very dependent on process technology. CMOS technologies are the best choice to design an LNA because they offer high speed operation, simplicity in fabrication, and low power consumption.

DC bias point is one of the most important parameters which define the characteristic of the amplifier. Stability, input and output matching network designs are based on these s-parameters. The dc bias point defines the class of the amplifier. S-parameters basically characterize the amplifier. The micro-strip antenna is a small electrically antenna that has a number of advantages over the other antennas i.e. lightweight, inexpensive, and easy to integrate with active devices to improve the system reliability. In this, a rectangular patch antenna that is resonant at 10-20 GHz with micro-strip feeding and simulated in ADS tool. All the design work taken a FR4 substrate with thickness of t = 0.245mm at the height h = 10mil above a lossless ground conducting layer.

III. CIRCUIT DESIGN

In LNA design there is a trade-off between the best-input match and the lowest noise figure. The traditional topology of LNA with source inductor is used for its good performance on signal to noise ratio. Fig 1 shows schematic of low noise amplifier design at 10-20 GHz. Peak gain of 15.7 dB is obtained at 10-20 GHz from the XF response analysis in SP analysis and the gain fall to -3 dB of the peak at two different frequencies.

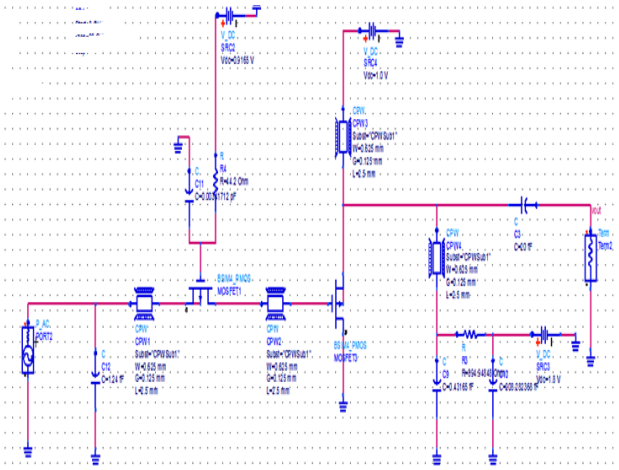

Fig.1: Schematic of LNA at 10-20 GHz.

The simulated peak gain curve of the amplifier from 10-20 GHz is shown in Fig.2. For maximum power transfer, the input of the wideband LNA should provide an impedance of 50Ω over the frequency band of interest. Again as this LNA will be succeed

by a mixer, its output impedance also should be 50Ω to match with the input impedance of the mixer.

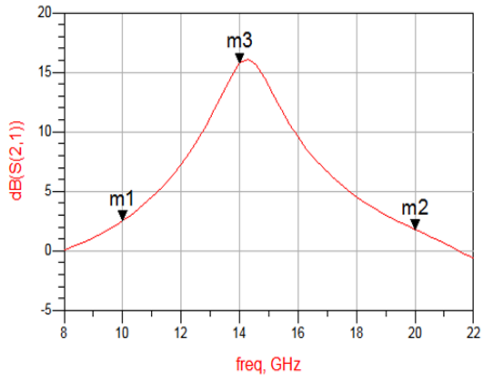

Fig.2: Forward gain Vs frequency

The best optimum result that this circuit predicts for the input reflection coefficient, S11 of -21 dB is shown in Fig.3. The simulation results for noise figure are shown in Fig. 4. The noise figure NF is 4.75 as input and 2.8 as output in scale at 35-45 GHz and in the operating bandwidth; the noise figure is less than 4 dB. The layout of the CG-CS LNA is shown in Fig.5. The chip area is 1.13 x0.86 mm^2. The circuit floor plan is well arranged to minimize the lengths of the interconnect lines in order to reduce the effects of the parasitic capacitance.

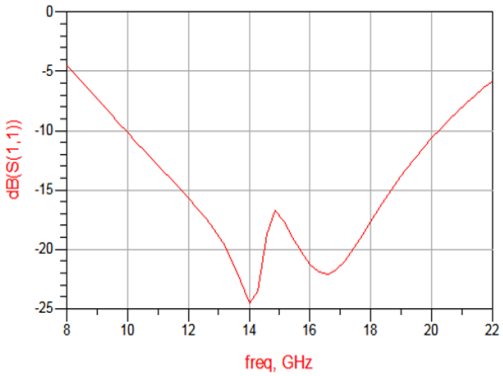

Fig.3: Reflection coefficient Vs frequency

The power consumption is 2.7 mW with 1 V bias voltage. It is shown that the CGLNA is capable of reducing the power dissipation and achieving good gain flatness at same time.

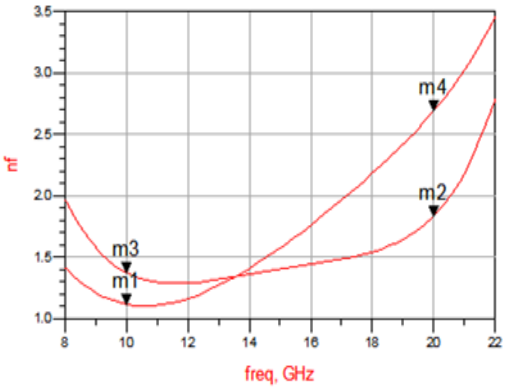

Fig. 4: Noise figure Vs frequency

IV. DESIGN CONSIDERATION OF THE ANTENNA

The micro-strip antenna is a small electrically antenna that has many advantages like lightweight, inexpensive and easy to integrate with active devices to improve the system reliability [9]. The proposed rectangular patch antenna is simulated in ADS platform. The 3D picture of patch antenna at 10-20 GHz is shown in Fig. 6. The proposed antenna achieves impedance bandwidth of 9 GHz from 35 to 44 GHz band range. The reflection coefficient of patch antenna is about -22dB with good radiation characterises.

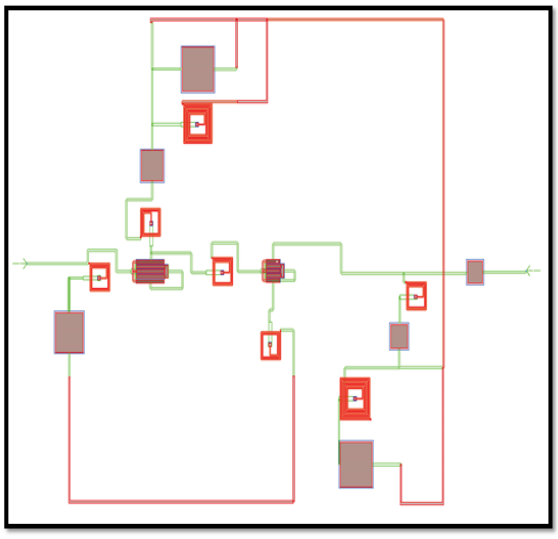

Fig. 5: Layout of CG-CS LNA.

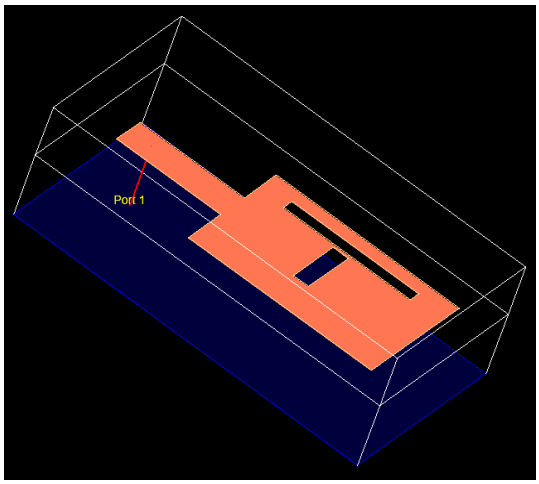

Fig. 6: 3D picture of patch antenna at 10-20 GHz

The 3D view of radiation characterises is shown in Fig 7. The current distribution view of patch antenna with bold arrows is shown in Fig. 8. Fig.9 shows the gain and directivity of patch antenna in polar plot form. The return loss of patch antenna is shown in fig.10.

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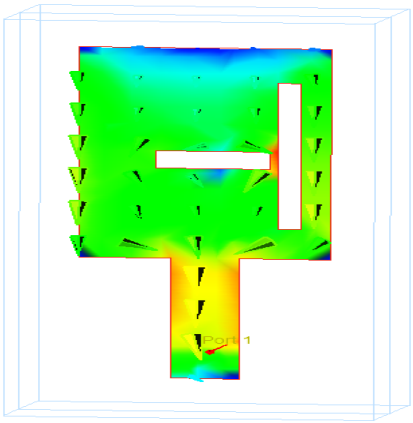


Fig. 7: 3D view of current distribution of patch antenna.

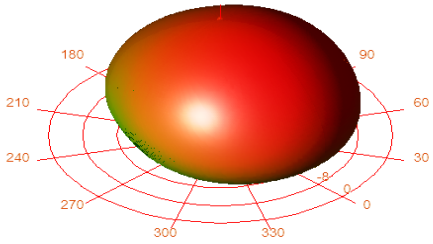


Fig. 8: 3D view of Maximum current distribution.

V. CONCLUSION

The single endede two stages Low noise amplifier are designed using 90nm CMOS process at 10-20 GHz band in this circuit.

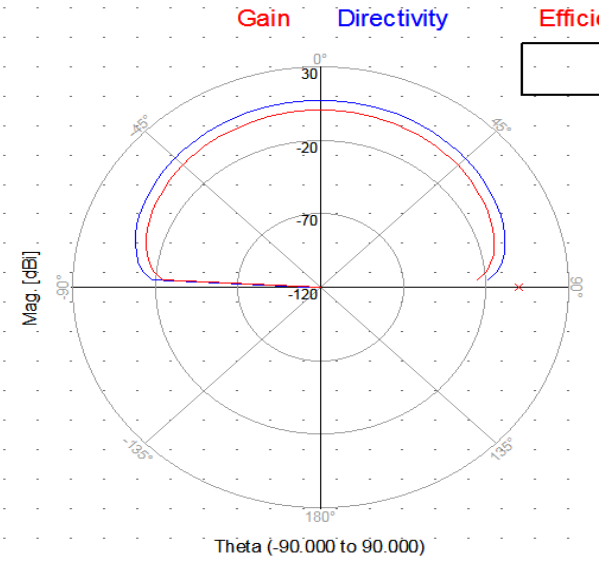


Fig.9: Gain and directivity of patch antenna.

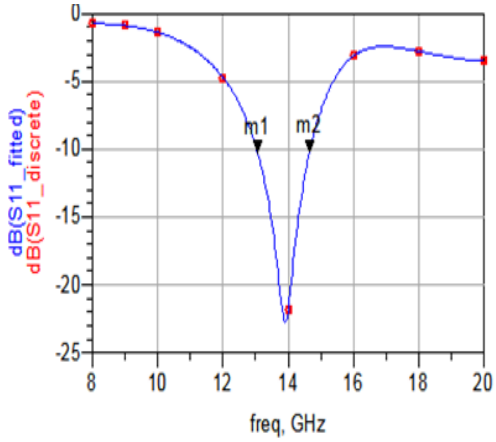


Fig.10: Return loss for patch antenna.

Performance parameters for LNA as well as patch antenna are met with this new design like Noise figure, peak gain and input-output matching of the circuit. Simulation results show that for LNA, the gain of 15.7 dB, noise figure of 1.5 dB and output matching of -12 dB is achieved. The proposed rectangular patch antenna is simulated in ADS platform and achieves impedance bandwidth of 9 GHz from 35 to 44 GHz band range. The reflection coefficient of patch antenna is about -22dB with good radiation characterises.

REFERENCES

[1] Alireza Zolfaghari, Member, IEEE and Behzad Razavi, Fellow, IEEE, "A low Pwer 2.4 GHz Transmitter / Receiver CMOS IC "Ieee Journal of solid state circuits, vol. 38, pp.177-181, february, 2003.

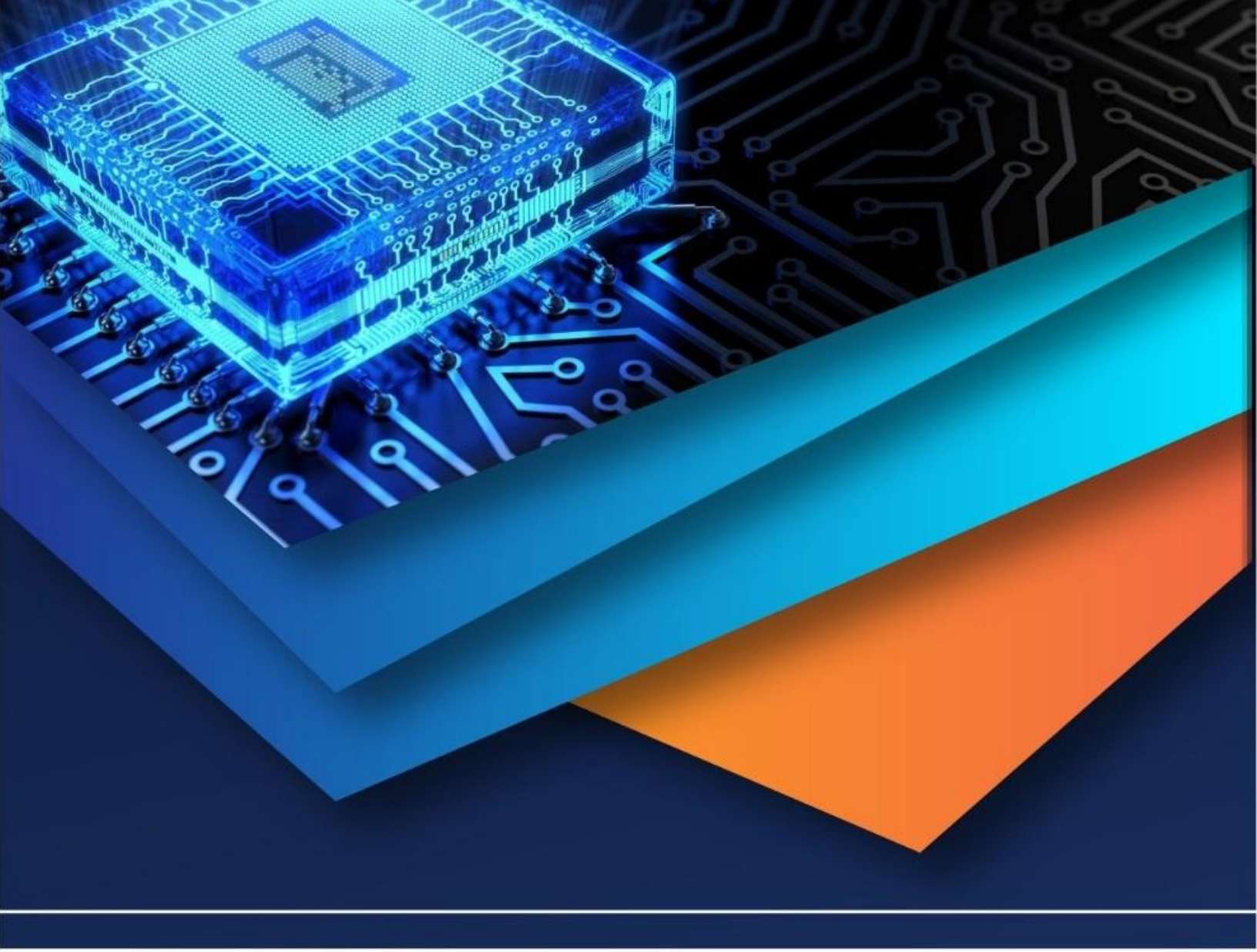
[2] Md. Ariful Haque et.al., 2006: "18.2 GHz Differential Low Noise Amplifier for On chip Ultra Wide-Band Transceiver".

[3] Ma Hongbo Feng et.al., vol.78, pp.123, 2000: "The Research Based on the Design of a 1.3GHz Cascode LNA".

[4] Xiaoling et.al., vol.15, pp.19, 2005: "A Power Efficient Differential 20-GHz Low Noise Amplifier With 5.3-GHz 3-dB Bandwidth".

[5] VasylyevA et.al., vol.69, pp.249, 2002: "A Monolithic 2.4 GHz, 0.13 µm CMOS Power Amplifier With 28 dBm Output Power And 48 % PAE at 1.2 V Supply".

[6] Rectangular Microstrip antenna loaded with symmetrical cut H hexagonal shaped metamaterial structure for bandwidth uimprovement at 1.79 GHz by Bhim Singh, Deptt. Of Electronics, International Journal of Advanced Technology & Engineering Research".



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