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AMBA AHB Design: A Review

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***Abstract:** In this paper, verification environment of AMBA AHB is presented by using system verilog. To replace complex bridges with the specific protocol block interface in SoC design AMBA protocol family is used. AMBA AHB is the communication bus protocol for a System on chip. AMBA AHB can be used in high clock frequency system modules. It acts as the high-performance system backbone bus. AMBA is basically single layer bus. The single layer AMBA AHB design has all the AMBA AHB signals or specifications. The paper also introduced various arbitration techniques of AMBA AHB.*
***Keywords:** AMBA, TDMA, SoC, AMBA AHB*

I. INTRODUCTION

An SOC may be a system that is taken into account as a collection of elements and interconnects among them. A SOC may include different Intellectual Property like memory, I/O peripherals and processors with different functionalities. These may vary in their speed and interconnection of these IP's will be important and it is done using SOC bus. The advanced microcontroller bus architecture was introduced by ARM Ltd in 1996.

As the level of style quality has become higher, SoC design requires a system bus with high bandwidth to perform the multiple operations in parallel. AMBA was given by ARM which provides different kinds of buses to be used in microcontrollers, SOC's and ASIC's. Due to high bandwidth AMBA protocol is best suited protocol for today's system. AMBA protocol is an open standard so that it can be tailored to any system's requirements. It is widely used in network interconnect chip, RAM controller, DMA controller, level 2 cache controller etc.

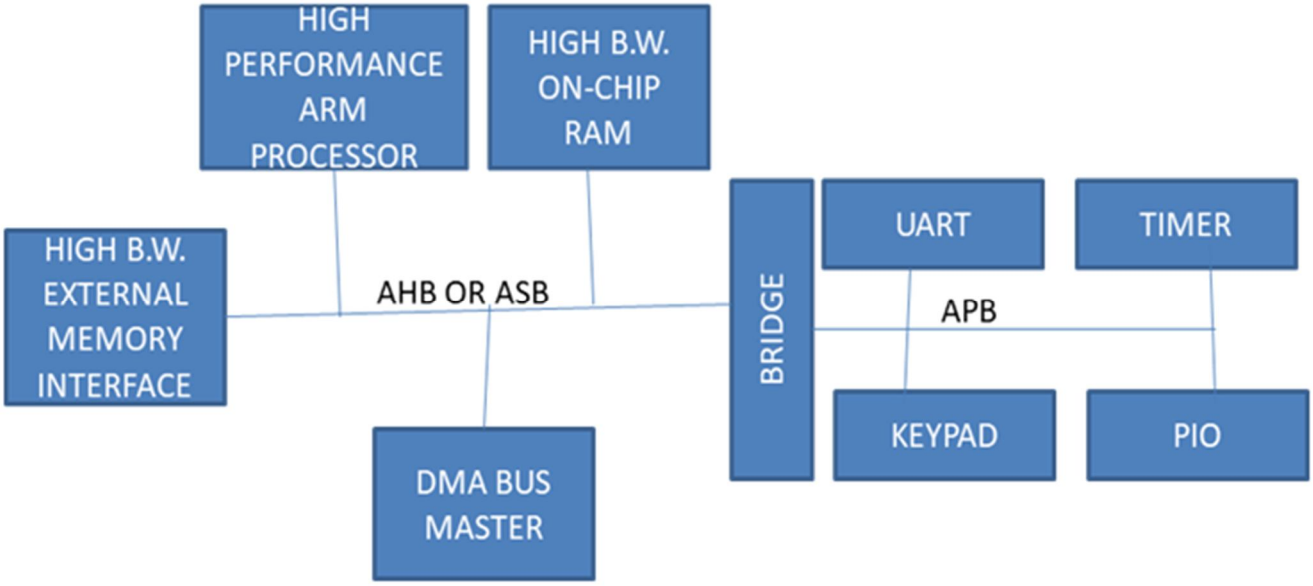

Fig 1. AMBA

A. *AMBA AHB Features*

1) High performance
2) Burst Transfer
3) Single edge clock operation
4) Address decoding
5) Large data bus width

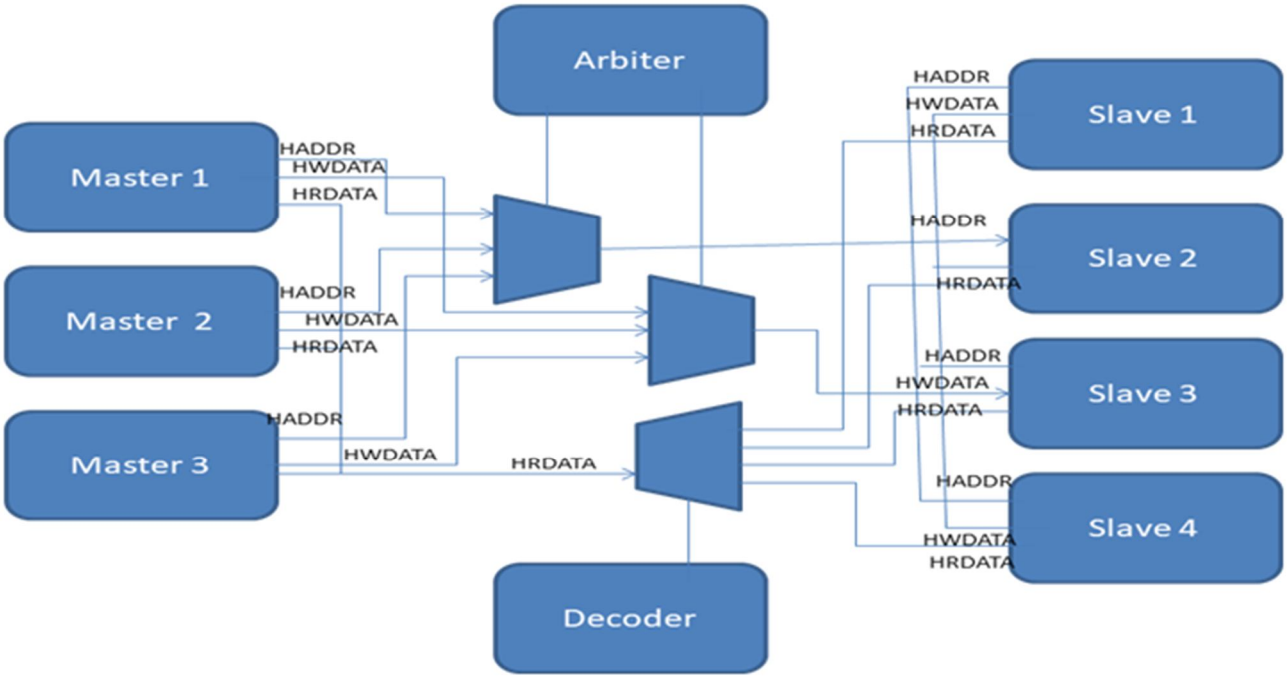

Fig 2.AMBA AHB Block Diagram

This paper is organized as follows. We discuss the comparison of various methodology of AMBA AHB. Next we explain the multichannel AHB. We also present the different arbitration techniques of AMBA AHB. Finally discuss the arbitration techniques in conclusion

B. Comparison of Various Methodology of AMBA AHB

Sr. No.	Authors	Paper Title	Proposed Methodology	Research Prospects
1	Han Ke, Deng Zhongliang, Shu Qiong	Verification of AMBA bus model using system verilog	Designing of reference model to dynamically predict the DUT behaviour.	A references model is used to verify SRAM and Flash controller. This model reduces the time consumption.
2	Shraddha Divekar, Archana Tiwari	Multichannel AMBA AHB with multiple arbitration techniques	Xilinx software is used to design AMBA AHB bus arbitration techniques and implementing by VHDL language using FPGA.	It provide interconnection scheme between multiple masters and slave. Interconnection busmatrix gives increase in bus bandwidth and flexibility.
3	Anurag Shrivastava, G.S. Tomar, Ashutosh Kumar Singh	Performance Comparison of AMBA Bus based SoC communication protocol	Case study of different AMBA SoC bus protocol.	Compare different AMBA protocols with their features and performance matrices.
4	Massimo Conti, Marco Caldari, Giovanni B. Vece, Simone Orcioni	Performance analysis of different arbitration algorithms of the AMBA AHB bus	Describe AMBA AHB by SystemC 2.0 SOFTWARE.	It give the system C and VHDL clock accurate model. This model is use to evaluate performance of the bus. It give result in reduction in power dissipation.
5	Marco Bertola, Guy Bois	A methodology for the design of AHB bus master wrappers	State machine is design by Mentor Graphics HDL Pro tool and simulation was done by Seamless CVE co-verification tool.	It gives the different steps for master wrapper and these steps or methodology can apply for other protocols

6	Rinku, Pawan Kumar Dahiya	Advance high performance bus arbitration techniques: A state of the art review	Defining the AMBA protocol with arbitration protocol.	Comparison of techniques gives that round robin arbitration technique is much better than the fixed priority and weighted round robin techniques.
7	Wang Zhonghai, YE Yizheng	Designing AHB/PCI bridge	RTL of AMBA bridge.	This describe model of AHB/PCI bridge at RTL level which is synthesized by synopsis software
8	Youngwoo Kim, Kyong Park, Myungjoon Kim	AMBA based multiprocessor system	Dual ARM processor cores with 0.18um.	It proposed no multiprocessing capabilities bus architecture. The bus architecture using dual ARM processor core with standard cell process.
9	Prakash Srinivasan, Adeoye Olugbon, Ali Ahmdinia,	Power Analysis of arbitration techniques for AMBA AHB based reconfigurable SoC	Using TDM and priority scheme of arbitration power is analysed .	It uses multi master under arbitration policies which gives the different features of each policy and strong correlation between power and effectiveness.
10	Prince Gurha, R.R. Khandelwal	SV assertion based verification of AMBA-AHB	To bind the assertion module uses BIND SV feature.	According to assertion based verification of AMBA AHB any one master can transfer the data at any one clock cycle.
11	Sreehari S, Jaison Jacob	AHB DDR SDRAM enhanced memory controller	Use Icarus verilog tool to synthesized.	To perform read and write operation necessary address and control signals are provided by memory controller. There is no loss of data. Using memory controller data and commands are transferred successfully.
12	Abhik Roychoudhary, Tulika Mitra, S.R. Karri	Using formal techniques to debug the AMBA SoC bus protocol	To detect a potential bus starvation scenario SMV model checker is used.	It represents experience in verification of SoC bus protocol. These use verification techniques which is useful in automatically detecting cases in protocol detection.
13	Soo-Yun Hwang, Kyoung-Sun Jhang	An improved implementation method of AHB bus matrix	Removal of input stage improved method of ML-AHB bus matrix is presented.	Verification techniques in the protocol specification as model checking are useful in automatically detecting suitable corner cases

C. Multi-channel AHB

The multi-layer/multi-channel AHB bus matrix is an interdependence scheme which is based on AMBA AHB protocol in which multiple masters and slave has parallel access path for data transaction. The multi-layer AHB uses slave side arbitration. Slave facet arbitration is completely different from master facet arbitration. After master provides a signal to the slave it wait for the response of the slave regarding the status for processing the data. Thus, AHB bus matrix has transferred based arbitration strategy only. Because of the arbitration strategy limitless of AHB bus matrix it may lead to system performance degradation. Several studies for the high performance bus has been recommended such as look up table based on cross bar arbitration, token ring arbitration etc.

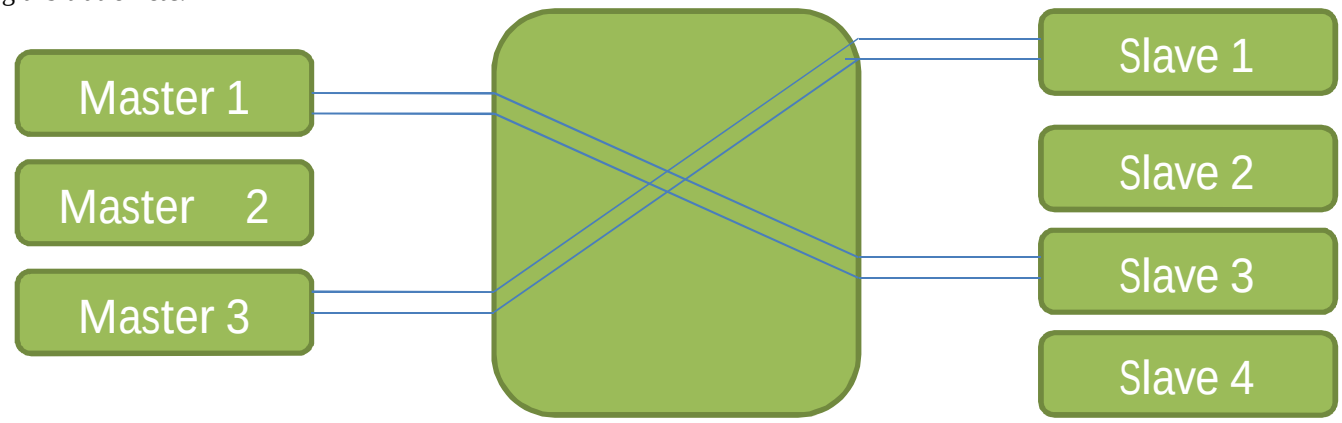

Fig 3. Block Diagram of Basic Multi-channel concepts

D. Arbitration Techniques

1) *Round Robin Technique:* In this mechanism the master who wants to send the data to slave first request to the arbiter for getting the access of the bus. The transfer of data with the highest priority changes in circulates fashion. If any masters do not want to access the bus then priority is transfer to the next priority master. So, in round robin technique access of the bus depend upon priority.
2) *Fixed Priority Technique:* In this technique all the master has fixed priority. If several masters are trying to access the same slave at same time then access of the bus is given to the highest priority master. It has low area cost, more flexibility and faster arbitration time.
3) *Dynamic Arbitration:* This mechanism is also depend upon priority level but after getting the access of the bus the master priority is reduced by 1.
4) *TDMA:* In this approach all the masters are given fixed time frames for transfer of data. If any master want more bandwidth can be given more time frame.

Table 1.Comparison of Techniques

Parameter	Round Robin	Fixed Priority	Dynamic	TDMA
Simplicity	Moderate	High	Low	Moderate
Cost	Moderate	Low	High	Moderate
Architecture	All masters have equal bandwidth	Shared Bus	Require more bandwidth	Require high and fixed bandwidth to all masters
Performance	Moderate	High	Low	High

II. CONCLUSION

This paper gives the discussion on design of AMBA AHB. The presented model is synthesized by QuestaSim and EDA tools software. For all transaction AMBA AHB uses rising clock edge. We analyze impact on power of the bus by different numbers of masters with different arbitration policies. Table 1 gives the comparison between arbitration policies.

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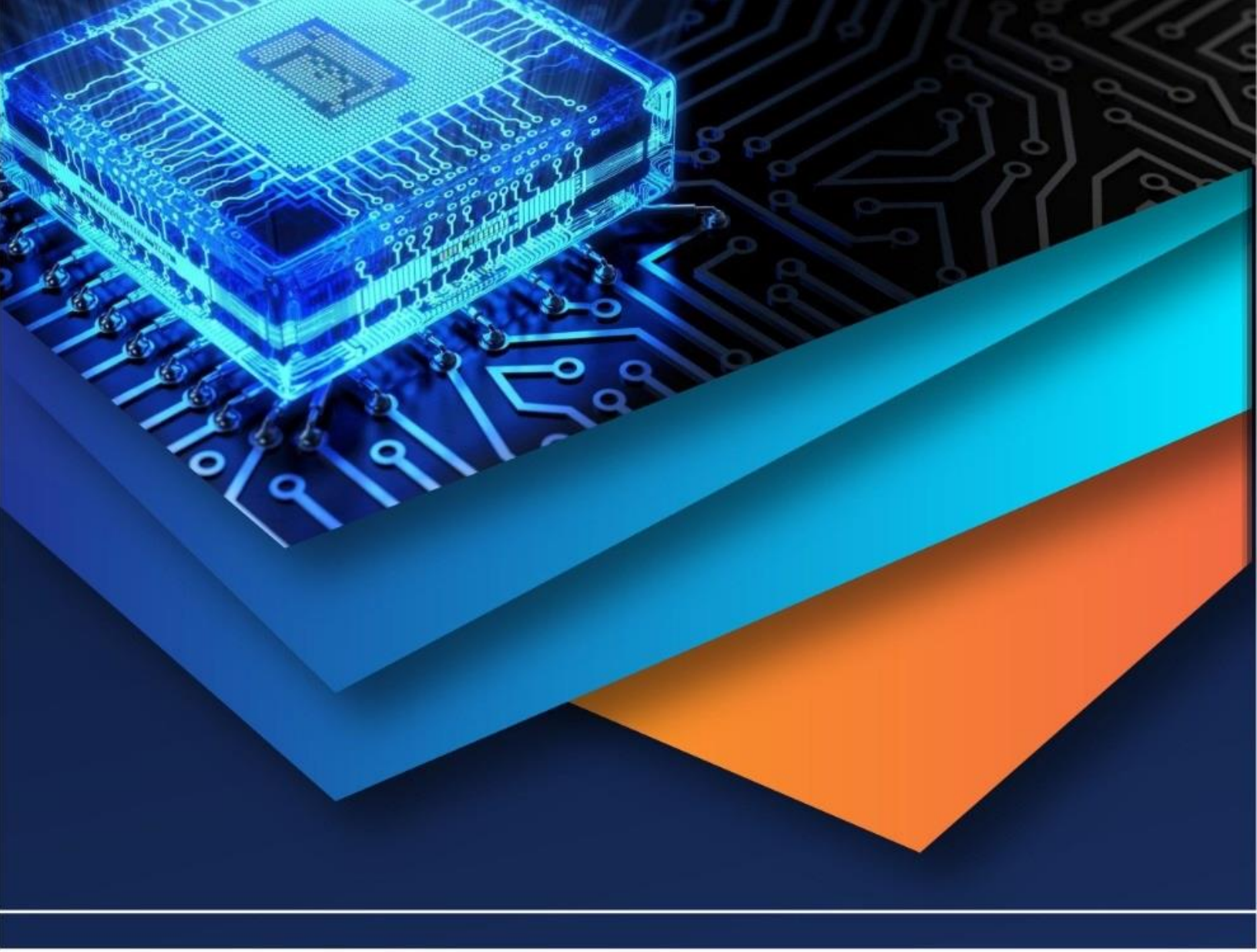

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