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Design of Single Ended 8T SRAM Cell using Sub threshold Logic

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Abstract: ***In this paper, a novel 8T SRAM cell is proposed which aims at decreasing the delay and lowering the total power consumption of the cell. The threshold voltage variations in the transistor and increased power dissipation increases with number of transistors which in turns affects the read and write stability of the cell. As the technology is being scaled down leakage power is becoming an important contributing factor in total dissipation of the circuit. The proposed 8T SRAM bit cell is designed using 65nm cmos, n-well technology with a supply voltage of 1.20V. The results have been obtained using cadence virtuoso tool. The experimental results show that the average delay has been improved by 80% compared to the conventional 6T cell. The total power is improved by 14.5% as compared to conventional 6T SRAM cell.***
Keywords: SRAM, Subthreshold, Low-power, CMOS logic.

I. INTRODUCTION

The portable microprocessor controlled devices contain embedded memory, which represents a large portion of the system-on chip (SoC). These portable systems need ultra low power consuming circuits to utilize battery for longer duration. The power consumption can be minimized using nonconventional device structures, new circuit topologies, and optimizing the architecture. Although, voltage scaling has led to circuit operation in sub threshold regime with minimum power consumption, but there is a disadvantage of exponential reduction in performance. The circuit operation in the sub threshold regime has paved path toward ultra low power embedded memories, mainly static RAMs (SRAMs). However, in sub threshold regime, the data stability of SRAM cell is a severe problem and worsens with the scaling of MOSFET to sub nanometer technology. Due to these limitations it becomes difficult to operate the conventional 6-transistor (6T) cell at ultra low voltage (ULV) power supply. In addition, 6T has a severe problem of read disturb. The basic and an effective way to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation. This read decoupling approach is utilized by conventional 8-transistor [read decoupled 8-transistor (RD-8T)] cell which offers read static noise margin (RSNM) comparable with hold static noise margin (HSNM). However, RD-8T suffers from leakage introduced in read path. This leakage current increases with the scaling thereby, increasing the probability of failed read/write operations.

1) *SRAM Operation:* An SRAM cell has three different states: standby (the circuit is idle), reading (the data has been requested) or writing (updating the contents). SRAM operating in read mode and write modes should have "readability" and "write stability", respectively.

II. LITERATURE SURVEY

A. *Power Reduction using Single Ended 8T SRAM Cell with Technique*

Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence but it is still volatile in the conventional sense that data are eventually lost when the memory is not powered. In this paper, a new 8T SRAM cell, which employs a single bit line scheme to perform the write and read operations, is proposed. This scheme enhances the write ability and read stability by cutting off the feedback loop of the inverter pair, there by eliminating the read and write constraints on the transistor dimensions.

SRAM based structures within the processor are especially liable to as one of the PMOS devices in the memory cell always has an input “0”. So in order to reduce the power consumption, an inverter is connected to the other end of NMOS device, such that the inverter replaces the ground. Now the size may be somewhat increased but the power leakage is controlled by the use of the inverter.

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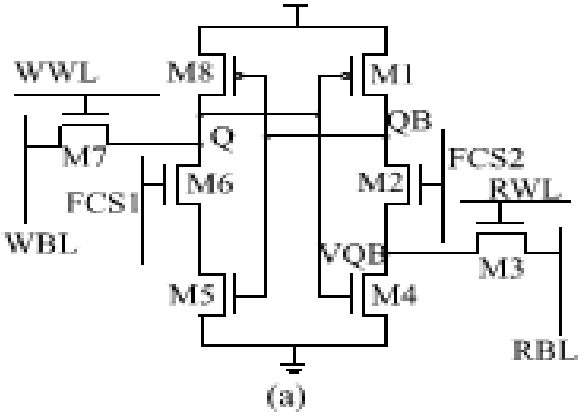
III. PROPOSED 8TSRAM CELL

To make a cell stable in all the operations, a single-ended 8t sram cell using subthreshold logic is represented .



Proposed 8T.Schematic.

The single-ended design is used to reduce differential switching power during the read–write operation. The power consumed during switching or toggling of data on a single bit line is lesser than that of differential bit-line pair. This enables writing through single nMOS in the 8 transistors. It also separates read and write path and exhibits read decoupling. The structural change of a cell is considered as to enhance the immunity against the (PVT) process–voltage–temperature variations.

A. Write Operation.

The feedback cutting scheme is used to write in 8T. In this , during write1 operation feedback control signal (FCS1) is made as low which switches OFF M6. When the read word line (RWL) is made low and FCS2 high, M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to word bit line (WBL) is 1 and write word line (WWL) is activated then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. Moreover, when Q changes its state from 0 to 1, the inverter (M1–M2–M4) changes the state of QB from 1 to 0. To write a 0 at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can go to a small negative value, and then the current from pull-upp MOS M1 charges QB to 1. The WT is measured as the time taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other.

During write 1/0 operation, the power consumption of 8T is highest for fast nMOS and fast pMOS process corner dominated by the fast switching activities. As write 0 operation is faster than write 1, the write 0 power consumption during write 0 is more as compared with that of write 1.

B. Read Operation

The read operation is performed by precharging read bit line (RBL) and activating read write line (RWL). If 1 is stored at node Q then the M4 turns ON and makes a low resistive path for the flow of a cell current through RBL to the ground. This discharge RBL quickly to the ground, which can be sensed through the full swing inverter sense amplifier. Since WWL, FCS1 and FCS2 were made low during read operation, therefore, there is no direct disturbance on the true storing node QB during reading the cell. The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original 0 value after successful read operation. If Q is high then, the size ratio of M3 and M4 will govern the read current and the voltage difference on RBL. During read 0 operation, Q is 0 and RBL holds precharged high value and the inverter sense amplifier gives 0 at output. Since M2 is OFF so virtual QB is isolated from QB and this prevents the chance of disturbance in QB node voltage which ultimately reduces the read failure probability and improves the read static noise margin (RSNM). During read operation, if FCS1/FCS2turns 1 before RWL is turned 0 then QB and VQB can share charge. As WWL is 0 no strong path exists between WBL and Q ,and any disturbance in QB will not affect Q. After that if RWL goes low, the positive feedback will restore the respective states(Q=1andQB=0).

The pulse width needed for write operation is very small as compared with the data retention time (in microseconds) of half-selected cells while, FCS2 is OFF to write 0 in selected cell. During read operation, FCS1 and FCS2 go low in whole column and QB of column half-selected cell will be floating for read period.

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OPERATION TABLE OF PROPOSED 8T SRAM CELL

	Hold	Read	Write '1'	Write '0'	Row half-selected		Column half-selected	
					Write	Read	Write	Read
WWL	'0'	'0'	'1'	'1'	'1'	'0'	'0'	'0'
RWL	'0'	'1'	'0'	'0'	'0'	'1'	'0'	'0'
FCS1	'1'	'0'	'0'	'1'	'1'	'1'	'1'	'0'
FCS2	'1'	'0'	'1'	'0'	'1'	'1'	'0'	'0'
WBL	'1'	'1'	'1'	'0'	'1'	'1'	'1'	'1'
RBL	'1'	Dis-charge	'1'	'1'	'1'	'1'	'1'	'1'

Proposed Table

IV. DESIGN IMPLEMENTATION

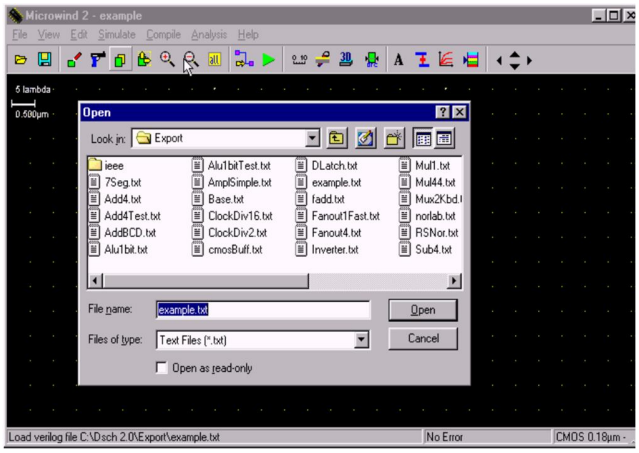
A. *EDA Tools*

Microwind is a truly integrated EDA software enclosing IC designs from concept to completion, authorise chip designers to design beyond their imagination. microwind integrates traditionally separated front-end and the back-end chip design in an integrated flow, accelerating the design cycle and reduced design complexities. It tightly amalgamates mixed-signal execution with the digital implementations, circuit simulations, transistor-level extractions and verification providing an innovative education initiative to help the individuals to evolve skills required for design positions in effectively every domain of IC industry.

1) *DSCH (Schematic Editor and Digital Simulator)*: The DSCH program is a logic editor and simulator. DSCH is used to accept the architecture of logic circuit before the micro electronic design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and affirmation of the complex logic structures. DSCH also features the symbols, models and assembly support for 8051 controllers. Designers can create logic circuits for interfacing with these controllers and also verify the software programs using DSCH.
2) *Three levels of design in Microwind and DSCH:* The specifications ,we are going to see will be different for different foundry and technologies.

a) Design Examples: NOR Gate
b) Logic Design
c) Circuit Design
d) Layout Design

3) *Microwind / DSCH NOR Example: Circuit Design:* Open layout editor window in Microwind. Click *File ->Select Foundry* and select *X.rul*. This sets your layout design in the X technology. Click on the *Compile ->Compile Verilog File*. An *Open* Window appears, Select the .txt verilog file which we saved before and open it.



a) Advantages

i) Low power consumption
ii) Simplicity—a refresh circuit is not needed
iii) Reliability

b) Disadvantages

i) Price
ii) Capacity

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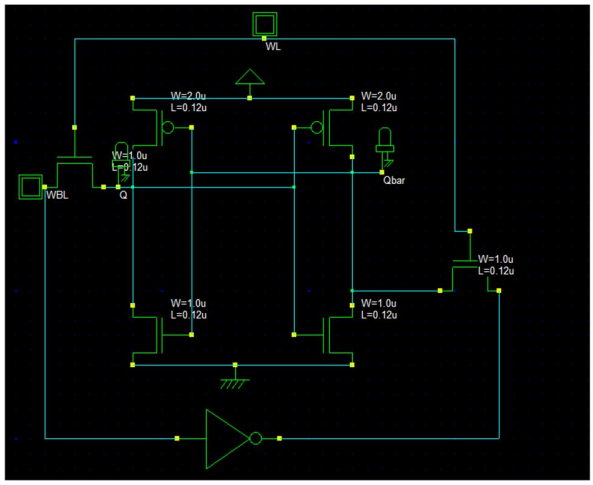
V. RESULTS

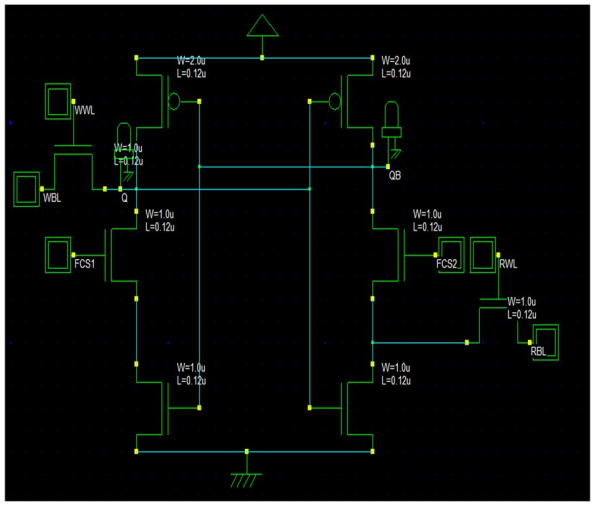
A. Layout Design

1) 6T SRAM Cell



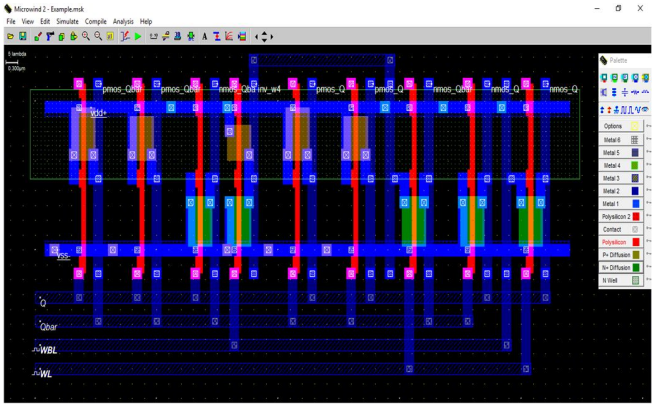
6T Layout Design

2) 8T SRAM Cell



8T Layout Design

3) Schematic Cell



6T Schematic Design

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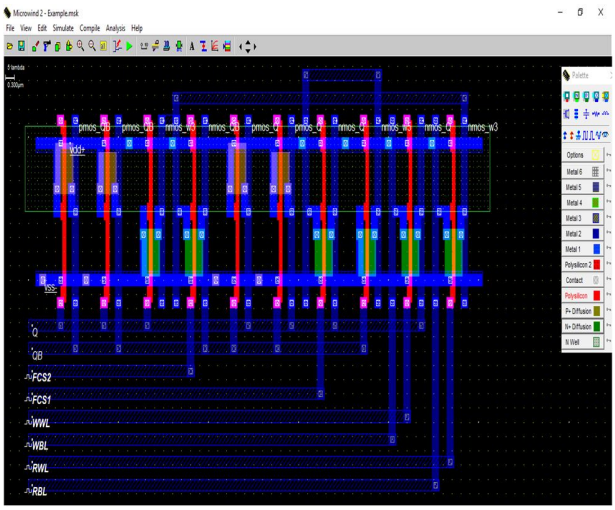

8T Schematic Design

VI. CONCLUSION

An 8T SRAM cell with high data stability (high is μ and low is σ)that operates in ULV supplies is presented. We achieved enhanced SNM in sub threshold regime using SE-DFC and read decoupling schemes. The proposed cell area is twice as that of a 6T. Still, it is better built-in process tolerance and dynamic voltage applicability. The proposed 8T cell has high stability and can be operated at ULV of 200 to 300 mV power supplies. The advantage of reduced power consumption of a proposed 8T cell enables it to be employed for battery operated SoC design.

Future and applications of the proposed 8T cell can be potentially low/ULV and medium frequency operation like neural signal processors, sub-threshold processors, wide-operating-range IA-32 processors, fast Fourier transform core, and low voltage cache operations.

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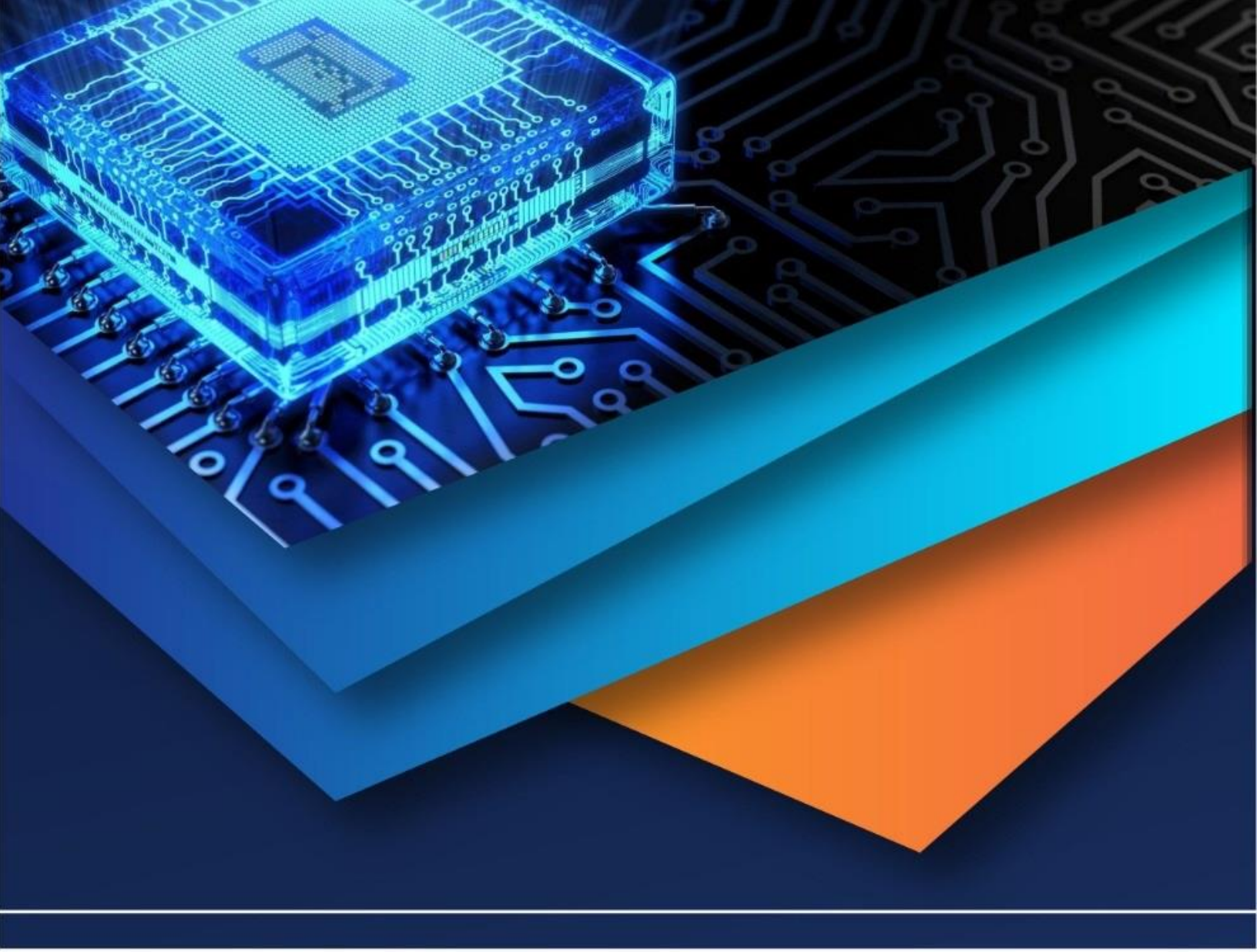

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