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Comparative Design and Analysis of Bio-Inspired Neural Sensing Amplifier for Neural Acquisition System (EEG)

Surya Prabha Rathore[1], Vijendra K. Maurya[2], Jubin Jain[3]

[1]Research Scholar, RTU Kota,

[2]Associate Professor GITS, Udaipur

[3]Production Engineer Black Lopper LED

Abstract: This paper exhibits the comparative design of front end analog amplifier for neural acquisition system, neural amplifier employed for recording of neural signals involves in the measurement of weak neural potentials or spikes, performance of whole recording system is affected by performance of neural amplifiers. The precise response of neural amplifier is contaminated due to the coupling of noise signals with signal of interest, which proves to be limiting factor. The comparative design of neural amplifier is presented based on two different architectures as CMFB OTA and DTMOS based VDTA in order to compare the performance parameters to obtain the best suited design for neural amplifier which positively satisfies the design parameters of neural amplifier such as noise, power dissipation, CMRR,PSRR & Gain. Based on comparative analysis, CMFB OTA exhibits the best suited results which are implemented in 0.35µm with gain of 63.89dB, noise 100uV/√Hz, NEF 3.0, power dissipation of $1.00*10^{-10}$W, CMRR as 110dB and PSRR as 81dB.

Index Terms: Low voltage signals, Low power consumption, High gain, Bio-Medical Interface (BMI),Low Noise Architecture, Weak Neural Signals, DTMOS, CMFB, OTA, VDTA.

I. INTRODUCTION

Neural potentials or spikes is responsible to carry the vital information about the neural activities of patient which enables the clinicians or doctors to diagnose and helpful to provide the desired treatment of disease such as brain injuries as well neural disabilities like epilepsy and Parkinson's disease. Neural signals posse's different amplitude and frequency characteristics. Neural signals are basically classifies in two categories includes neural spikes and local field potentials. Neural spikes produced by the neurons categorized in the frequency range of 300Hz – 5kHz, amplitude of neural signal comes under the range of 1µV and 100µV. There is need to bring the improvement in the healthcare quality as a result proper signal acquisition system is needed which proves to provide precise results for variety of neural signals lying under various amplitude and frequency range. In order to attain the desired performance of acquisition system, quality of neural signals recorded are required to be improved which is highly dependent on noise which proves to be limiting factor. A low noise or neural amplifier is equipped at the primary stage of receiver. Low noise amplifier is the predominant part for recording good quality of neural signal sensing system to process and analyze low voltage signals. Commonly used non-invasive method to record the neurological activities by employing electrodes on scalp is Electroencephalogram (EEG).

Neural acquisition system block diagram is shown in figure 1.Interfacing circuitry with the nervous system is considered to be the difficult task. The regular advancement in the field of neural interfacing has enhanced the proper understanding of central nervous system which has enabled to develop potentially therapeutic and prosthetic applications.
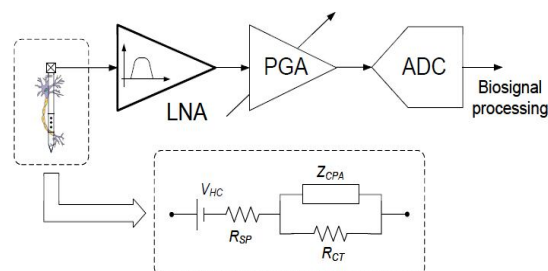

Figure 1: Block Diagram of Neural Signal Acquisition

In this paper we have designed neural amplifier (LNA) which is highly efficient in terms power consumption, gain, CMRR and noise, considered as important design parameters of amplifier. Power consumption optimization, in neural prosthesis power consumption is exhibited as important concern in order to avoid excessive heating of neural tissues which may cause the damage. Improved low voltage detection of neural bio-potentials obtained from microelectrodes in order to interpret the neural signals properly to analyze the neural disorders in desired way. Noise, the recorded neural signals posses' weak amplitude in few milli-volts and micro-volt so noise signals may get coupled with the neural signals and corrupt the signals in order to avoid this problem noise immunity is improved.

II. DESIGN OF FRONT END ANALOG NEURAL AMPLIFIER

A. Characteristics of Neural Amplifier

Amplifier should be capable to produce enough gain in order to provide signal quality as well high order of PSRR and CMRR is needed. The value of Noise efficiency factor should be set in between 2-6 for such application. The action potentials associated with the neural cell membrane is about 100mV, so gain should at least be maintained nearly at 40dB.Input impedance should be high. In order to achieve the, maximum transfer of the neural signal, input impedance should be high of the analog interface. CMRR should be high enough to reject the common mode interferences. The rejection can be achieved by making use of differential type amplifier. Mismatches are responsible for the degradation of CMRR. Low noise response required in order to obtain the high quality neural signal. Low power dissipation is desired.

B. Introduction to Neural Signals

There are basically two types of extracellular neural signals classified as Neural Spikes and Local Field Potentials (LFPs). Spikes are considered as digital events; spikes are produced by neurons of similar amplitude and durations and timing of spike contains the encode information about neurons. There are millions of neuron firing in the brain happens whose combined effect is LFPs which are responsible to carry information about CNS which can be easily recorded and analyzed to obtain certain neurological disorders.

Action potentials are considered as the basic signal waveform which mediates transfer of information in neural cells as shown in figure.2, occurrences of these action potentials in neural cell membrane is due to reverting action of polarization or depolarization.
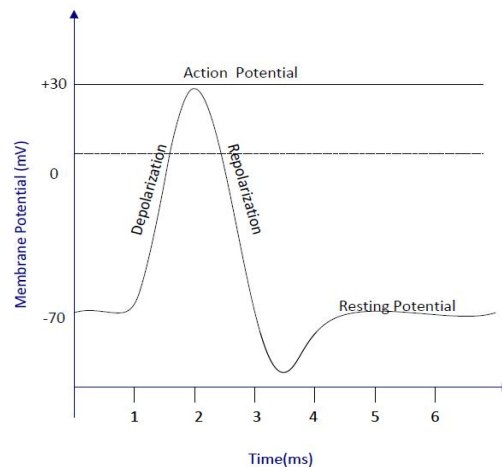

Figure 2: Membrane potential of neurons

C. Noise in Op-amp

The minimum level of signal is limited by the noise effect, which can be processed by the circuit. Noise is a basic problem reason is that it trade-off between various parameters power dissipation, linearity and speed of the circuit. The analog signals which are to be processed by the analog circuits can be corrupted by two different types of noise one is noise from electronic devices and other is environmental noise. Basically there are two types of noise one is thermal noise and flicker noise. Thermal noise is exhibited by MOS transistors. Noise is significantly generated in channel. An interesting phenomenon is observed in the interface existing between gate oxide and silicon substrate of the MOS. At the end of the interface in silicon crystal there exists a dangling bond which is responsible to provide rise in the energy states known as flicker noise.

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D. VDTA based Neural Amplifier using DTMOS

In order to meet the requirements of high power efficiency and low supply voltage in bio-inspired analog circuitry. The concept of DTMOS is exhibited, which is capable to operate in low voltage, do have low power dissipation and the leakage level is also low.DTMOS structure is obtained by making connection between the gate and body of MOS by which the threshold voltage is dynamically changed which can be illustrated by the relation as shown in equation.1 and circuital symbol of DTMOS is shown by figure 3.

$$V_{TH}=V_{TO}+\gamma(\sqrt{\phi}+V_{SB}-\sqrt{\phi_0}) \dots\dots\dots\dots\dots (1)$$

Zero bias threshold V_{TO} is given by equation.2:

$$V_{TO}=V_{FB}+\phi_{0+}\gamma\sqrt{\phi_0} \dots\dots\dots\dots\dots(2)$$

Flat band voltage (V_{FB}) and body effect is given by equation 3:

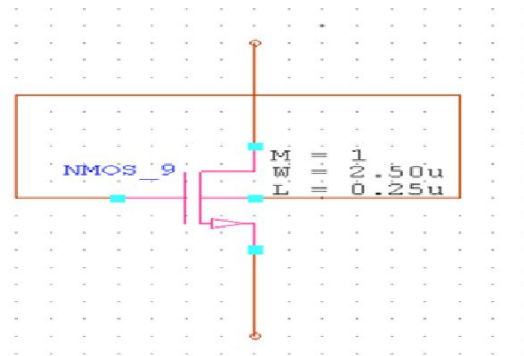$$\gamma=(\frac{\sqrt{2q\xi siNA}}{Cox}) \dots\dots\dots\dots\dots\dots(3)$$

Figure 2: Circuital Symbol of DTMOS

The implemented circuit shown in figure.4, based on bio-inspired architecture, DTMOS efficiently handle lower voltage levels along with low power consumption and as in case of neural signal acquisition system frequency of neural signals are not so high as a result this design proves to be fit. The design is composed of cascading two operational trans-conduction amplifiers.

The first stage of op-amp is composed of transistors PMOS_3,PMOS_4,PMOS_5,PMOS_1,PMOS_2,NMOS_2,NMOS_1,NMOS_4,NMOS_3 and the second stage of OTA is composed of PMOS_8,PMOS_9,PMOS_10,PMOS_6,PMOS_7,NMOS_7 and NMOS_8 where the DTMOS stage is composed of PMOS_3,PMOS_4,PMOS_5,PMOS_1 and PMOS_2 and the second part of DTMOS is consist of PMOS_6,PMOS_7,PMOS_8,PMOS_9,PMOS_10.

DTMOS do have ideal threshold voltage V_T that efficiently swings under voltage range of V_{DD}. An additional circuitry is prevented by biasing voltage at $V_{b1}=V_{b2}=V_{b3}=V_{b4}=0$ volts. Mirror pairs formed by using the transistors NMOS_3 and NMOS_2. NMOS_3 is responsible to supply biasing currents to the transistors PMOS_1 and PMOS_2. Currents mirror pairs are NMOS_2 and NMOS_3 as well NMOS_1 and NMOS_4. V_{b2} is the biasing voltage which can be changed in requirement to adjust the biasing current of OTA.

With respect to the mode of operations the drain current can be given by the equation 4, trans-conductance can be given by equation 5 and active MOS trans-conductance can be given by equation 6.

$$I_d=I_s(\frac{W}{L})e^{q(Vgs-Vth)/nkT}[1-e^{-q(Vds/kT)}] \dots\dots\dots(4)$$

$$G_m=\frac{q}{nkT}I_d \dots\dots\dots\dots\dots(5)$$

$$G_{PMOS\_3}=\frac{gPMOS\_2}{gNMOS\_8}g_{NMOS\_4}=G_{PMOS\_4}=\frac{gPMOS\_7}{gNMOS\_5}g_{NMOS\_8} \dots\dots\dots(6)$$

The schematic is implemented using 0.18 micron technology, from the simulation waveform shown in figure.5 it can be observed that the input signal is provided through MOS V_p and V_n, The neural signal picked up by the input stage amplifier is 100uV and it is amplified to 91.6mV which will be further processed by the signal conditioning circuitry. The circuit is operated by the supply of +0.2 volts and -0.2 volts only.
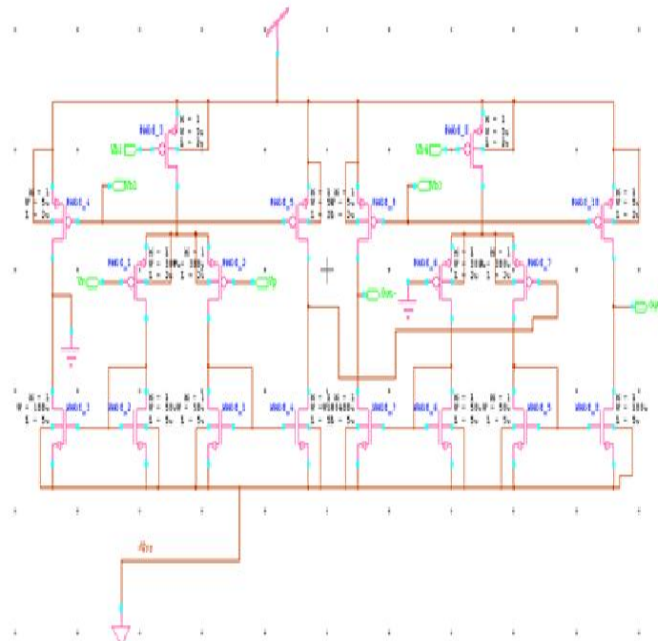
Figure 4: Schematic Implementation of VDTA using DTMOS

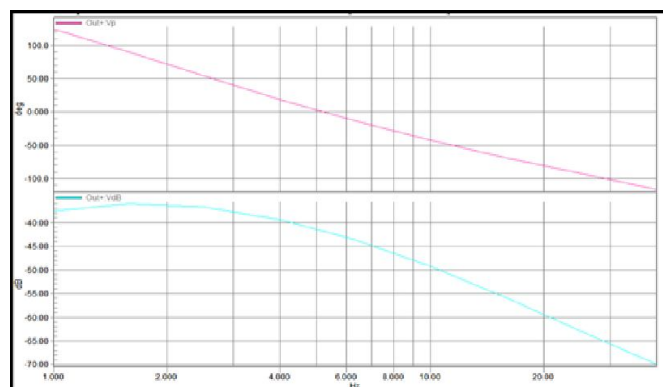Figure 5: Simulation Waveform of Neural Amplifier VDTA using DTMOS

Figure 6: AC response of Op-amp (a).Magnitude Response (dB) (b).Phase Response (Deg)
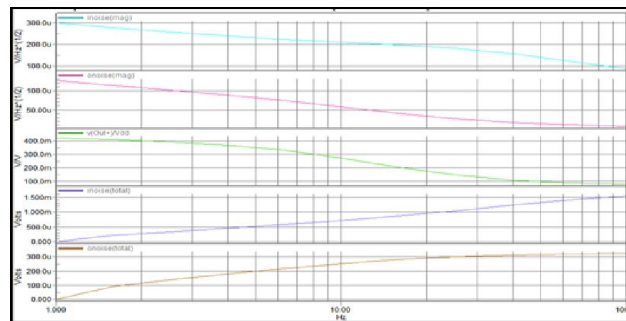
Figure 7: Noise Analysis Response of Neural Amplifier (Using DTMOS Technique)

E. Neural Amplifier Using Common Mode Feedback architecture

A common mode feedback (CMFB) with the fully differential architecture provides high value of noise rejection ratio. A common mode voltage V_{OCM} is provided at the input in designed circuit shown in figure.8, based on this common mode feedback is generated which provided back to the LNA block. In order to attain good recording of neural signals it is necessary to obtain good noise performance, main sources of noise are thermal noise and flicker noise.

It is although difficult to determine which transistor op-amp proves to be dominant source of noise, a thumb rule for inspection is that change voltage of gate (V_{GS}), each MOS by small amount and determine the effect of noise.

Effect of noise is negligible on the cascode devices, at lower frequency range. The noise controlling MOS in the telescopic op-amp using CMFB is PMOS_3 –PMOS_4 and NMOS_1-NMOS_2. Contribution of noise exhibited by PMOS_3 and PMOS_4 is same, as a reason sizing of the MOS from left to right branch is done similar. The same fundamental is for the MOS NMOS_1-NMOS_2. The flicker noise associated with the PMOS is less in comparison to the NMOS.

Input referred noise is mainly contributed by the PMOS_3 and PMOS_4 as a reason it is desired to select the PMOS as PMOS_3 and PMOS_4 in order to eliminate the flicker noise. In accordance to the equation…when the flicker noise is low the W/L ratio of NMOS_1 and NMOS_2 should be set smaller than in comparison to PMOS_3-PMOS_4.

The critical for the neural recording applications is the gain of the amplifier, so the gain of the amplifier can be given by equation 7:

$$A_V = g_{PMOS\_3}[g_{PMOS\_1}r_{o1}r_{o3} \| g_{NMOS\_3}r_{oNMOS\_3}r_{oNMOS\_1}] \ldots\ldots\ldots(7)$$

Output resistance of MOS is given by r_o in equation 7.In order to attain the good linearity of an amplifier a high gain is desired. In order to obtain high gain and low noise value sizing of W/L ratio is considered as important constraint. In order to obtain the common mode output voltage it is needed to set V_{CMFB} at the required voltage. The design of telescopic amplifier using CMFB is illustrated in figure.8, with the reference to schematic current is produced together with the MOS NMOS_11 and NMOS_12 which based according to the V_{OUT+} and V_{OUT-}.

The mirrored current I_{PMOS_7} tends to be compared with the current developed at NMOS_9 and NMOS_10 which is I_{OCM}. The same current is desired in the current branches of current mirror. Consequently the size of transistor chosen is same as same for the transistor NMOS_9 to NMOS_12. Same followed will same for the MOS PMOS_7-PMOS_8.

The common mode voltage that is obtained from the V_{OUT+} and V_{OUT-} matches with V_{OCM}, the value of current I_{PMOS_7} and I_{OCM} will become same as result the value of V_{CMFB} will be fixed.

In case, if the common mode voltage is larger in V_{OUT} node than the V_{OCM} as a result the value of I_{PMOS_7} will be greater than the I_{OCM} which will reduce the value of V_{CMFB}. The V_{OUT} will tend to decrease until the value becomes same that of V_{OCM}. Te same procedure will be repeated when the $V_{OUT} < V_{OCM}$ due to raised levels in V_{CMFB}. In accordance to the biasing voltage sizing of the transistors were determined.

The noises associated with telescopic circuit such as total input-referred noise, thermal and flicker noise can be given by equation.8 and equation.9.

$$V_n{}^2 = 4kT\left(2*\frac{2}{3g_{m}\,PMOS\_3,4} + 2*\frac{2g_m\,NMOS\_1,NMOS\_2}{3g_{m2}\,PMOS\_3,PMOS\_4}\right) \quad \ldots\ldots\ldots(8) \qquad V_n{}^2 = 2\frac{K_p}{(WL)_{1,2}\,C_{ox}\,f} + 2\frac{K_n}{(WL)_{7,8}\,C_{ox}\,f}\frac{g_{2m}\,NMOS\_1,NMOS\_2}{g_{2m}\,PMOS\_3,PMOS\_4}$$

……(9)

In mentioned thermal noise equation.8, Boltzmann constant (K), Temperature (T) and the trans-conductance is denoted by g_m. Similarly in flicker noise equation.9 W/L are the width and length of MOS, Oxide capacitance of MOS (C_{ox}), Working frequency of op-amp is *f* and flicker noise of NMOS and PMOS is denoted by K_N and K_P.

The neural signals obtained from the subject are weak in amplitude, weak signal amplitude is applied to the positive input of op-amp (in+) which is in range of 100uV and hence amplified signal is in range of 156.7mV shown in figure (9).The topology is operated at 3.3.volts and designed in 0.35 micron technology. The AC response plot is illustrated in figure (10) and Noise analysis is shown in figure 4.8, in which magnitude of input noise (inoise), output noise (onoise) and total noise (totnoise) is represented.
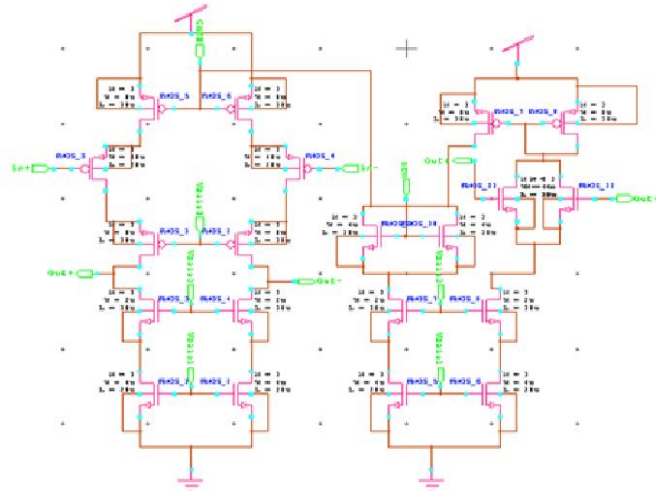

Figure.8: Schematic Implementation of bio-inspired telescopic amplifier using CMFB Technique

Figure.9: Simulation Waveform of Neural Amplifier Telescopic Amplifier using CMFB Technique
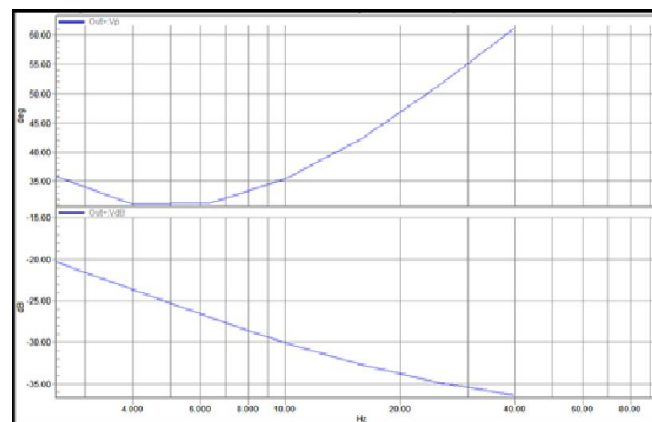

Figure 10: AC response of op-amp (a). Magnitude Response (dB) (b).Phase Response (Deg)
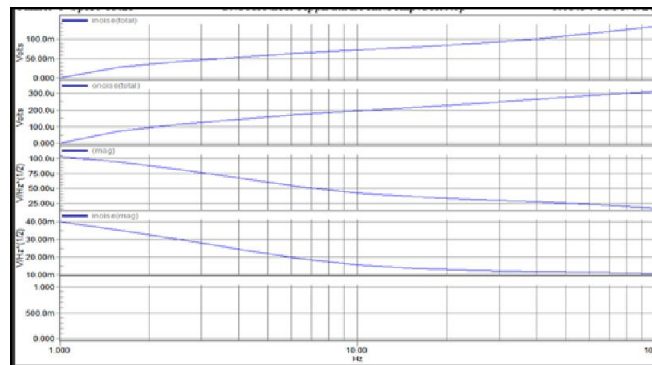
Figure 11: Noise Analysis of Neural Amplifier (Using CMFB)

F. Analysis of Performance in between both Architectures

Table 1: Comparison Between Various Parameters

S.No	Parameters	Units	Simulated Results	
			Neural Amplifier: VDTA Using DTMOS	Neural Amplifier: Telescopic Amplifier using CMFB
1.	MOS Technology	nm	0.18	0.35
2.	Supply Voltage	V	1.8	3.3
3.	DC Gain	dB	59.23	63.86
4.	Phase Margin	degree	80	60
5.	NEF	NA	4.8	3.0
6.	CMRR	dB	65	110
7.	PSRR	dB	22.40	81
8.	Noise	V/√Hz	400m	100u
9.	Power Dissipation	W	2.61×10^{-09}	1.00×10^{-10}
10	Current	A	295f	50n
11	GBW	Hz	273k	468k
12	Input referred Noise$V_{ni,rms}$ @300Hz	V	8.4m	13μ
13	Figure of Merit	NEF^2V_{dd}	41.47	29.7

III.   DISCUSSIONS

Gain, The neural amplifier (Low Noise Amplifier) is the first stage which is responsible to acquire the low amplitude or weak neural signal which ranges in milli-volts or micro-volts based on the neural activities. The neural signal obtained from the subject is amplified first and then propagated to the succeeding stage for conditioning. CMFB technique exhibit gain of 63.29dB and another amplifier using DTMOS architecture shows the gain of 59.23dB.

Phase margin, is the parameter which is responsible to signify how stable the op-amp is, in order to attain the good stability adequate phase margin is needed. Too much of the ringing is undesirable in signal. As neural signals obtained posses low amplitude, it is important to attain desirable phase as in accordance to simulation 60dB phase margin is obtained by simulation of neural amplifier(Telescopic op-amp using CMFB) which is most desired figure and another neural amplifier based on DTMOS has attained the phase margin of 80dB

CMRR(Common Mode Rejection Ratio),of neural amplifier is basically the measurement of the capability of an op-amp to reject the common mode signals. At the input of an op-amp if the applied signals are equal as result the differential input voltage remains unaffected and by the same output should not be affected. In the case of neural amplifier high value of CMRR is mandatory, Since the amplitude of neural signals tends to remain weak frequency range as well have low frequency and prone to get coupled with power line interference from the ac source and environmental noise. With issues mentioned above the neural amplifier (using CMFB technique) approaches the CMRR of 110dB and another neural amplifier (using DTMOS) exhibits the CMRR of 65dB. As a result neural amplifier (using CMFB technique) suits better than another one.

PSRR,In order to obtain the proper amplification of neural signal it is necessary to reject the supply voltage variation and fluctuation, as the amplitude of the neural signal is weak. These variations are comparatively larger than the neural signals. So the

high value of PSRR is necessary, such that the neural signals amplified more rather than the supply voltage. The PSRR obtained from the simulation of both the design neural amplifier (using DTMOS) is 22.40dB and another one is neural amplifier (using CMFB) is 80dB. Neural amplifier (using CMFB) seems to be best suited for initial stage amplifier

Noise, The neural signals obtained from the subject posses lower value of amplitude which ranges from $100\mu V$-$500\mu V$. The sources of noise such as interfering noise and external noise get coupled to the wire responsible to deliver low amplitude neural signals. It is very critical issue which in result corrupts the signal of interest or may not detectable. The noise obtained from the neural amplifier (using DTMOS technique) is 400mV/Hz and result of neural amplifier (using CMFB) is 100uV/Hz. As a result neural amplifier using CMFB proves to be better suited than other design.

Power Dissipation, A large quantity of data is streamed continuously by multi-channel neural recording system which is transmitted in order for amplification in regard to further processing of signal. Basically dissipation of power should be low and it is essential since it causes excessive heating of tissue and may cause damage to the neural tissue. Power consumption obtained from the simulation of neural amplifier (using DTMOS) is $2.61*10^{-09}$W and another amplifier using CMFB technique has dissipation of $1.00*10^{-10}$W

IV. CONCLUSION

In this research paper, I have designed Neural Amplifier of Low Noise Amplifier (LNA) in which I have proposed respectively two architectures which were studied and implemented namely Telescopic Amplifier using CMFB technique and Variable Differential Trans-conductance amplifier using DTMOS technique as neural amplifier or LNA. Both the designs were implemented and simulated; the parameters obtained are compared and analyzed.

Neural acquisition system involved in measurement of weak amplitude neural signals and one predominant factor in such application is noise once coupled with signal may corrupt signal of interest and become limiting factor for the performance of system. The overall noise at the input of interfacing system is composed of noise is basically get introduced through electrode system. As the neural signals or spikes are characterized with low frequency and low amplitude which posse's stringent requirements on amplifier design, the amplifier should have characteristics such as high value of CMRR ,PSRR, Gain and low value of NEF, Noise, Power dissipation and Input referred noise. Neural interfacing system is responsible to enable the continuous interaction with the sum of neural cells by the action of recording in order to provide facility for early diagnosis and prediction of the neural activities such that the corrective or preventive measures could be undertaken for the proper and desired treatment of brain ailment. As the input stage, neural or low noise amplifier of receiver system is predominant in order to determine the overall system performance. On the behalf of comparison in between the two architecture, it can be stated that the best suited design of neural amplifier or LNA which is proposed for the first stage is Telescopic Amplifier using CMFB technique which stands best suited in all cases.

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