iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 7 **Issue:** VI **Month of publication:** June 2019

DOI: http://doi.org/10.22214/ijraset.2019.6367

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177
Volume 7 Issue VI, June 2019- Available at www.ijraset.com

Design of Low Power Arithmetic Units Using the Adaptive Nano Ionic Memristors (ANIM) Model for Chaotic Applications

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Abstract: ***Recent researches on low power, area efficient, faster operation leads to evolution of the new nanoscale solid state device memristor which occupies the major role in the future electronic systems. Memristor is the promising technology which can replace the traditional technology which faces the major issues in scaling down of the devices. Memristor based device designing and scaling leads to design of future processors which plays an important role in quantum computing. Considering above criteria, the paper proposes design of Arithmetic Logic units (ALU) based on memristor which works on the principle of adaptive voltage thresholds (ANIM) based on windowing doping functions. The proposed model has been simulated in MATLAB and various parameters such as area, power has evaluated and compared with the other conventional Nano transistors and also with the traditional CMOS based design technology. The proposed ANIM model has more advantage in executing the non-linear dynamic chaotic systems and compared with the TEAM (ThrEshold Adaptive Memristor) and VTEAM (Voltage ThrEshold Adaptive Memristor) models in which the proposed model outperforms existing algorithms in terms of Area efficient and Power efficiency.***

Keywords: ANIM, Memristor, ALU, TEAM, VTEAM, Nano Transistors, CMOS technology.

I. INTRODUCTION

Nano ionic devices have the tendency to replace the conventional memory technology and lead the market towards better computation for the futuristic applications. Memristor, the fourth basic passive circuit element was originally realized mathematically by Leon Chua in 1971 [1], representing the missing link between charge and flux. The physical existence of memristor was reported by HP(Hewlett-Packard) group in 2008 [2]. Memristor finds its application from non-volatile memory to neuromorphic computing [3]-[6]. Memristors can be used to model human brain since its properties is more similar to synapses. Therefore, with the help of synapse as memristor and neurons as a CMOS control circuit, the entire brain can be modelled and fabricated in chip. The basic principle of operation of memristor is based on resistive switching by ionic charge transport comparison to electronic transport in conventional memory devices.

It is characterized as a two-terminal circuit component in which the transition between the two terminals is an element of the proportion of electric charge that has gone through the gadget. Memristor isn't a storage component for the energy.



Fig. 1 MEMRISTOR

The doping of thin film is actually represented by oxygen vacancies. The doped oxide region has a high resistance value Ron while the undoped region has a low resistance R_{off}. Several assumptions which have been taken into consideration while establishing this model. Those are: a) ohmic conductance b) equal mean ion mobility and c) linear drift of ions under the influence of a uniform electric field. A state variable is used to properly identify the switching phenomenon between the on and off states of the memristor. The mathematical expression representing the same is in the form of a simple differential equation given in the form

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$dw/dt=\mu[R_{on}/D] * i(t)$ (1)

$V(t)= [[R_{on}*w(t)/D * R_{off}*[1-w(t)/D]]$ (2)

Where w(t) is the static variable of the memristor and R_{on} is the On Resistance and Roff is the Off resistance. μ is the average dopant mobility and D is the length of the memristor. The window functions serve a major role in the validation of the 'linear ion drift model' as they help to limit the drift of the mobile ions within the physical bounds of the device. There are various kinds of window function such as the Jogelkar window [11], Biolek window [12], Prodromakis window [13] etc. The linear model has the advantage of being mathematically simple, computationally efficient and optimized. The only disadvantage being the reduced amount of non-linearity that could be exhibited through the use of this model. To suffice this several new models have been proposed such as the TEAM and non-linear ion drift model [14] These models are characterized by several assumptions, complex mathematical equations and various complicating physical phenomenon. Nowadays with an advent of nano scale memristor, the development of more powerful but smaller computers, the ALU becomes smaller and complex. The factors that affect the development of smaller but more complex chips are the fabrication technology, cost and designer productivity. The continuing demand for high density high speed integrated circuits (ICs) can be addressed at different levels of design, such as circuit, process technology and architecture.

Hence the paper proposes the new model of memristor ANIM which works on the principle of the adaptive voltage-controlled mechanism based on windowing functions. The various ALU circuits has been modelled, simulated and evaluated. Also, the proposed ANIM model has been compared with the conventional nano transistor and CMOS devices.

The paper is organized as follows as Section-I deals with the related works, the working models, characteristics of ANIM model are detailed in Section-II, implementation of ANIM model for different circuit designs were detailed in Section-III. Finally results and comparative analysis were discussed in Section-IV.

II. RELATED WORKS

Valeriy A. Slipko demonstrate that the genuine decision of window capacity is vital for the prescient displaying of memristors. this work utilizes the memristor attractors, this work shows that whether stable fixed focuses exist relies upon the kind of window capacity utilized in the model. The principle discoveries are detailed as far as two memristor attractor hypotheses, which apply to expansive classes of memristor models. For instance, of these discoveries, the proposed system predicts the presence of stable fixed focuses in Biolek window work memristors and their nonappearance in memristors portrayed by the Joglekar window work, when such memristors are driven periodic alternating polarity pulses. It is foreseen that the consequences of this investigation will contribute toward the improvement of increasingly complex models of memristive gadgets and frameworks [1].

Garrett S. Rose described a novel chaos-based arithmetic logic unit. This chaotic ALU is constructed from chaogates that can evolve through different functional configurations. Given the complexity of the state space of a chaogate, it is shown that the state space of the chaos-based ALU is also complex and leads to an exponential number of possible op-code sets as the chaotic oscillators are allowed to evolve over time. It should be pointed out that the number of possible op-code sets, though large, is made possible with a minimal amount of hardware. The complexity of the control values used to generate different operations provides a useful architectural handle for code obfuscation [2].

Michaux Kountchou deals with the problem of optimal synchronization of two identical memristive chaotic systems. We first study some basic dynamical properties and behaviours of a memristor oscillator with a simple topology. An electronic circuit (analog simulator) is proposed to investigate the dynamical behaviour of the system. An optimal synchronization strategy based on the controllability functions method with a mixed cost functional is investigated. A finite horizon is explicitly computed such that the chaos synchronization is achieved at an established time. Numerical simulations are presented to verify the effectiveness of the proposed synchronization strategy. Pspice analog circuit implementation of the complete master-slave-controller systems is also presented to show the feasibility of the proposed scheme [3].

K. Paramasivam investigated Memristor and its presentation by utilizing two diverse window works in MATLAB. Hysteresis bend is gotten for investigation. Memristor based memory cell is planned utilizing memristor with proposed window capacity to investigate the presentation utilizing LT in 180nm innovation. Peak and normal power results are contrasted. It demonstrates that 94% of intensity is diminished in the proposed memory cell [4].

Shyam Prasad Adhikari presents a circuit-theoretic foundation of the “memristor,” and clarifies why it is fundamentally different from a 3-terminal device with a similarly-sounding name called the “memistor.” Here we show that while the memristor is a basic 2-terminal circuit element based on classic nonlinear circuit theory, the memistor is an ad hoc 3-terminal gadget devised for one specific application, and does not qualify as a 3-terminal circuit element because it is impossible to predict its behavior when connected with other circuit elements [5].

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Amirthalakshmi designed the 8-bit ALU using conventional CMOS and low power nano device SET. It is simulated in SPICE software and it is proved that the ALU using SET consumes much less power when compared to the conventional CMOS. This 8-bit ALU can be used in many digital processors to make it power efficient compared to the conventional processors [6].

Mohammed F. Tolba proposed General continuous and discrete memristor IP cores for FPGAs and validated that can be easily interfaced and used with a wide range of applications. The efficiency of the designed core is proved through the low area utilization and the high speed. The proposed IP core models provide extra degrees of controllability than the conventional switching model by increasing the number of states. These models can develop new ideas to construct essential trend in the research community. A comparison of the hysteresis loops between the models was presented. The functionality of the proposed models is verified in the memristive chaotic oscillator where various chaotic attractors are generated [7]. Satyajeet Sahoo focused on the implementation of 1-bit Arithmetic Logic Unit (ALU) using memristors based on Voltage Threshold Adaptive Memristor (VTEAM) model in Cadence Virtuoso environment. Considering the size of Memristor in nano regime helped in decreasing the feature size thus enhancing the density. This will lead to reduction of the die area in comparison to Complementary Metal Oxide Semiconductor (CMOS) based ALU [8]. Vinay Saripalli characterized the Energy-Delay performance of logic circuits realized using Single Electron Transistor (SET) devices. As technology scaling progresses, it is getting increasingly challenging to continue reducing energy, especially at low activity factors and low VCC, due to increasing leakage energy dominance. A SET can be viewed as the ultimate transistor operating in the limit of scaling; hence, this work uses this device as an example to understand the challenges of energy-reduction in the nanoscale. This work explores the design space for SET-devices based on physical dimensions and electrostatic properties. Based on this design space, this work characterizes SETs into categories of applications: complementary-logic design, and BDD design with sense amplification. Based on these two circuit design styles, this work compares the Energy-Delay products of benchmark logic circuits, implemented using nanometer CMOS and SETs [9].

III. PROPOSED ANIM MODEL

Previously the memristor models has been proposed without the threshold model which varies the resistance for any application of current and voltage. These type of memristor model exhibits only the linear characteristics which may not applied for chaotic model. The VTEAM model has been proposed which works on the principle of the voltage-controlled thresholds. This leads to non -linear characteristics from the model and finds its applications in chaotic areas. But the major drawback of the VTEAM and other models, non-linearity is executed only depends on the voltage thresholds. The proposed ANIM model were designed based on the two parameters such as the voltage threshold and windowing doping factors. The several windowing functions were used in ANIM model which are described as follows

1) Strukov window function
2) Benderli window function
3) Joglekar window function
4) Biolek window function
5) Prodromakis window function

Joglekar et al. proposed novel window function [7] gives zero float at the edges yet it has terminal state issue. Subsequently the memristor may not work appropriately at the edges. Biolek et al. proposed another window function [8] in which parameter current I is acquainted with limit the terminal state issue. Brokenness in window capacity is its drawback. Strukov et al. offered the window work [5] and it tends to be changed as f (x) =x-x2, by Benderli and Wey [9] to build up a zest full scale model of TiO2 memristor.

The adaptable windowing capacities was proposed by Prodromakis [10] with parameter j which takes care of the issue of confinement on greatest estimation of unity. A window work [11] proposed by Sangho Shin et al. with non-zero esteem (ä) even at limits can be utilized to dispense with the backing issue however it causes the abundance aggregation charge at memristor.

The proposed ANIM model considers the above windowing functions along with the different voltage thresholds. The ANIM model is considered to be extension of VTEAM models in which the voltage thresholds are varied in accordance with the windowing functions to produce the complex non-linearity behavior suitable for the chaotic applications. The mathematical model which was used for ANIM model is given as follows

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}\left(\frac{v(t)}{v_{off}} - 1\right)^{a^{off}} . f_{off}(w), 0 < V_{off} < v \\ 0, v_{on} < v < V_{off} \\ k_{on}\left(\frac{v(t)}{v_{on}} - 1\right)^{a^{on}} . f_{on}(w), 0 < V_{on} < v \end{cases} \quad (3)$$

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$$i(t) = \left[R_{on} + \frac{R_{off}-R_{on}}{W_{off}-W_{on}}\,(W - W_{on})\right]^{-1} . v(t) \quad (4)$$

Where koff, k_{on}, α^{off} are constants, V_{on} and V_{off} are the threshold voltages used for the modelling the ANIM model. $f_{on}(W)$ is the windowing functions used in the ANIM model for non-linearity characteristics.

The variation of the different voltage threshold in accordance with the windowing functions which are used in the ANIM model is listed in table I

TABLE I
Operating Point Of The Anim Model For Non -Linear Characteristics

SL.NO	Voltage Thresholds(V)	$f_{on}(W)$
01	10-15	Prodramakis Windows
02	8-10	Biolek Windows
03	11-14	Prodramakis Windows
04	12-15	Joglekar Window
05	11-15	Prodramakis Windows

Table I shows the adaptive voltage thresholds are considered between the 10-15V with the different window regions. These regions in the proposed model exhibits the non -linear characteristics which are discussed in the section-III.

A. ALU design using ANIM model

The arithmetic logic units are the heart of the microprocessors. Since all the processors are leading the way to quantum computing, ANIM model is employed to design the various structures such as adder, subtractor, multiplier, comparators and shifters. The proposed model has replaced the CMOS designs and also Nano transistors. The ANIM model along with CMOS has been integrated to design the ALU which are used to calculate the area and power. The following circuits used for employing the ANIM model is as follows

1) ANIM Model For ADDER

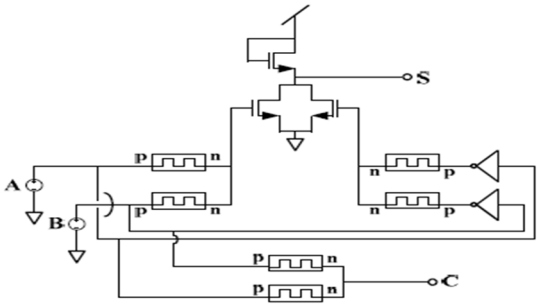


Fig. 2 Shows the ANIM model for Adder Circuits in ALU

2) ANIM Model For Subtractor

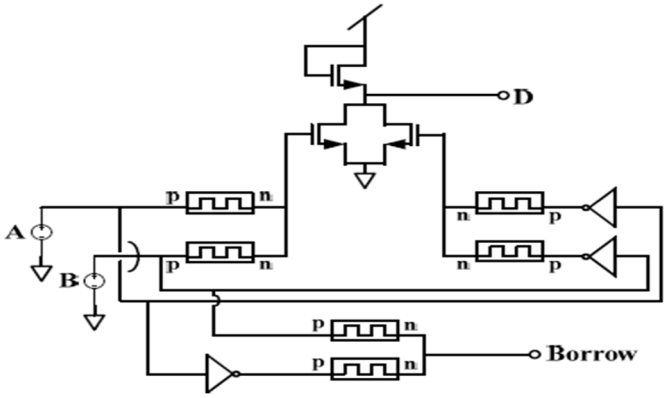


Fig. 3 Shows the ANIM model for Subtractor Circuits in ALU

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3) ANIM Model for Comparator

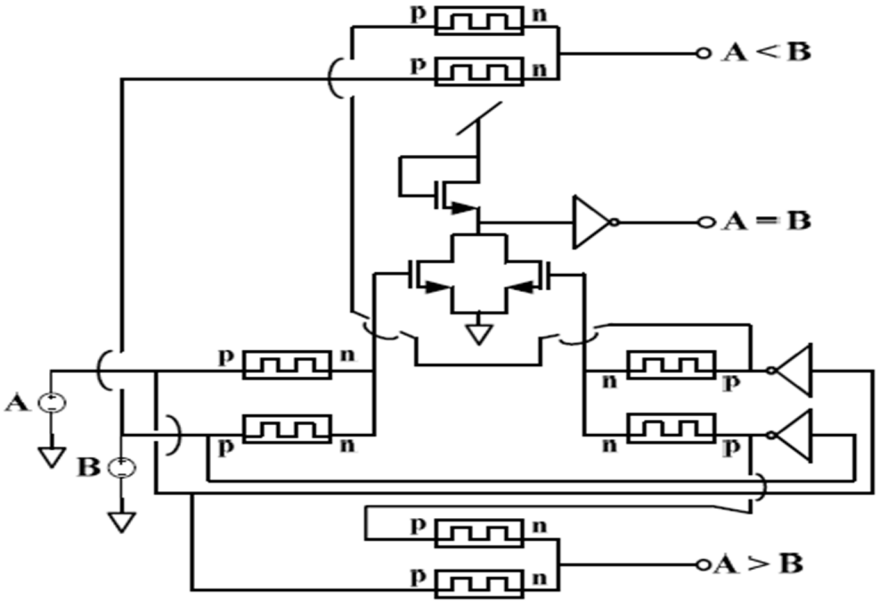


Fig. 4 Shows the Schmetic Models Using ANIM model for Comparator

4) ANIM Model for Shifter

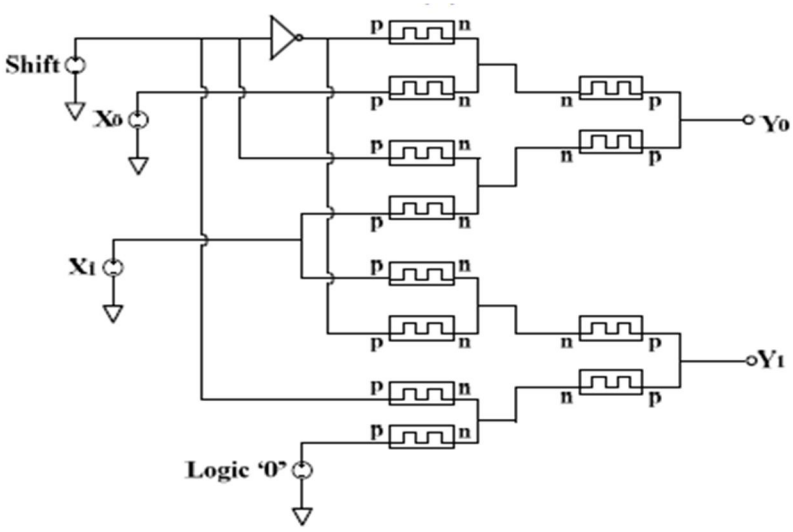


Fig.5 Shows the Schmetic Models Using ANIM model for Shifters

5) ANIM Model For Multiplexer

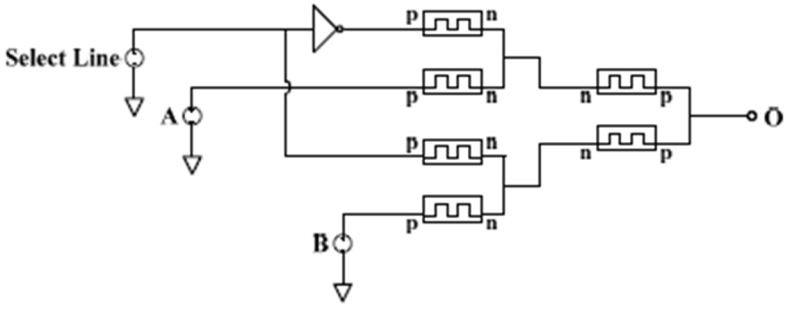


Fig. 6 Shows the Schmetic Models Using ANIM model for Multiplexer

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IV. RESULTS AND DISCUSSION

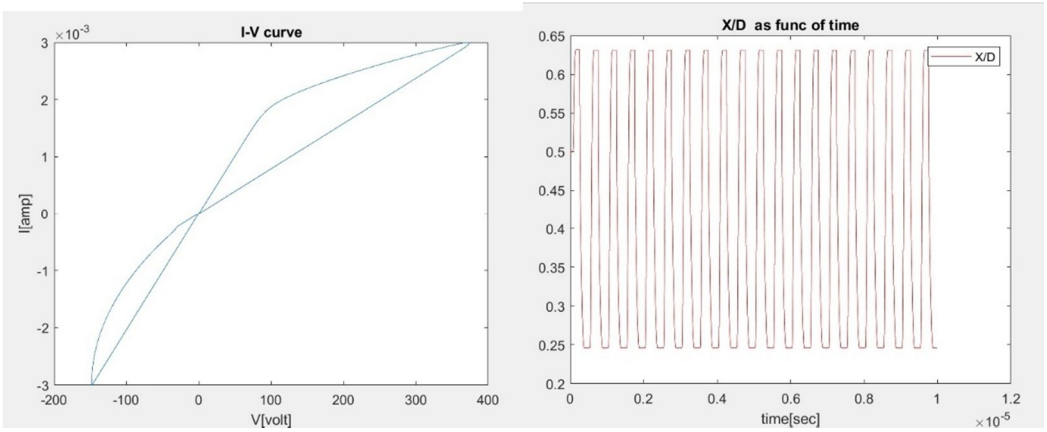
A. I-V Characteristics Of Proposed ANIM Model

The parameters used for modelling the proposed ANIM model is tabulated in the table II

TABLE II
Parameters Used For Anim Model

SL.NO	Parameters taken for Modelling	Parameter value
01	Num_of_cycles	20 s
02	I-Amp	0.003
03	Frequency	2e6Hz
04	Initial Condition	0.5
05	D	3e-9 nm
06	Vt=Voltage threshold	10-15V
07	P_Coeff	02
08	R_{off}	2e2 ohms
09	R_{on}	100 ohms
10	Model Used	Non-Linearity Drift Model
11	Dopants Mobility	1e-15

The proposed ANIM model has been modelled using MATLAB 2019 version using the different voltage thresholds and windowing functions to execute the non-linearity applications. The different I-V characteristics for the ANIM model for different voltages are shown as follows



(a) (b)

Fig. 7 I-V characteristics for the proposed ANIM model for the V=100 mV along with the Joglekar window

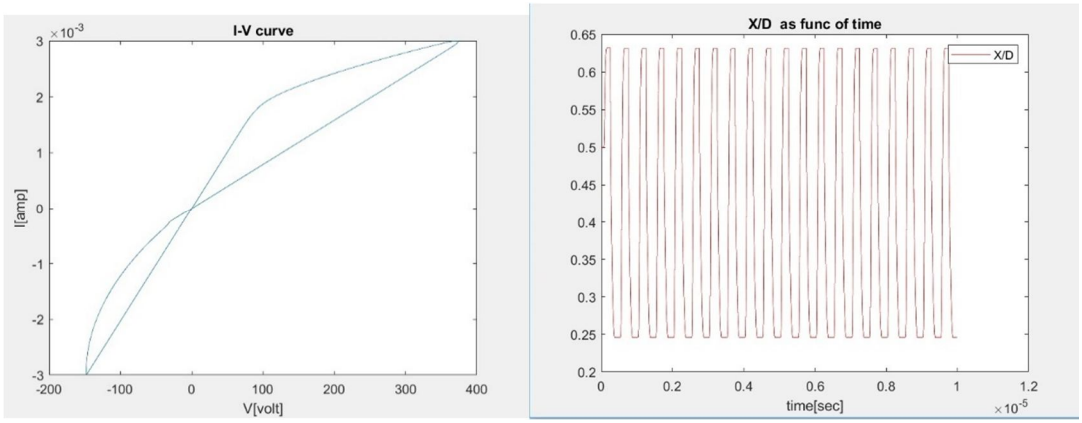
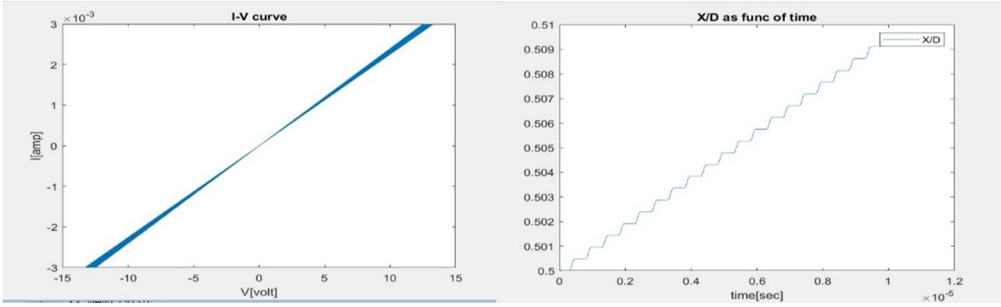


Fig. 8 V-I characteristics for the proposed ANIM model for the 120 mV along with the Biolek Window

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(e) (f)

Fig. 9 V-I characteristics for the proposed ANIM model for the V=10-15 V along with the Prodromakis Window

Fig 7and Fig 8 shows the linear characteristics of the ANIM model when the voltage is 100 mV using the biolek and joglekar windows. Fig 9 clearly shows the non-linear characteristics of the ANIM model when the voltage is between 10 to 15V with the prodromakis windows. Hence the proposed ANIM model executes the non-linearity sequences when threshold voltage is between 10 to 15V long with the prodomokis windows.

B. Area Comparison

As we discussed, it is clear that the memristor based ALU design occupies lesser area when compared to the CMOS and Nano transistors. Table III clearly depicts the comparative analysis between the above techniques

TABLE III
Comparative Analysis Of The Area Utilized Between The Proposed Anim, Nano Transistors And CMOS

Sl.no	ALU designs	ANIM model	Nano Transistor	CMOS	VTEAM [15]
01	Adder	5M	12T	15T	6M+5T
02	Subtractor	5M	14T	19T	6M+4T
03	Shifter	5M	12T	17T	6M+5T
04	Multiplier	7M	16T	17T	7M+6T
05	Comparator	4M	12T	15T	5M+5T
06	Invertor	2M	1T	3T	2M+0T

*M- memristor, *T- transistors

The comparative analysis of the area utilized between the different techniques are shown in table III. Table clearly shows the ALU design using ANIM model occupies less area when compared with the other techniques such as Nano transistors, CMOS and VTEAM models. The 50% of the less area is occupied by the ANIM model which also occupies the less die -areas during fabrication process.

C. Peak Power Analysis

As discussed above, area occupied by the ANIM model is very less and peak power is calculated and compared with the other techniques. Table IV shows the Peak power analysis of proposed models and other models

TABLE IV
Comparative Analysis Of The Peak Power Between The Proposed Anim, Nano Transistors And CMOS

Sl.no	ALU designs	ANIM model(mW)	Nano Transistor(mW)	CMOS (mW)	VTEAM [15] (mW)
01	Adder	0.563	0.798	0.945	0.570
02	Subtractor	0.452	0.788	0.823	0.580
03	Shifter	0.431	0.763	0.880	0.508
04	Multiplier	0.753	0.976	1.459	0.798
05	Comparator	0.231	0.411	0.456	0.341
06	Invertor	0.200	0.501	0.732	0.249

The comparative analysis of the peak power between the different techniques are shown in table. Table IV clearly power consumed by the ALU designed using ANIM model consumes only 30% of the total power consumed by the Nano transistors, CMOS and Hybrid Models. Since the power consumed by the proposed ANIM model is very less, it can occupy the major share in design of IoT security devices.

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D. Overall Comparative Analysis

The proposed ANIM model is compared with the different techniques and are tabulated in table V

TABLE V
Comparative Analysis Anim Model With Other Techniques

Sl.no	Techniques Used	Area Efficiency	Power	Non-Linearity	Nature	Chaotic Applications
01	CMOS	High	Low	No	Complex	Not Suitable
02	Nano Transistor	High	Low	No	Easy	Not Suitable
03	TEAM [14]	High	Low	Yes	Complex	Suitable
04	Hybrid Model [15]	High	Low	Yes	Complex	Suitable
05	Proposed ANIM model	Very High	Very Low	Yes	More Complex	Suitable

Table V Clearly Shows the proposed ANIM model outperforms other techniques both in nanoscale and other hybrid models which makes the proposed models to find it more suitable for designing chaotic encryption systems to be implemented for an IoT security applications.

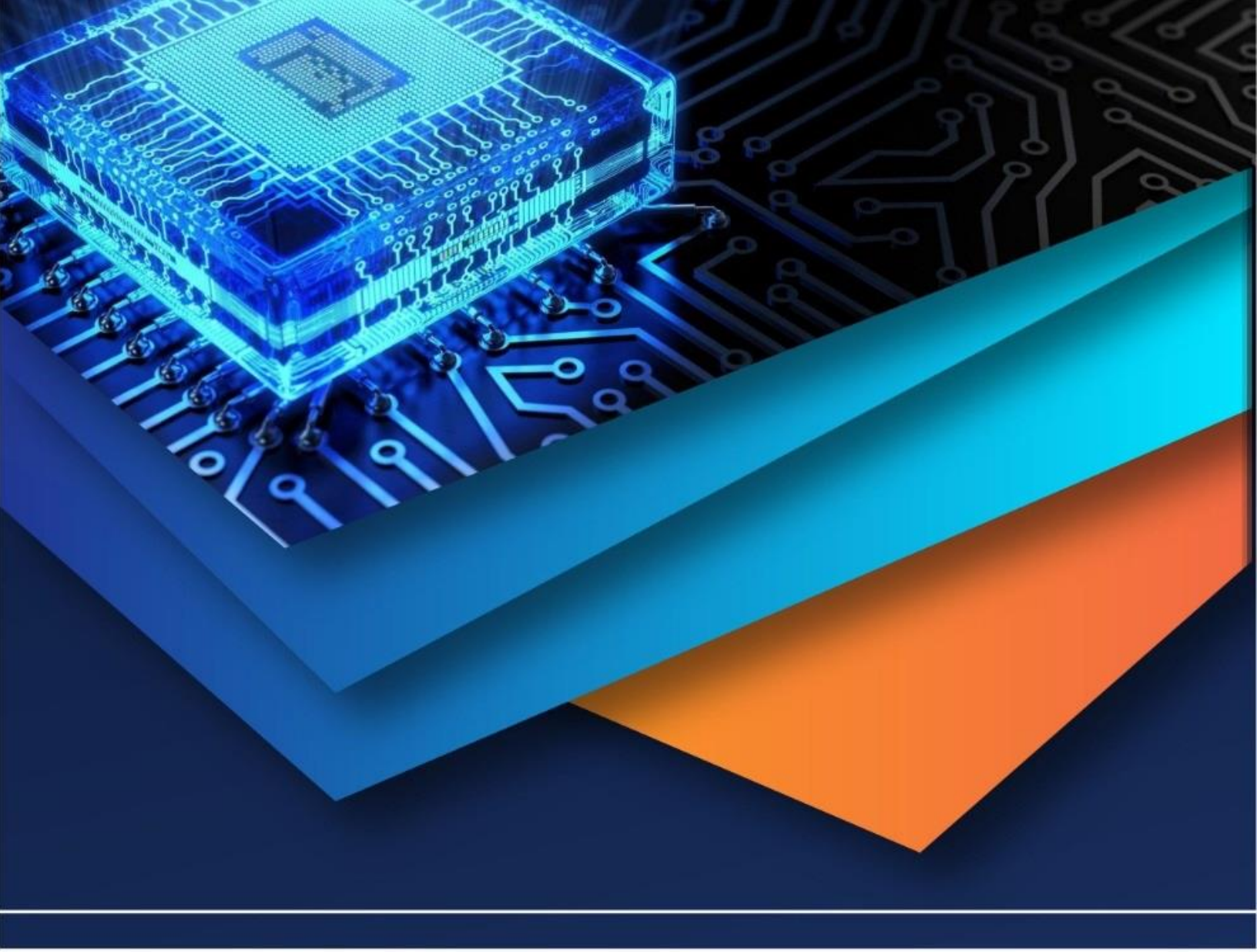
V. CONCLUSION

The proposed ANIM model works on the principle of adaptive thresholds along with the windowing functions. The ANIM model has been modelled using MATLAB to find its non-linearity characteristics and ALU has been designed and simulated using the proposed ANIM model. It is clear that the area utilization is reduced to 50% when compared with the other techniques and power is reduced to 30% which finds its place in different applications of wearable devices. Moreover, the complex non-linearity characteristics of the proposed ANIM model will play a major role in the IoT encryption process.

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