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An Arithmetic Logic Unit using Vedic Mathematics – A Review

Tirupati B. Yadav[1], Devendra S. Chaudhari[2]
[1]*PG Student,* [2]*Professor of Electronics and Telecommunication Department, Goverment College of Engineering, Jalgaon, Maharashtra, India*

Abstract: ***Arithmetic and Logic Unit (ALU) is the most crucial and core component of central processing unit which consists of many computational units like adders, multipliers, logical units, etc. Real time applications such as controlling environmental conditions demand quick response of the processor for processing the acquired signals. The vedic mathematics consists of many sutras which can be used for improving speed with reduced component requirement and also delay. It accomplishes arithmetic, logic operations on integers stored in accumulator, register array, operand register and fetch value from external memory. VLSI architecture design should meet the desired speed, power, size, etc. In this paper vedic mathematics sutra which can be used for enhancing the overall performance of the processor is discussed with a brief mention of a vedic mathematic based ALU.***
Keywords: ALU, Vilokanam, UrdhvaTiryakbhyam, Nikhilam, Parvartaya sutra.

I. INTRODUCTION

The word “Vedic” is derived from the word “Veda” which means the store-house of all knowledge. Vedic Mathematics is an ancient system of mathematics existed in India. In this eminent approach, methods of basic arithmetic are simple, powerful and logical. Another advantage is its regularity. Because of these advantages, Vedic mathematics has become an important topic for research. The technique use in Vedic Mathematics is mainly based on sixteen Sutras. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884 –1960) after his eight years of research on Vedas[1]. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras[2]. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time. ALU is the main part of the central processing unit which performs various arithmetic and logical operations. The speed of arithmetic unit is of extreme importance and depends greatly on the speed of multiplier. Therefore, the technologies are always looking for new algorithm and hardware so as to implement this operation in much optimized way in the terms of area and speed. Vedic Mathematics deals with various branches of mathematics like arithmetic, algebra, geometry etc. The use of Vedic Mathematics concepts in the computation algorithm of a processor will reduce the complexity of execution time, area and power consumption etc. The efficiency of Urdhav Triyagbhyam Vedic method for multiplication, strikes a difference of actual process of multiplication, by enabling parallel generation of intermediate product, eliminating unwanted multiplication steps with zeros and scaled to higher bit level. This formula (Sutra) can used to build high speed power efficient multiplier in a processor. Nikhilam division algorithm just involves the addition of numbers which is very much different from the traditional division technique including multiplication of big numbers by the trial digit of the quotient at each step and subtracts that result from dividend at each step. This work aims to design arithmetic and logic unit using the technique of ancient Indian Vedic Mathematics to improve the performance of a processor[3].

II. WORK ON VEDIC ALU

Based on the Vedic mathematics concepts for digital signal processing applications, many researchers have proposed ALUs and other computational units. From these research, they have proved that conventional arithmetic computational algorithms are very robust when compared to proposed arithmetic computations.

In one of the studies 16-bit Vedic ALU using Vilokanam sutra, Urdhva Tiryakbhayam sutra and Parvartaya sutra for performing the addition, subtraction, multiplication and division respectively was proposed. In this technique to show the efficiency of proposed vedic ALU at 16 bit level, it has been compared with conventional ALU. For the comparison purpose some standard papers have been used. Addition using ripple carry scheme is less efficient when compared to applying vedic addition using vilokanam sutra in terms of delay and area. Subtraction using ripple carry scheme is less efficient when compared to applying vedic subtraction using vilokanam sutra in terms of delay and area. The efficiency of proposed vedic multiplier at 16-bit level has been compared with other

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popular multiplier structures and vedic multiplier showed lowest path delays. The result of device utilization and delay as the restoring division method shows a larger delay as compared to the proposed divider and the percentage of device utilization in restoring division method is quite [4].

In the other study an ALU design using vedic mathematics approach was proposed. High speed 8*8 bit multiplier was designed and analyzed. This method is different from the conventional method of employing product of two numbers accomplished by the process of add and shift. This method involved the vertical and crossed multiplication and it was found to be efficient and fast.[5].

Some researcher have proposed a modified compressor based multiplier, constructed experimental set up that used Vedic mathematics to get a high speed multiplication operation. The designs of 16x16 bits and 32x32 bits Vedic multiplier was designed using Xilinx 13.2 (vertex 7). The computation delay for 8x8 bits multiplier was found to be 5.02 ns, the computation delay for 16x16 bits multiplier was 9.09ns. The computation delay for 32x32 bits 4:2 compressor Vedic multiplier was 15.8 ns and for 32x32 bits Wallace tree Vedic multiplier was 12.7ns. It is therefore seen that the Wallace tree Vedic multiplier observed to be faster than the 4:2 compressor Vedic multiplier. For vertex 5 the computation delay for 32x32 bits 4:2 compressor Vedic multiplier was 18.71ns and for 32x32 bits Wallace tree Vedic multiplier were 18.80ns. Urdhvatiryakbhyam, Nikhilam and Anurupye sutras used in proposed algorithm results in minimum delay, power and hardware requirements for multiplication of numbers. Use of a compressor observed to be easy processing element with less complexity which used in digital logic design for compression of data. [6]

Some researcher have proposed an ALU design using Vedic mathematics concepts. In their proposed designed vedic multiplier analysis was carried out using *Urdhav Triyagbhyam* sutra. In this multiplication they eliminated the unwanted steps with zeros that enabled parallel generation of intermediate product. In this high speed power efficient multiplier was achieved. [7] In other studies an ALU design using vedic mathematics approach was proposed. Every digital domain based technology was operated only by ALU either partially or whole. For this high speed ALU was required. The proposed ALU could perform three arithmetic operations with the desired speed. [8]Some of the other researcher have proposed an 8 bit ALU design using vedic mathematics concepts. In this technique, he reduces the propagation delay in processor and hardware complexity in terms of area and speed by eliminating the unwanted multiplication steps[9]. In one of the study, it is discussed that VLSI architecture have higher orders of time and space complexities. In this he designed binary division architecture using Nikhilam sutra and Paravartya sutra[10].

III. AN APPROACH TOWARDS SPEED ENHANCEMENT

After referring to the researched papers of many researchers it can be said that the ALU can be implemented using the vedic sutras as follows:

A. Addition Using Vilokanam Sutra

Vilokanam sutra performs addition which is carry independent due to which the delay gets reduced and enhances the overall speed of the processor.

B. Subtraction by 2's Complement using Vilokanam Sutra

The subtraction can also be performed by simply performing the 2's complement method.

C. Multiplication using Urdhva Tiryakbhayam Sutra

The word "Urdhva-Tiryakbhyam" shows vertical and crosswise multiplication. This sutra is used for the multiplication of two numbers in decimal number system. The same concept can be applicable to binary number system.

Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc.

These methods can be directly applied to plane and spherical geometry, trigonometry, conics, calculus (both differential and integral), and applied mathematics. In conventional mathematics the step required for calculation are more, in order to reduce the step for calculation in Vedic mathematics plays great role. This is so because the Vedic formulae are to be based on the natural principles on which the human mind works. Figure 1 indicate the line diagram for multiplication of two 2 digit numbers which perform the 2 digit multiplication operation. Take a two numbers, multiply the numbers in the unit place and put the product under unit place. Cross multiply first unit place tens place number and add the two products and place the answer to the left of the unit place's answer. Multiply the numbers in the tens place and place the answer to the left side of the previous answer step. This is a very interesting part of the mathematics and it presents some effective algorithms that can be applied to various branches of engineering.

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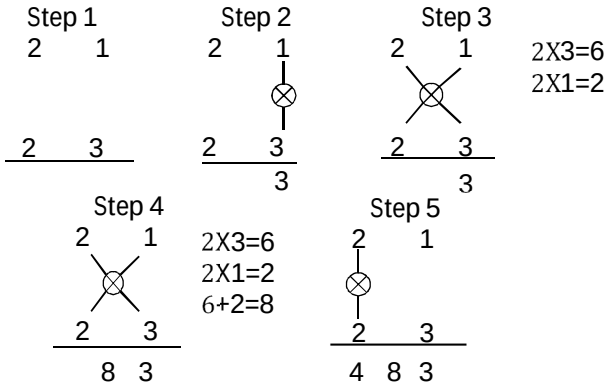


Fig- 1: Line Diagram for Multiplication of Two 2 - Digit Numbers

The multiplier architecture can be generally classified into three types. First is the serial multiplier which emphasizes on hardware and minimum amount of chip area. Second one is the parallel multiplier (array and tree) which carries out high speed mathematical operations.

Observation is that the partial products and their sums are calculated in parallel due to which the multiplier independent of clock frequency of processor, thus multiplier require same amount of time to calculate product.

4. Division using Nikhilam Sutra/Parvartaya Sutra

Nikhilam sutra is used when the value of dividend is below the base of powers of 10 whereas the Parvartaya sutra is used only when the value of dividend is above the base of powers of 10, both Nikhilam and parvartaya sutra provides the less number of iterations due to which the calculation becomes fast and the processor speed to enhanced.[4]

IV. CONCLUSION AND FUTURE SCOPE

Arithmetic and Logic Unit forms an important part of the digital system design and various architectures are proposed which reduces the area or the timing delay of the circuit in recent years. Design with vedic sutras is seen to be efficient in speed and area in digital designs with respect to other logical circuits. Considering all the sutras discussed above, we can conclude that the vedic sutras based ALU observed as a promising technique in terms of speed, area and also might be in power also. The work can be further extended with the design of such vedic ALU with the help of vedic sutras.

Vedic Mathematics, developed about 2500 years ago, gives us a clue of symmetric computation. Vedic mathematics deals with various topics of mathematics such as basic arithmetic, geometry, trigonometry, calculus etc. All these methods are very efficient as far as manual calculations are concerned. If all those methods effectively implement hardware, it will reduce the computational speed drastically.

Therefore, it could be possible to implement a complete ALU using all these methods using Vedic mathematics methods. Vedic mathematics is long been known but has not been implemented in the DSP and ADSP processors employing large number of multiplications in calculating the various transforms like FFTs and control applications such as P, PI, PID Controller implementing in FPGA etc. FPGA is advantageous in terms of cost, development time, cost, maintainability and practicability. Stability and minimizing the tendency of mistakes in designs can be solved with all designs in FPGA.

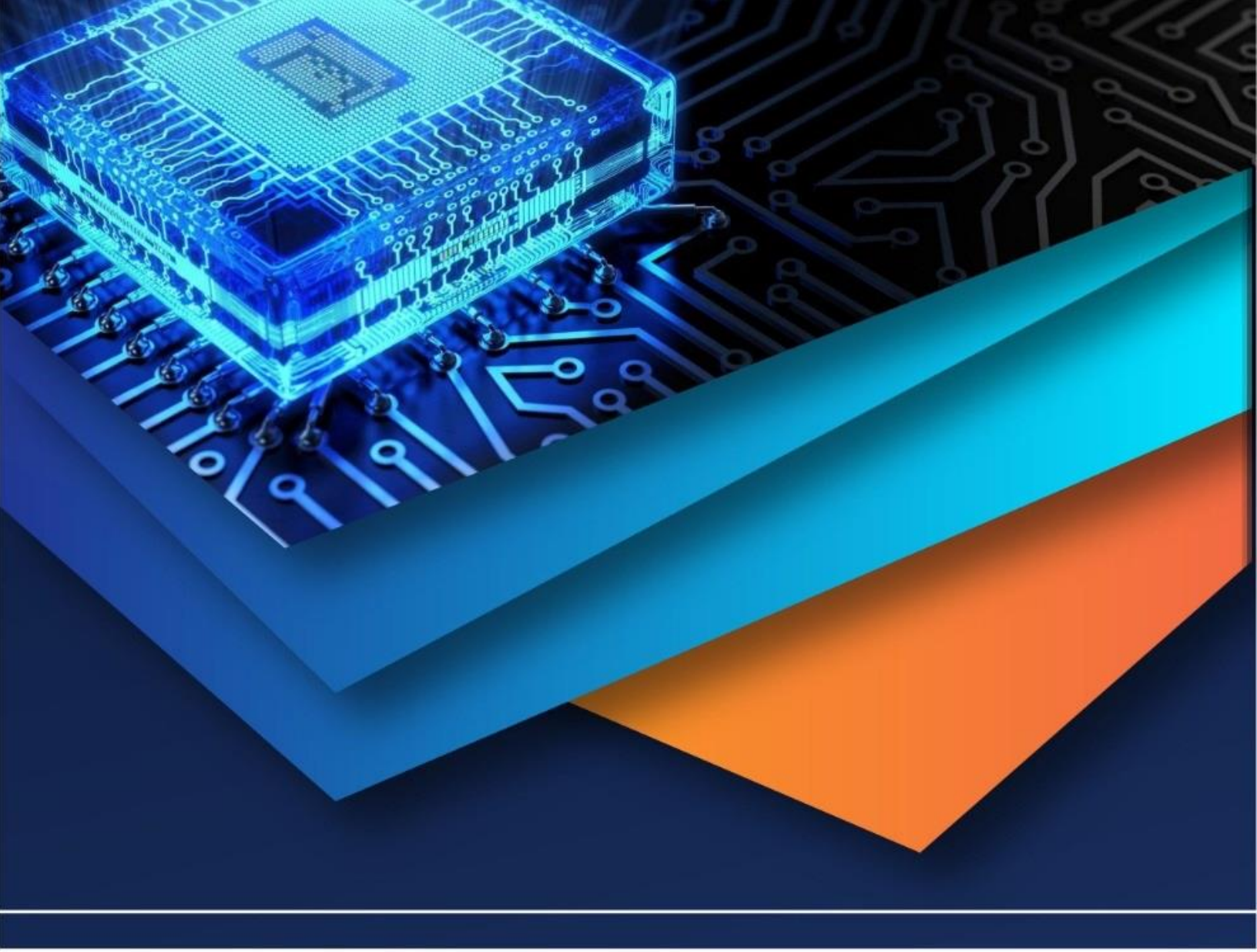
FPGA is used to upgrade obsolete integrated circuits reduces hardware circuit board changes, increases productivity, and ensures that the operational constraints are met. Vedic mathematics sutra are used in different place of different arithmetic operation like division, multiplication, square and cube etc. Used in applications like digital signal processing, image processing, cryptography and computation of heavy calculation. More research and study in the field of Vedic mathematic and their sutras used in multiplier will give better result and have a lot of scope in different field.

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