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Design and Implementation of Robust Router with Cache Memory using VLSI

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Abstract: ***The main approach here is to design a variable hardware router code by using Verilog and a VLSI design for the implementation at the synthesizable level. The focus is to make this router as much variable which will give the robustness for the design to be called as a Robust Router in which we can make the same router to not only go for N number of connections but also to detect all variety of packets and route the same. To do so code should be added with specific case's for every type of packets and to add to the router to route the packets. With this project an approach is to get the basic packets routing with multiple protocols starting with the IPv4 and IPv6.***

Keywords***: Robust Router, Multiple protocols with IPv4 and IPv6, strategies of data transmission.***

I. INTRODUCTION

In today's market, communication is very important and also complex that it is not possible to communicate or send a data from more sources to destination at a time. The routing is done by simple software which will take more time, which has minimal set of pins and it is not possible to make it reconfigurable due its compactness, so HDL based robust router is designed which will help to configure for multiple input and output and it is also possible to communicate with high speed and it will take less time which is well robust at time we can communicate with the many source and destination.

In the emerging environment of high performance IP networks, it is expected that local and campus area backbones, enterprise networks, and Internet Service Providers (ISPs)will use multi giga bit and terabit networking technologies where IP routers will be used not only to interconnect backbone segments but also to act as points of attachments to high performance wide area links. Special attention must be given to new powerful architectures for routers in order to play that demanding role. It is observed that the achievement of high throughput IP routers is possible if the critical tasks are identified and special purpose modules are properly tailored to perform them.

II. RELATED WORK

A. *Design of Switch logic*

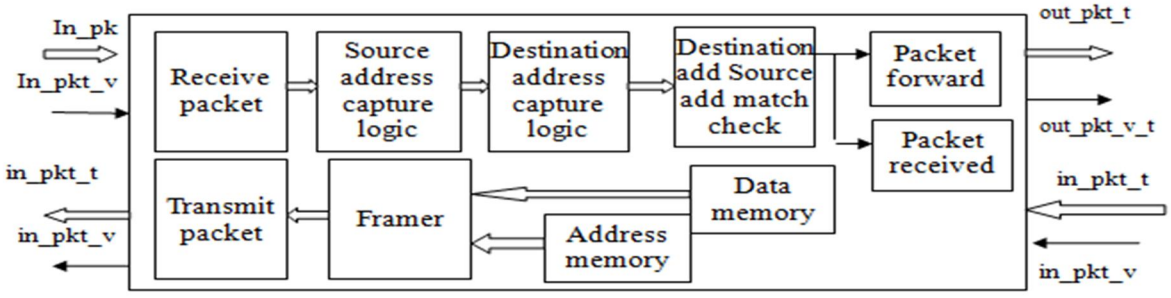


Fig 2.1: Design of Switch logic

Initially in_pkt and in_pkt_v will be received by receive packet block. Then it will send it to source address and destination address decoder, then sent to source and destination address, source address match check. If address is matched packet is terminated and saved inside local memory. If not, it is forward by passing an out pkt_t and out_pkt_v_t. If assume that the switch is a receiving node which would be enabled by TCAM,TCAM interface in in_pkt_t and in_pkt_v will be sent to framer logic through address memory and data memory.

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B. Design of Routing Lookup System

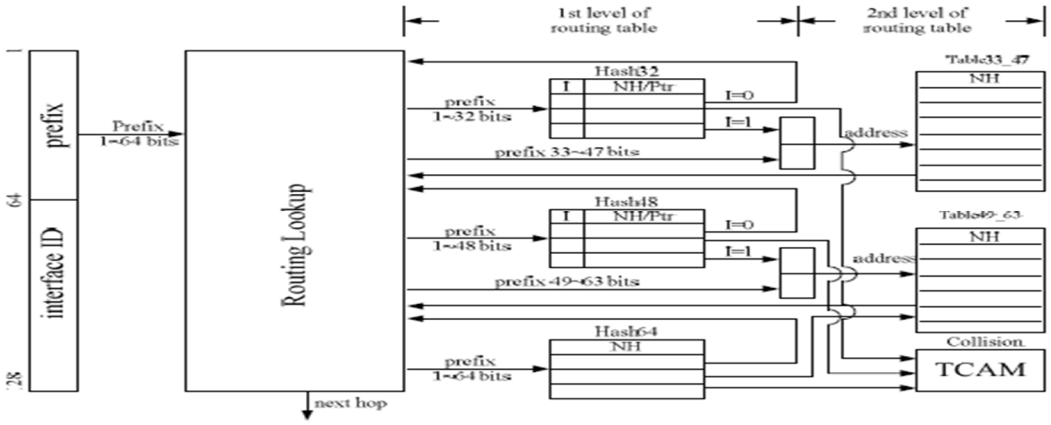


Fig 2.2 : The architecture of routing lookup system

The TCAM performs a parallel search to achieve high performance routing lookup. The second layer of the routing table contains two tables: TAB33_47, which stores entries with prefixes lengths between 33 and 47 bits; and TAB49_63, which stores entries with prefixes between 49 and 63 bits. The routing lookup ASIC contains the control unit, the datapath and the cache memory implemented in TCAM.

III. EXPERIMENTAL RESULTS

A. Farmer

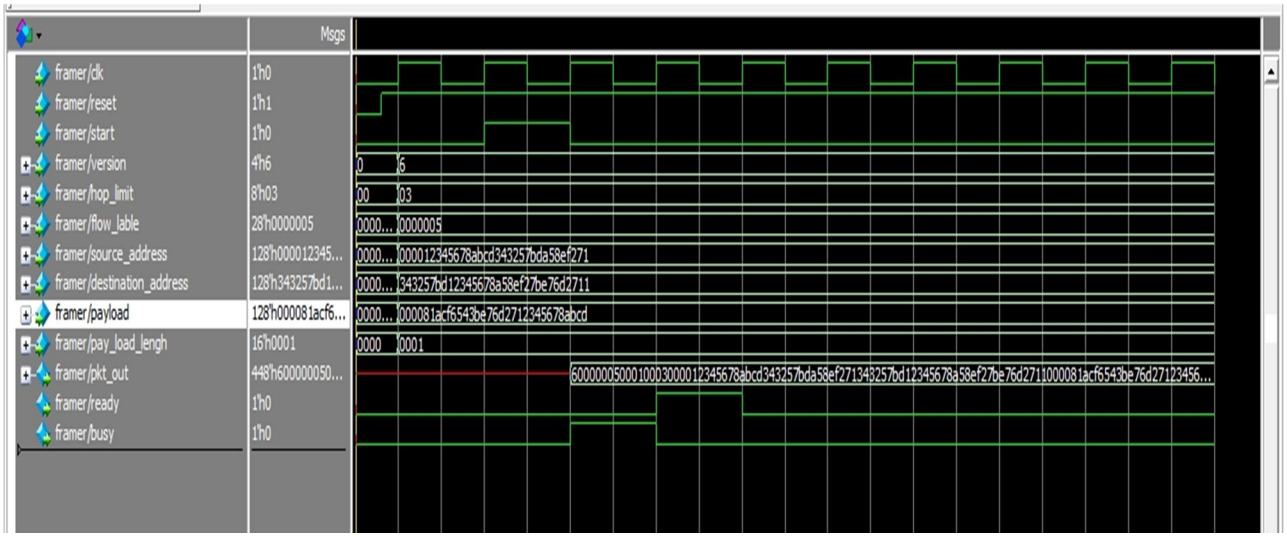


Fig 3.1 : Waveform showing the output of Framer

B. Payload Read Of A Farmer

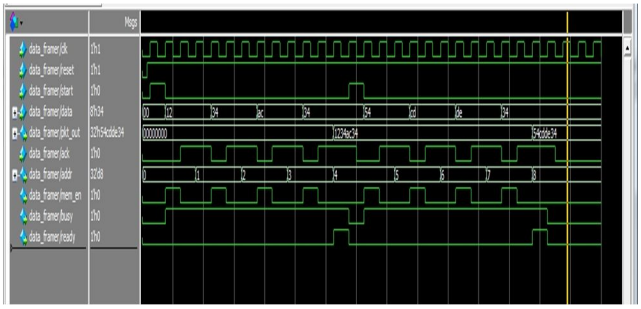


Fig 3.2 : Waveform showing the payload read of a farmer

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C. Data Transmission And Conversion

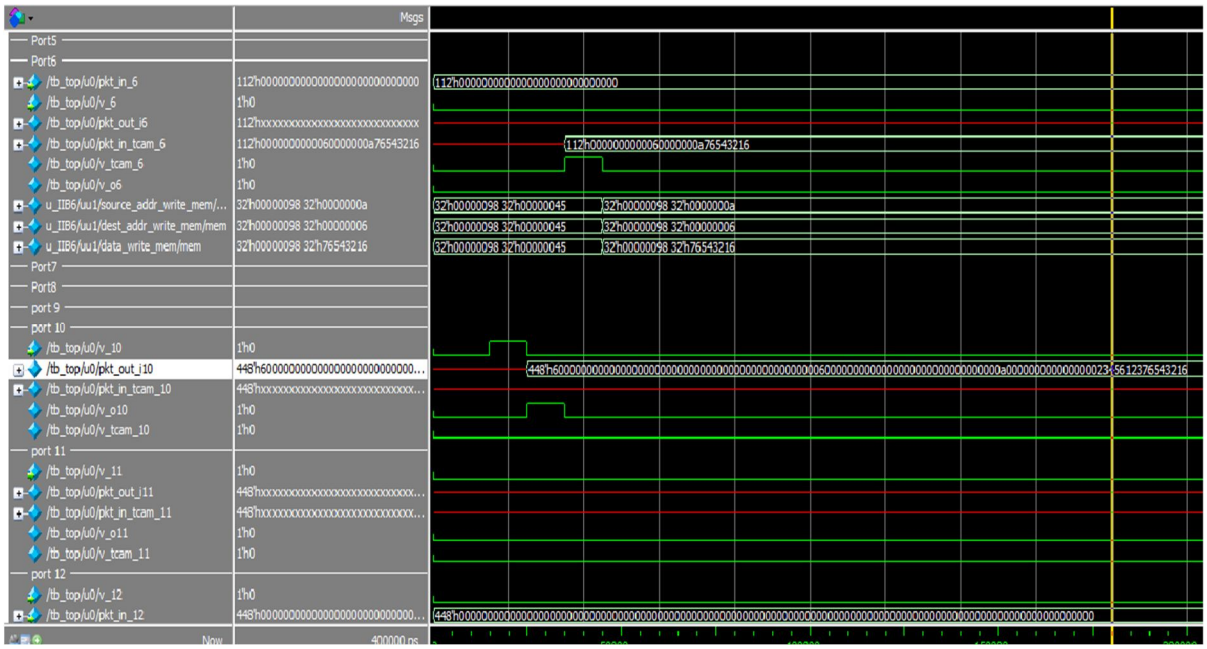


Fig 3.3 Waveform showing the output of simple transfer and packet conversion.

When the enable signal on then the packet containing the source address a will be sent to the destination address 6 as specified. In this case the source address is of version 6 and destination address is of version 4. Hence conversion of version takes place.

IV. CONCLUSION

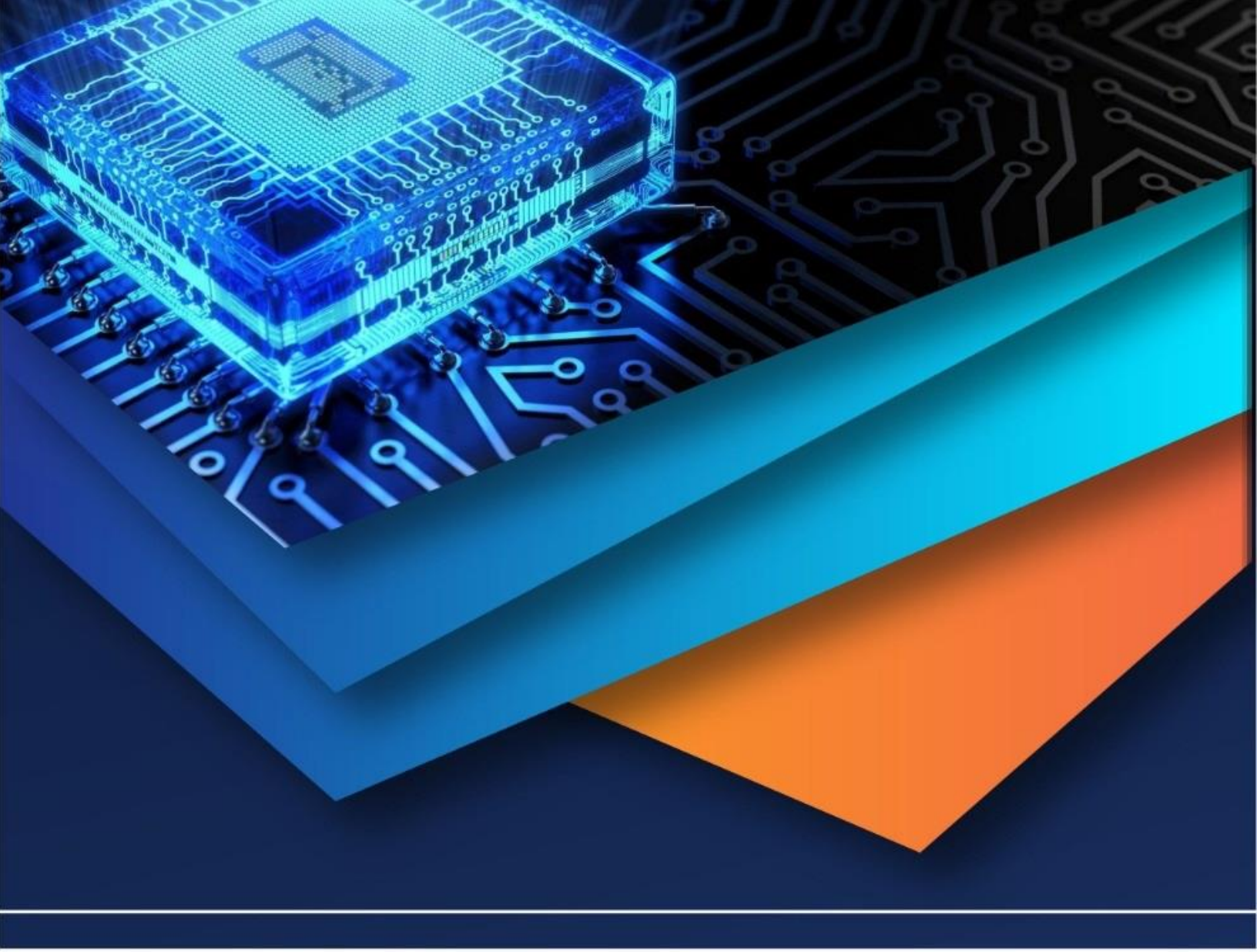
In high-speed networking applications, TCAM has been used as one of the principal components due to its ability to perform fully associative ternary search. This ability can be exploited to perform an wide range of operations, and new applications are still being discovered and implemented. To provide a fair comparison against past techniques when power is concerned, there is a need for an accurate TCAM power model that can be directly compared against comparable SRAM, cache, and logic models.

This Project is mainly concerned about providing robustness to the router for networking purpose with multiple protocols and multiple IP packets. Packet framing, reading packet from the memory and writing packet into the memory of the router is designed and the packet processing is done without collision. The TCAM is designed along with the v6/v4 converter. Hence This model will enable realistic energy estimations to be made across a wide range of TCAM based applications and designs. Presently the design is built and simulated for 16-nodes. It find difficulty to implement because of huge combinational logic as a reason implementation is realized for 8-nodes.

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